Precision, 20-MHz, 1-pA, Low-Noise, RRIO, CMOS Operational Amplifier

General Description

ET85202 is a dual low-voltage (1.8 V to 5.5 V) operational amplifier (op amp) with very low noise and wide bandwidth capabilities while operating on a low quiescent current of only 1.5 mA.

ET85202 is ideal for low-power, single-supply applications. Low-noise (7 nV/√Hz) and high speed operation also make it well-suited for driving sampling analog-to-digital converters (ADCs).Other applications include signal conditioning and sensor amplification.

ET85202 features a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of typically 114 dB over the full input range. The input common mode range extends 100 mV beyond the negative and positive supply rails. The output voltage typically swings within 10 mV of the rails.

Features

- Precision with Zero-Crossover Distortion:
  - Low Offset Voltage: 150 μV (Maximum)
  - High CMRR: 114 dB
  - Rail-to-Rail I/O
- Low noise: 7 nV/√Hz at 10 kHz
- Wide Bandwidth: 20 MHz
- Slew Rate: 10 V/μs
- Quiescent Current: 1.5 mA/Ch
- Single-Supply Voltage Range: 1.8 V to 5.5 V
- Unity-Gain Stable

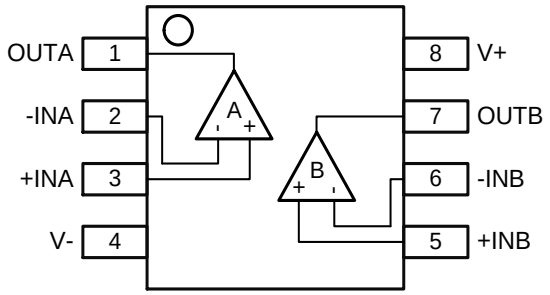
Applications

- High-Z Sensor Signal Conditioning
- Transimpedance Amplifiers
- Test and Measurement Equipment
- Programmable Logic Controllers (PLCs)
- Motor Control Loops
- Communications
- Input/Output ADC/DAC Buffers
- Active Filters

Device information

Part No.	Package	Tape / Reel
ET85202M	SOP8	Tape and Reel

Pin Configuration



Top View

Pin Function

Pin Number	Symbol	Descriptions
1,7	OUT	Output
4	V-	Negative supply
3,5	+IN	Non-inverting input
2,6	-IN	Inverting input
8	V+	Positive supply

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	0 to 6	V
V_{IN}	Signal input terminals Voltage(1)	(V-)-0.5 to (V+)+0.5	V
I_{IN}	Signal input terminals Current(1)	-10 to +10	mA
I_{SC}	Output short-circuit current(2)	Continuous	mA
V_{ESD}	ESD (Human Body Model)	±4000	V
	ESD (Component Discharge Model)	±1000	V
	ESD (Machine Model)	±200	V
T_{STG}	Storage Temperature Range	-65 to +150	°C
$T_{J(MAX)}$	Max Junction Temperature Range	+150	°C
T_A	Operating Temperature Range	-40 to +125	°C

Note1: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.

Note2: Short-circuit to ground, one amplifier per package.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	122.6	°C/W

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_S	Supply Voltage: (V+) - (V-)	1.8(±0.9) ~ 5.5(±2.75)	V
T_A	Operating Temperature Range	-40 ~ +125	°C

Electrical Characteristics

V_S = (V+) – (V-) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{CM} = V_{OUT} = V_S/2 (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±40	±150	µV
$\Delta V_{OS}/\Delta T$	Input offset voltage vs temperature	V_S = 5.5V,T_A = –40°C to +125°C		±1.5	±5	µV/°C
PSRR	Input offset voltage vs power supply	V_S = 1.8 to 5.5 V		±5	±20	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V-)-0.1		(V+)+0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V-) - 0.1 V < V_{CM}< (V+) + 0.1 V		114		dB
INPUT BIAS CURRENT						
I_B	Input bias current(3)	T_A = 25°C		±1		pA
I_{OS}	Input offset current(3)	T_A = 25°C		±1		pA
NOISE						
E_n	Input voltage noise (peak to peak)	f = 0.1 Hz to 10 Hz		2.8		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		
i_n	Input current noise density(3)	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			5		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ,		132		dB
		0.2 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ,		123		
PM	Phase margin	V_S = 5 V, C_L=50pF		47		°

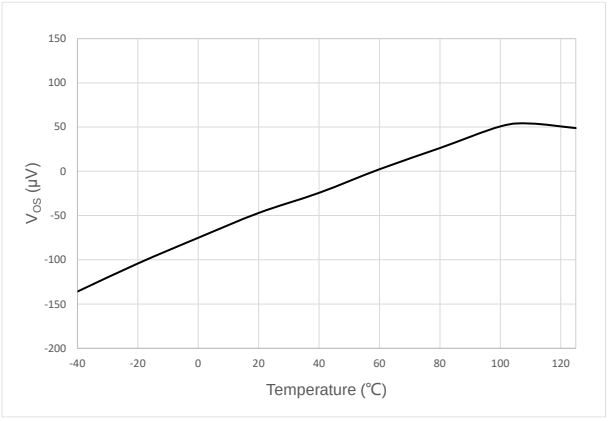
Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY RESPONSE, V_S = 5 V, C_L = 50 pF						
GBP	Gain-bandwidth product	Unity gain		20		MHz
SR	Slew rate	G =+1		10		V/μs
t_S	Settling time(3)	To 0.1%,2V step, G = +1		0.25		μs
		To 0.01%, 2V step, G = +1		0.32		
t_{OR}	Overload recovery time	V_{IN} × gain > V_S		100		ns
THD+N	Total harmonic distortion + noise	V_O = 4 V_{pp}, G = 1, f = 1 kHz, R_L = 10 kΩ		0.0004		%
		V_O = 2 V_{pp}, G = 1, f = 1 kHz, R_L = 600Ω		0.0005		%
OUTPUT						
V_O	Voltage output swing from supply rails	R_L = 10 kΩ, T_A = 25°C		10	20	mV
		R_L = 2 kΩ, T_A = 25°C		25	35	
		R_L = 10 kΩ, T_A = -40°C to 125°C			30	
		R_L = 2 kΩ, T_A = -40°C to 125°C			45	
I_{SC}	Short-circuit current	V_S = 5.5 V		±70		mA
Z_O	Open-loop output impedance(3)	I_O = 0mA, f = 1MHz		90		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		1.5	1.7	mA
		I_O = 0 mA, V_S = 5.5 V, T_A = -40°C to 125°C			1.8	

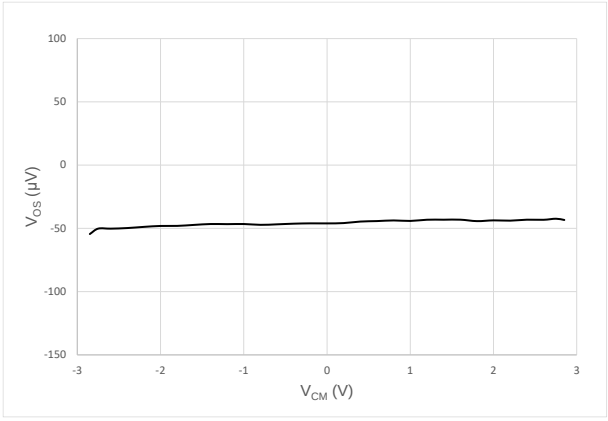
Note3:Guaranteed by design.

Typical Characteristics

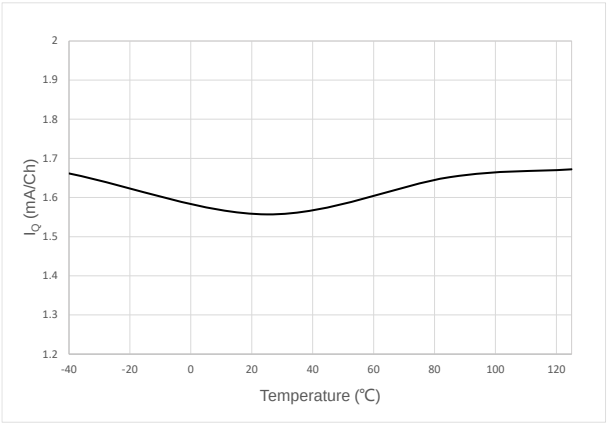
V_S = 5.5 V(±2.75V), V_{CM} = V_{OUT} = V_S/2, and R_L = 10kΩ connected to V_S/2,T_A = 25°C (unless otherwise noted)



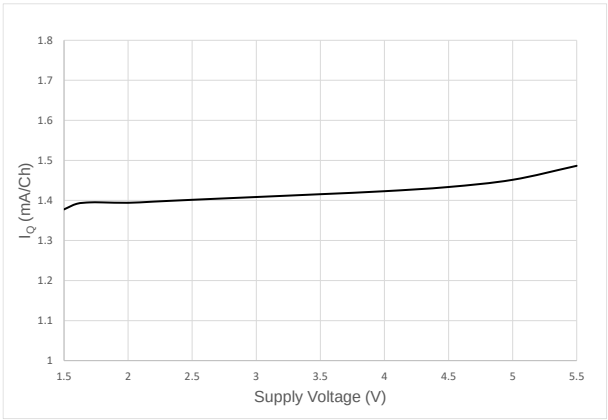
Offset Voltage vs Temperature



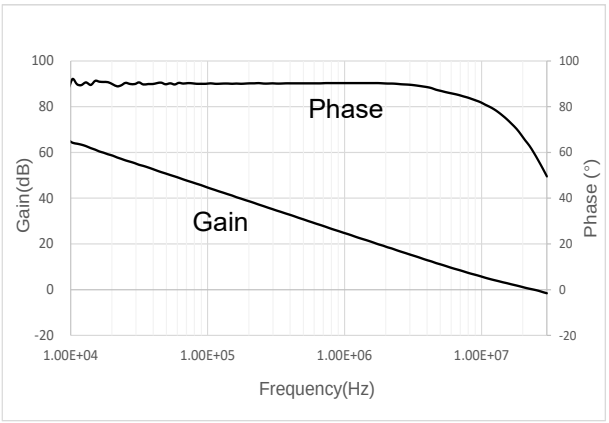
Offset Voltage vs Common-Mode Voltage



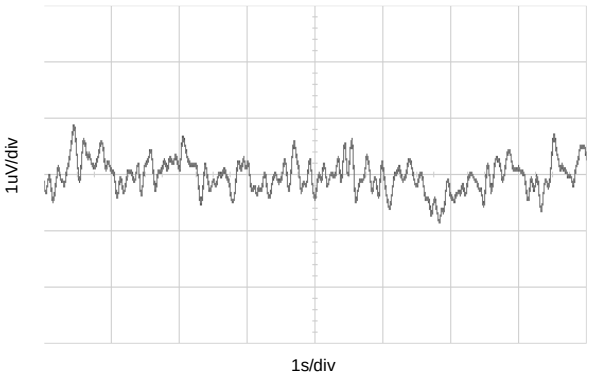
Quiescent Current vs Temperature



Quiescent Current vs Supply Voltage

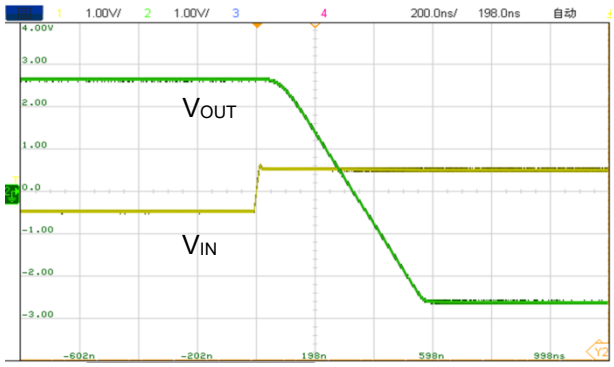


Open-Loop Gain vs Frequency

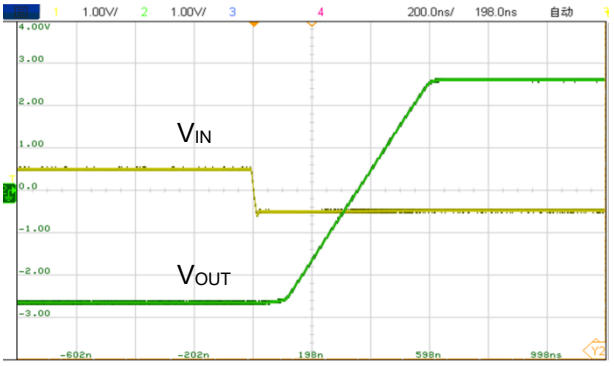


0.1 Hz to 10 Hz Noise

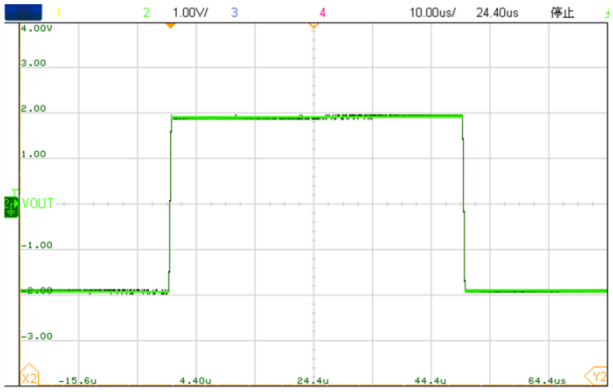
Typical Characteristics (Continued)



Positive Overload Recovery
(G = -10)



Negative Overload Recovery
(G = -10)



Large-Signal Step Response
(G = +1,R_L = 10 kΩ, C_L = 100 pF)

Small-Signal Step Response(100 mV)
(G = +1,R_L = 10 kΩ, C_L = 100 pF)

Functional Description

Overview

ET85202 is a high-speed, precision amplifier, perfectly suited to drive 12-, 14-, and 16-bit analog-to-digital converters. Low output impedance with flat frequency characteristics and zero-crossover distortion circuitry enable high linearity over the full input common mode range, achieving true rail-to-rail input from a 1.8 V to 5.5 V single supply.

Operating Voltage

ET85202 is unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), making it highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 µF to 0.1 µF). ET85202 is fully specified from 1.8 V to 5.5 V and over the extended temperature range of -40°C to 125°C.

Rail-to-Rail Input

ET85202 features true rail-to-rail input operation, with supply voltages as low as ±0.9 V (1.8 V). ET85202 includes an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6 V above the external supply (V_{S+}). This internal supply rail allows the single differential input pair to operate and remain very linear over a very wide input common mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary input stage operational amplifiers. This topology allows the ET85202 to provide superior common-mode performance (CMRR > 110 dB, typical) over the entire common-mode input range, which extends 100 mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear V_{CM} range of the ET85202 assures maximum linearity and lowest distortion.

Capacitive Load and Stability

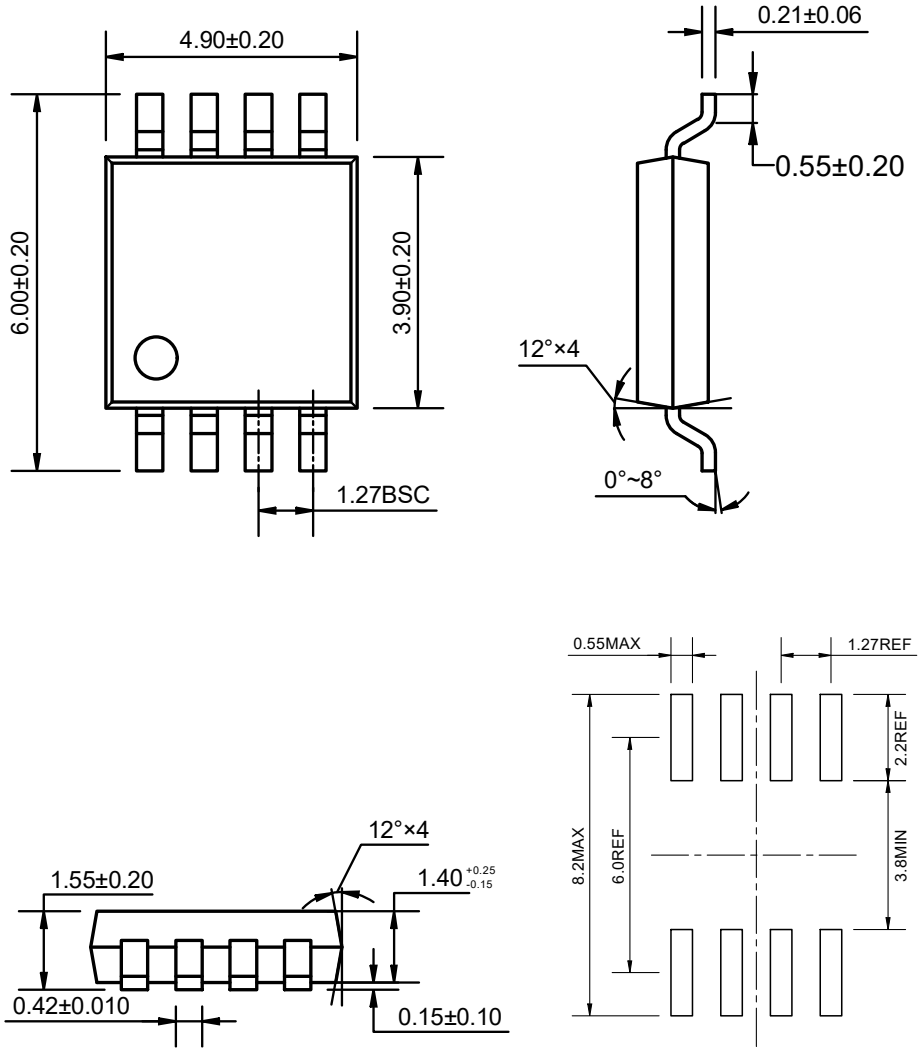
ET85202 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the ET85202 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, ET85202 remains stable with a pure capacitive load up to approximately 1 nF.

Layout Guidelines

ET85202 is a wideband amplifier. To realize the full operational performance of the device, good high frequency PCB layout practices are required. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

Package Dimension

SOP8



Recommended Land Pattern

Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2024-10-25	Original Version	Qinpl	Jiangxw	Liujy