USB Type-C Analog Audio Switch with Protection Function

General Description

ET7480M is a high performance USB Type-C port multimedia switch which supports analog audio headsets. ET7480M can pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal through USB Type-C port. It also supports low resistance switch with as high as 20V high voltage protection function on SBU port and USB port on USB Type-C receptacle side.

Features

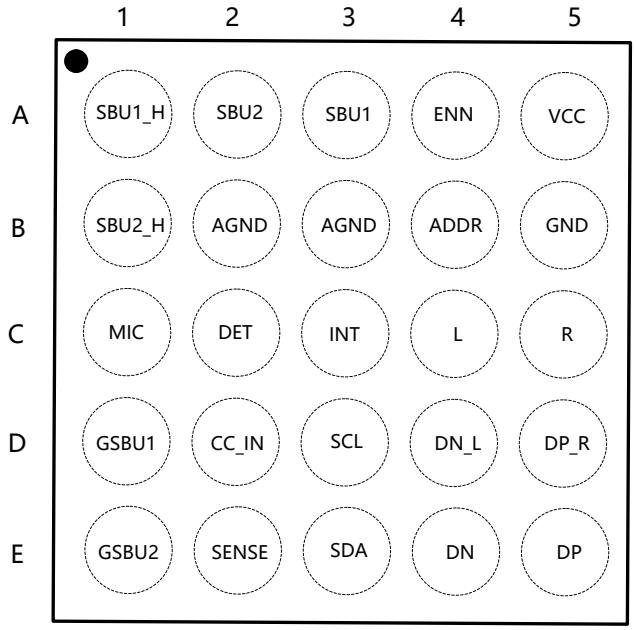
- Power Supply of VCC is from 2.7 V to 5.5 V
- USB High Speed (480Mbps) Switch
  - -3dB bandwidth up to 750MHz
  - R_{ON} Typical is 3Ω
- Audio Switch
  - Negative Rail Capability is range of -3V~ +3V
  - THD+N = -110dB (@1VRMS, f=20Hz~20 kHz, 32Ω R_{LOAD})
  - R_{ON} Typical is 1Ω
- High Voltage Protection
  - 20 V DC Tolerance on Connector Side Pins
  - Over Voltage Protection : V_{TH} = 5 V (Typ)
- OMTP and CTIA Pin Out Support
- Compatible with the 1.2V signal communication
- Support Audio Sense Path
- Part No. and Package

Part NO.	Package	MSL
ET7480M	WLCSP25 (2.31mm × 2.34mm, ball pitch=0.4mm)	Level 1

Applications

- Mobile Phone, Tablet
- Notebook PC, Media Player

Pin Configuration

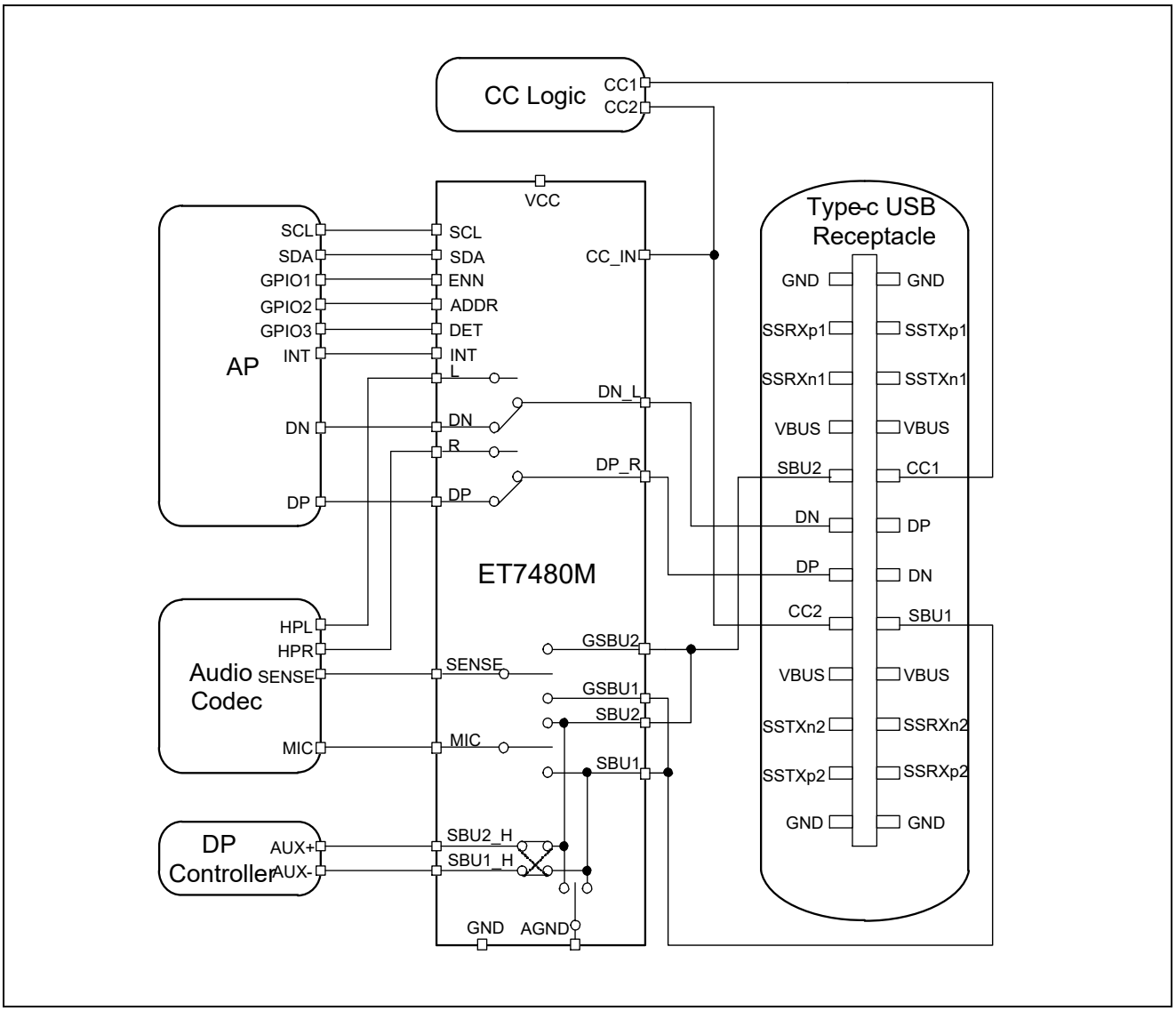


TOP VIEW

Pin Function

Pin No.		Name	Pin Function
1	A5	VCC	Power Supply (2.7 to 5.5 V)
2	B5	GND	Ground
3	D5	DP_R	USB/Audio Common Connector
4	D4	DN_L	USB/Audio Common Connector
5	E5	DP	USB2.0 Data (D+)
6	E4	DN	USB2.0 Data (D–)
7	C5	R	Audio – Right Channel
8	C4	L	Audio – Left Channel
9	A3	SBU1	Sideband Use Wire 1
10	A2	SBU2	Sideband Use Wire 2
11	C1	MIC	Microphone Signal
12	B2	AGND	Audio Signal Ground
13	B3	AGND	Audio Signal Ground
14	E2	SENSE	Audio Ground Reference Output
15	C3	INT	I^2C Interrupt Output, Active Low (open drain)
16	D2	CC_IN	Audio Accessory Attachment Detection Input
17	D1	GSBU1	Audio Sense Path 1 to Headset Jack GND
18	E1	GSBU2	Audio Sense Path 2 to Headset Jack GND
19	C2	DET	Push-pull Output. When CC_IN>1.5V, DET is Low; CC_IN<1.2V, DET is High
20	D3	SCL	I^2C Clock
21	E3	SDA	I^2C Data
22	B1	SBU2_H	Host Side Sideband Use Wire 2
23	A1	SBU1_H	Host Side Sideband Use Wire 1
24	A4	ENN	Chip Enable, Active, Internal Pull-down by 470kΩ
25	B4	ADDR	I^2C Slave Address Pin

Block Diagram

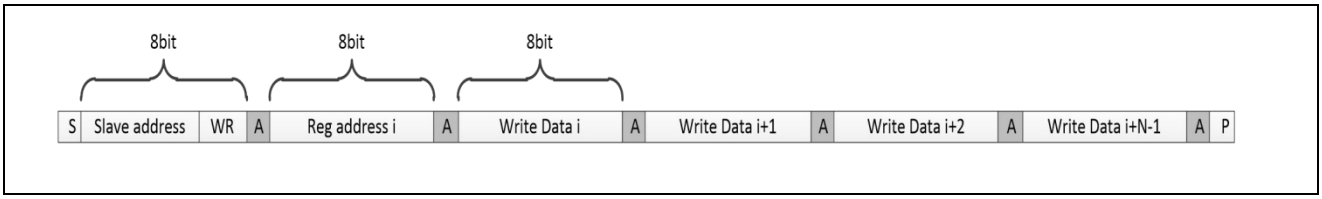


Functional Description

I²C Interface

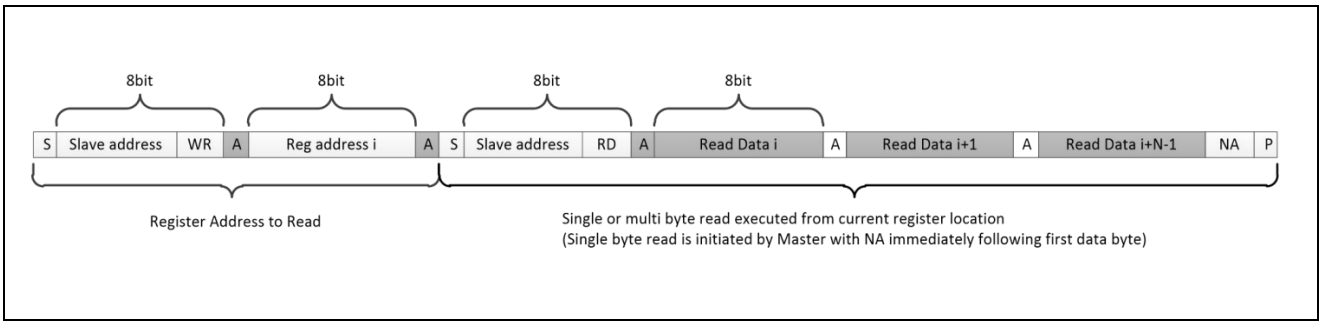
The ET7480M includes a full I²C slave controller which fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz signals.

Examples of an I²C write and read sequence are shown in below figures respectively.



Note: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 1. I²C Write Example



Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

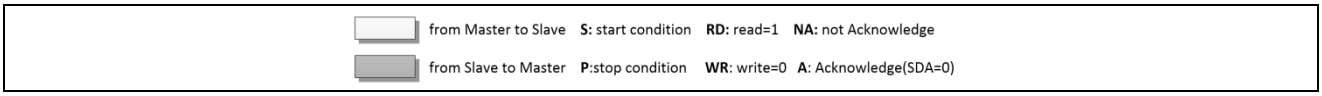


Figure 2. I²C Read Example

Over-Voltage Protection

The over-voltage protection (OVP) on receptacle side pins will switch off the internal signal routing path if the input voltage exceeds the OVP threshold. When OVP is occurred, interrupt signal can be send by INT signal and FLAG data will provide information that which pin had OVP event.

Headset Detection

ET7480M integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling.

	Device Disable	Device Enable
CC_IN < V_{TH_L} = 1.2 V	DET = 0	DET = 1
CC_IN > V_{TH_H} = 1.5 V	DET = 0	DET = 0

MIC Switch Auto-off Function

The function is active during control bit 0x12h bit[2] = 1.
When CC_IN is high (CC_IN > 1.5 V) and L/R/Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50us first. Then it shows high-Z status under MIC switch is set to on status.

Audio Ground Detection and Configuration

The function is active when control bit 0x12h bit[0] = 1 and R, L AGND switches are set to be on status.

For type-C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R and L switches will turn on according to switch configuration and timing setting. MIC, Sense and Audio ground will turn on according to detection results and timing control setting.

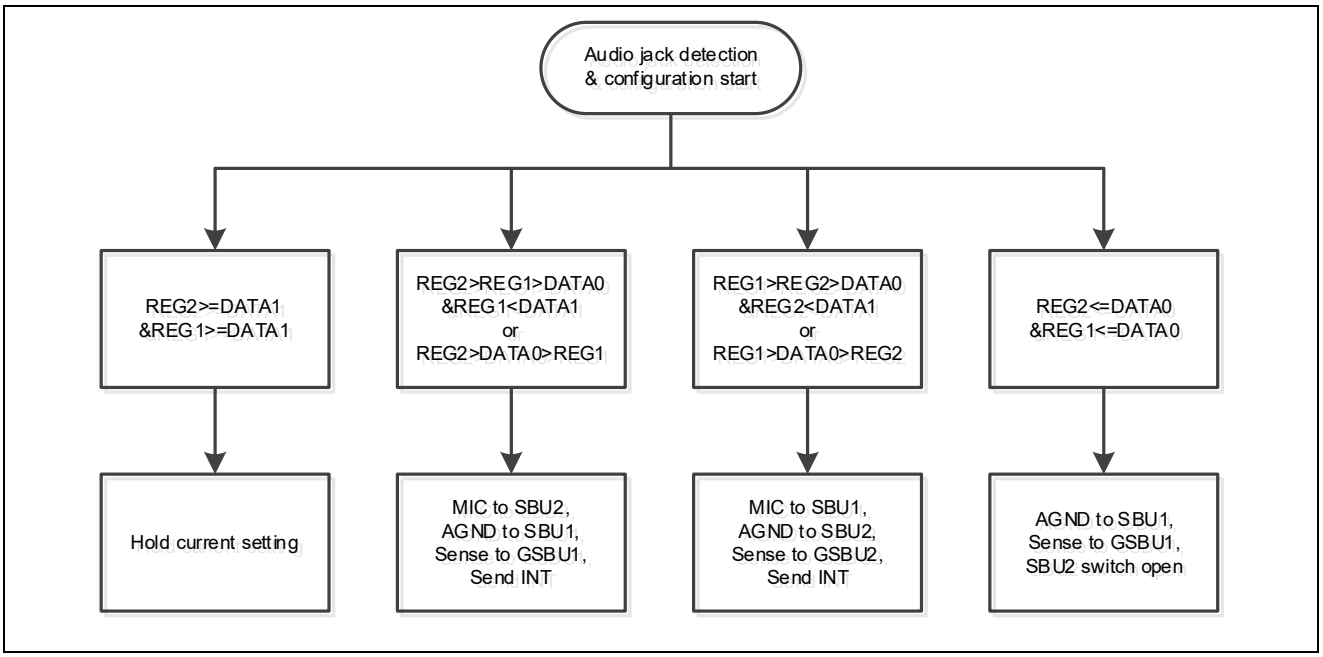


Figure 3. Audio Ground Detection and Configuration

Resistance Detection

The function is active during control bit 0x12h bit[1] = 1.

It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register.

The measurement could be from 1 k to 2.56 M which is controlled by internal register. The detection interval can be set at 100 ms, 1 s or 10 s by register 0x16h.

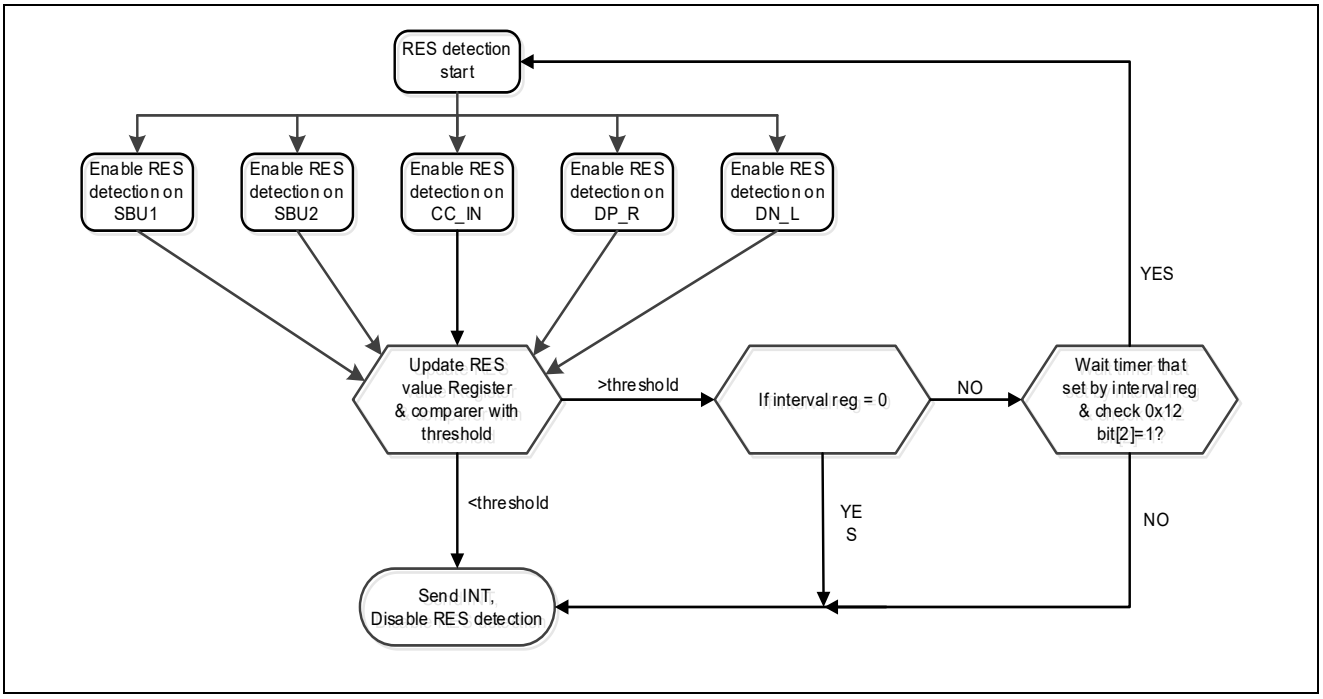


Figure 4. Resistance Detection

Manual Switch Control

The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF.

It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.

Power	ENN	ADDR	INT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/ Audio GND Switch	SBU by Pass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	OFF	OFF	DP_R to DP DN_L to DN	OFF	OFF	ON SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	0	1	OFF	OFF	DP_R to DP DN_L to DN	OFF	OFF	ON SBU1 to SBU2_H SBU2 to SBU1_H
ON	L	1	0	GSBU2 to SENSE	ON	OFF	DP_R to R DN_L to L	SBU1 to MIC SBU2 to AGND	OFF
ON	L	1	1	GSBU1 to SENSE	ON	OFF	DP_R to R DN_L to L	SBU2 to MIC SBU1 to AGND	OFF

Register Information

Register Maps

Addr	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0x88	1	0	0	0	1	0	0	0
01H	OVP Interrupt Mask	R/W	0x00	Reserved	Mask OVP Interrupt	Mask DP_R OVP	Mask DN_L OVP	Mask SBU1 OVP	Mask SBU2 OVP	Mask GSBU1 OVP	Mask GSBU2 OVP
02H	OVP Interrupt Flag	R/C	0x00	Reserved		DP_R	DN_L	SBU1	SBU2	GSBU1	GSBU2
03H	OVP Status	R	0x00	Reserved		DP_R	DN_L	SBU1	SBU2	GSBU1	GSBU2
04H	Switch Settings Enable	R/W	0x98	Device control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	AGND to SBUx
05H	Switch Select	R/W	0x18	Reserved	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	AGND to SBUx
06H	Switch Status0	R	0x05	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status1	R	0x00	Reserved				SBU2 Switch Status		SBU1 Switch Status	
08H	Audio L Switch Slow Turn On Control	R/W	0x01	Audio Switch Left Channel Slow Control [7:0]							
09H	Audio R Switch Slow Turn On Control	R/W	0x01	Audio Switch Right Channel Slow Control [7:0]							
0AH	MIC Switch Slow Turn On Control	R/W	0x01	MIC Switch Channel Slow Control [7:0]							
0BH	Sense Switch Slow Turn On Control	R/W	0x01	Sense Switch Channel Slow Control [7:0]							

Register Maps(Continued)

Addr	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0CH	AGND Switch Slow turn on Control	R/W	0x01	Audio Ground Switch Channel Slow Control [7:0]							
0DH	Timing Delay Between R/L Switch Enable	R/W	0x00	Timing Delay Between R Switch Enable and L Switch Enable Control [7:0]							
0EH	Timing Delay Between MIC/L Switch Enable	R/W	0x00	Timing Delay between MIC Switch Enable and L Switch Enable Control [7:0]							
0FH	Timing Delay Between Sense/L Switch Enable	R/W	0x00	Timing Delay between Sense Switch Enable and L Switch Enable Control [7:0]							
10H	Timing Delay Between AGND/L Switch Enable	R/W	0x00	Timing Delay between Audio Ground Switch Enable and L Switch Enable Control [7:0]							
11H	Audio Accessory Status	R	0x01	Reserved						CC_IN	DET
12H	Function Enable	R/W	0x08	Reserved	DET I/O Control	RES Detection Range Setting	GIPO Control	SLOW Turn-on Control	MIC Auto Control	RES Detection: Auto Clear	Audio Jack Detection: Auto Clear
13H	RES Detection Pin Select	R/W	0x00	Reserved					Detection Pin Select [2:0]		
14H	RES Detection Value	R	0xFF	R Detection Value [7:0]							

Register Maps(Continued)

Addr	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
15H	RES Detection Interrupt Threshold	R/W	0x16	R Detection Interrupt Resistance Threshold [7:0]							
16H	RES Detection Interval	R/W	0X00	Reserved						Detection Interval [1:0]	
17H	Audio Jack Status	RO	0x01	Reserved				4pole, SBU2 MIC	4pole, SBU1 MIC	3pole	No audio
18H	Detection Interrupt	R/C	0x00	Reserved					Audio Detection Done	Low RES Detection Occurred	RES Detection Done
19H	Detection Interrupt Mask	R/W	0x00	Reserved					Audio Detection Done Mask	RES Detection Occurred Mask	RES Detection Done Mask
1AH	Audio Detection RGE1	RO	0xFF	Audio Detection Value REG1 [7:0]							
1BH	Audio Detection RGE2	RO	0xFF	Audio Detection Value REG2 [7:0]							
1CH	MIC Threshold DATA0	R/W	0x20	MIC Threshold Value DATA0 [7:0]							
1DH	MIC Threshold DATA1	R/W	0xFF	MIC Threshold Value DATA1 [7:0]							
1EH	I^2C Reset	W/C	0x00	Reserved							I^2C Reset
1FH	Current Source Setting	R/W	0x00	Reserved	Current Source Setting [3:0]						

Register specification

I²C Slave Address

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR=L	1	0	0	0	0	1	0	R/W
ADDR=H	1	0	0	0	0	1	1	R/W

00H: Device ID

Address: 00h

Reset Value: 8'b 1000_1000

Type:Read

Bits	Name	Description
7:6	Vendor ID	Vendor ID
5:3	Version ID	Device Version ID
2:0	Revision ID	Revision History ID

01H: OVP Interrupt Mask

Address: 01h

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
7	Reserved	Do Not Use
6	OVP Interrupt mask control	OVP Interrupt function Enable/Disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	0: Don't mask DP_R OVP interrupt 1: Mask DP_R OVP interrupt
4	DN_L OVP Interrupt mask control	0: Don't mask DN_L OVP interrupt 1: Mask DN_L OVP interrupt
3	SBU1 OVP Interrupt mask control	0: Don't mask SBU1 OVP interrupt 1: Mask SBU1 OVP interrupt
2	SBU2 OVP Interrupt mask control	0: Don't mask SBU2 OVP interrupt 1: Mask SBU2 OVP interrupt
1	GSBU1 OVP Interrupt mask control	0: Don't mask GSBU1 OVP interrupt 1: Mask GSBU1 OVP interrupt
0	GSBU2 OVP Interrupt mask control	0: Don't mask GSBU2 OVP interrupt 1: Mask GSBU2 OVP interrupt

02H: OVP Interrupt Flag

Address: 02h

Reset Value: 8'b 0000_0000

Type:Read Clear

Bits	Name	Description
[7:6]	Reserved	Do Not Use
5	DP_R OVP	0: DP_R OVP event has not occurred 1: DP_R OVP event has occurred
4	DN_L OVP	0: DN_L OVP event has not occurred 1: DN_L OVP event has occurred
3	SBU1 OVP	0: SBU1 OVP event has not occurred 1: SBU1 OVP event has occurred
2	SBU2 OVP	0: SBU2 OVP event has not occurred 1: SBU2 OVP event has occurred
1	GSBU1 OVP	0: GSBU1 OVP event has not occurred 1: GSBU1 OVP event has occurred
0	GSBU2 OVP	0: GSBU2 OVP event has not occurred 1: GSBU2 OVP event has occurred

03H: Current OVP Status

Address: 03h

Reset Value: 8'b 0000_0000

Type:Read

Bits	Name	Description
[7:6]	Reserved	Do Not Use
5	OVP on DP_R PIN	0: DP_R OVP event don't occur 1: DP_R OVP event occur
4	OVP on DN_L PIN	0: DN_L OVP event don't occur 1: DN_L OVP event occur
3	OVP on SBU1 PIN	0: SBU1 OVP event don't occur 1: SBU1 OVP event occur
2	OVP on SBU2 PIN	0: SBU2 OVP event don't occur 1: SBU2 OVP event occur
1	OVP on GSBU1 PIN	0: GSBU1 OVP event don't occur 1: GSBU1 OVP event occur
0	OVP on GSBU2 PIN	0: GSBU2 OVP event don't occur 1: GSBU2 OVP event occur

04H: Switch Enable

Address: 04h

Reset Value: 8'b 1001_1000

Type:Read/Write

Bits	Name	Description
7	Device Enable	0: Device Disable (L/R pull-down by 10kΩ and other switch nodes will be high-Z) 1: Device Enable Device Enable =1 Device enable =0 ENN= 1 Device Disable Device Disable ENN= 0 Device Enable Device Disable
6	SBU1_H to SBUx switches	0: Switch Disable; SBU1_H will be high-Z 1: Switch Enable
5	SBU2_H to SBUx switches	0: Switch Disable; SBU2_H will be high-Z 1: Switch Enable
4	DN_L to DN or L switches	0: Switch Disable; DN_L、DN will be high-Z, L pull-down by 10k Ω 1: Switch Enable
3	DP_R to DP or R switches	0: Switch Disable; DP_R、DP will be high-Z, R pull-down by 10k Ω 1: Switch Enable
2	Sense to GSBUx switches	0: Switch Disable; Sense、GSBU1、GSBU2 will be high-Z 1: Switch Enable
1	MIC to SBUx switches	0: Switch Disable; MIC will be high-Z 1: Switch Enable
0	AGND to SBUx switches	0: Switch Disable; AGND will be high-Z 1: Switch Enable

05H: Switch Select

Address: 05h

Reset Value: 8'b 0001_1000

Type:Read/Write

Bits	Name	Description
7	Reserved	Do Not Use
6	SBU1_H switches	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN or L switches	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP_R to DP or R switches	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

06H: Switch Status 0

Address: 06h

Reset Value: 8'b 0000_0101

Type:Read

Bits	Name	Description
[7:6]	Reserved	Do Not Use
[5:4]	Sense Switch Status	00: Sense Switch is Open/Not Connected 01: Sense to GSBU1 switch ON 10: Sense to GSBU2 switch ON 11: Not Valid
[3:2]	DP_R Switch Status	00: DP_R Switch is Open/Not Connected 01: DP_R to DP switch ON 10: DP_R to R switch ON 11: Not Valid
[1:0]	DN_L switch Status	00: DN_L Switch is Open/Not Connected 01: DN_L to DN switch ON 10: DN_L to L switch ON 11: Not Valid

07H: Switch Status 1

Address: 07h

Reset Value: 8'b 0000_0000

Type:Read

Bits	Name	Description
[7:6]	Reserved	Do Not Use
[5:3]	SBU2 Switch Status	000: SBU2 switch is Open/Not Connected 001: SBU2 to MIC switch ON 010: SBU2 to AGND switch ON 011: SBU2 to SBU1_H switch ON 100: SBU2 to SBU2_H switch ON 101: SBU2 to both SBU1_H and SBU2_H switch ON 110~111: Not Valid
[2:0]	SBU1 Switch Status	000: SBU1 switch is Open/Not Connected 001: SBU1 to MIC switch ON 010: SBU1 to AGND switch ON 011: SBU1 to SBU1_H switch ON 100: SBU1 to SBU2_H switch ON 101: SBU1 to both SBU1_H and SBU2_H switch ON 110~111: Not Valid

08H: Audio Switch Left Channel Slow Turn-on

Address: 08h

Reset Value: 8'b 0000_0001

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 25600 us
		……
		00000001: 200 us
		00000000: 100 us

09H: Audio Switch Right Channel Slow Turn-on

Address: 09h

Reset Value: 8'b 0000_0001

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 25600 us
		……
		00000001: 200 us
		00000000: 100 us

0AH: MIC Switch Slow Turn-on

Address: 0Ah

Reset Value: 8'b 0000_0001

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 25700 us
		……
		00000010: 350 us
		00000001: 250 us
		00000000: Not Valid

0BH: SENSE Switch Slow Turn-on

Address: 0Bh

Reset Value: 8'b 0000_0001

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 25600 us
		……
		00000001: 200 us
		00000000: 100 us

0CH: AGND Switch Slow Turn-on

Address: 0Ch

Reset Value: 8'b 0000_0001

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 179000 us
		……
		00000001: 1400 us
		00000000: 700 us

0DH: Timing Delay Between R Switch and L Switch Enable

Address: 0Dh

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	11111111: 25500 us
		11111110: 25400 us
		……
		00000001: 100 us
		00000000: 0 us

0EH: Timing Delay Between MIC Switch and L Switch Enable

Address: 0Eh

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	11111111: 25500 us
		11111110: 25400 us
		……
		00000001: 100 us
		00000000: 0 us

0FH: Timing Delay Between SENSE Switch and L Switch Enable

Address: 0Fh

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	11111111: 25500 us
		11111110: 25400 us
		……
		00000001: 100 us
		00000000: 0 us

10H: Timing Delay Between AGND Switch and L Switch Enable

Address: 10h

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	11111111: 25500 us
		11111110: 25400 us
		……
		00000001: 100 us
		00000000: 0 us

11H: Audio Accessory Status

Address: 11h

Reset Value: 8'b 0000_0001

Type:Read

Bits	Name	Description
[7:2]	Reserved	Do Not Use
1	CC_IN	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	DET	0: DET output is low 1: DET output is high

12H: Function Enable

Address: 12h

Reset Value: 8'b 0000_1000

Type:Read/Write

Bits	Name	Description
7	Reserved	Do Not Use
6	DET I/O Control	1: DET pin is Open/Drain Output 0: DET pin is Push/Pull Output
5	RES detection range setting	1: 10k to 2560 k 0: 1k to 256 k
4	GPIO control enable	1: Enable (Manual Switch Control) 0: Disable
3	Slow turn on control enable	1: Enable 0: Disable
2	MIC auto break out Control enable	1: Enable 0: Disable
1	RES detection enable	1: Enable; will be changed to 0 after resistance detection 0: Disable

0	Audio jack detection and configuration enable	1: Enable; will be changed to 0 after audio jack detection and configuration 0: Disable

During 0x12h bit[4]=1, Manual Switch Control is active, 0x04h is read-only, I²C Slave Address is fixed **8'b1000_0100**.

13H: RES Detection Pin Setting

Address: 13h

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:3]	Reserved	Do Not Use
[2:0]	Pin selection	000: CC_IN 001: DP_R 010: DN_L 011: SBU1 100: SBU2 101~111: Not Valid

If RES detection pin is enable before setting PIN selection it will always do the CC_IN first. Recommend user to select the pin first before setting the RES detection pin enable.

14H: RES Detection Value

Address: 14h

Reset Value: 8'b 1111_1111

Type:Read

Bits	Name	Description
[7:0]	Detected resistance value	00000000b: R <= 1 k / 10 k ..... 11111111b: R >= 256 k / 2.56 M

15H: RES Detection Threshold

Address: 15h

Reset Value: 8'b 0001_0110

Type:Read/Write

Bits	Name	Description
[7:0]	RES detection threshold	Selection by 1k Ω per step if Reg 12h [5] = 0 Selection by 10k Ω per step if Reg 12h [5] = 1 0000_0000: 1 KΩ /10 KΩ ..... 0001_0110: 23 KΩ/230KΩ Default Value ..... 1111_1111: 256 KΩ / 2560 KΩ

16H: RES Detection Interval

Address: 16h

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:2]	Reserved	Do Not Use
[1:0]	RES detection interval	00: Single 01: 100 ms 10: 1 s 11: 10 s

17H: Audio Jack Status

Address: 17h

Reset Value: 8'b 0000_0001

Type:Read

Bits	Name	Description
[7:4]	Reserved	Do Not Use
3	4 pole	1: 4 Pole (SBU2 to MIC, SBU1 to AGND) 0: others
2	4 pole	1: 4 Pole (SBU1 to MIC, SBU2 to AGND) 0: others
1	3 pole	1: 3 Pole 0: others
0	No audio accessory	1: No audio accessory 0: Audio accessory attached

18H: RES Detection/Audio Jack Detection Interrupt Flag

Address: 18h

Reset Value: 8'b 0000_0000

Type:Read Clear

Bits	Name	Description
[7:3]	Reserved	Do Not Use
2	Audio jack detection and configuration	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
1	Low resistance occurred	0: Low resistance has not occurred 1: Low resistance has occurred
0	Resistance detection done	0: Low resistance has not occurred 1: Low resistance has occurred

19H: RES Detection/Audio Jack Detection Interrupt Mask

Address: 19h

Reset Value: 8'b 0000_0000

Type:Read/Write

Bits	Name	Description
[7:3]	Reserved	Do Not Use
2	Audio jack detection and configuration mask	1: Mask Audio jack detection and configuration interrupt
1	Low resistance occurred mask	1: Mask Low resistance occurred interrupt
0	Resistance detection done mask	1: Mask Low resistance detection interrupt

1AH: Audio Jack Detection REG1 Value

Address: 1Ah

Reset Value: 8'b 1111_1111

Type:Read

Bits	Name	Description
[7:0]	Audio jack detection value	Voltage from resistance between SBU1 and SBU2 (SBU2 = ground) 00000000b: = 0 V …….. 11111111b: = 2.4 V

1BH: Audio Jack Detection REG2 Value

Address: 1Bh

Reset Value: 8'b 1111_1111

Type:Read

Bits	Name	Description
[7:0]	Audio jack detection value	Voltage from resistance between SBU2 and SBU1 (SBU1 = ground) 00000000b: = 0 V …….. 11111111b: = 2.4 V

1CH: MIC Detection Threshold DATA0

Address: 1Ch

Reset Value: 8'b 0010_0000

Type:Read/Write

Bits	Name	Description
[7:0]	MIC detection threshold DATA0	MIC detection threshold DATA0 0010_0000: 300mV

1DH: MIC Detection Threshold DATA1

Address: 1Dh

Reset Value: 8'b 1111_1111

Type:Read/Write

Bits	Name	Description
[7:0]	MIC detection threshold DATA1	MIC detection threshold DATA1 1111_1111: 2.4 V

1EH: I²C Reset

Address: 1Eh

Reset Value: 8'b 0000_0000

Type: Write/Auto Clear

Bits	Name	Description
[7:1]	Reserved	Do Not Use
0	I²C reset	0: Default 1: I²C reset

1FH: Audio Jack Detection Current Setting

Address: 1Fh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Description
[7:4]	Reserved	Do Not Use
[3:0]	Current Source Setting	0000: Not Valid 0001: 100uA .... 0111: 700uA(Default Value) 1111: 1500uA

Absolute Maximum Ratings

Symbol	Name		Min	Max	Unit
V_{CC}	Supply Voltage from V_{CC}		-0.5	6.5	V
V_{VCC_IN}	V_{CC_IN}, to GND		-0.5	20	V
V_{SW_C}	V_{DP_R} to GND, V_{DN_L} to GND		-3.6	20	V
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND		-0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND		-3.6	6.5	V
$V_{V\_SBU/GSBU}$	V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU2} to GND		-0.5	20	V
V_{VSBU_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND		-0.5	6.5	V
$V_{I/O}$	SENSE, MIC, DET, INT, to GND		-0.5	6.5	V
V_{CNTRL}	Control Input Voltage	SDA, SCL, ENN, ADDR	-0.5	6.5	V
I_{SW_Audio}	Switch I/O Current, Audio Path		-250	250	mA
I_{SW_USB}	Switch I/O Current, USB Path		-	100	mA
I_{SW_MIC}	Switch I/O Current, MIC to SBU1 or SBU2		-	50	mA
I_{SW_SBU}	Switch I/O Current, SBUx to SBUx_H		-	50	mA
I_{SW_SENSE}	Switch I/O Current, SENSE to GSBU1 or GSBU2		-	100	mA
I_{SW_AGND}	Switch I/O Current, AGND to SBU1 or SBU2		-	500	mA
I_{IK}	DC Input Diode Current		-50	-	mA
V_{ESD}	Human Body Model, ANSI/ESDA/JEDEC JS-001-2017	Connector Side Pins: SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN	±4000	-	V
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2017	Host Side Pins: The Rest Pins (Include V_{CC})	±2000	-	V
	Charged Device Model, JEDEC JS-001-2018		±2000		V
T_J	Absolute Maximum Junction Operating Temperature		-40	150	°C
T_{STG}	Storage Temperature		-65	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device.

If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommend Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Power					
V_{CC}	Supply Voltage	2.7	-	5.5	V
USB Switch					
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	0	-	3.6	V
Audio Switch					
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	-3.6	-	3.6	V
MIC Switch					
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	0	-	3.6	V
SENSE Switch					
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	0	-	3.6	V
SBU TO SBUX_H Switch					
V_{VGSBU}	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	0	-	3.6	V
CC_IN Pin					
V_{CC_IN}	V_{CC_IN} to GND	0	-	5.5	V
Control Voltage (ENN/SDA/SCL)					
V_{IH}	Input Voltage High	1.1	-	V_{CC}	V
V_{IL}	Input Voltage Low	-	-	0.5	V
Operating Temperature					
T_A	Ambient Operating Temperature	-40	+25	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied.

Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC Electrical Characteristics

V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ) = 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
I_{CC}	Supply Current	USB switches on, SBUx to SBUx_H switches on	V_{CC} =2.7V to 5.5V	-	65	95	uA
		Audio switches on, MIC switch on and Audio GND switch on		-	60	90	uA
I_{CCZ}	Quiescent Current	ADDR=L, ENN = L, 04H'b7 = 0		-	0.5	5	uA
USB/AUDIO Common Pins : DP/R, DN_L							
I_{OZ}	Off Leakage Current of DP_R and DN_L	DN_L, DP_R = -3V to 3.6V	V_{CC} =2.7V to 5.5V	-3.0	-	3.0	uA
I_{OFF}	Power-Off Leakage Current of DP_R and DN_L	DN_L, DP_R = 0 V to 3.6 V	Power off	-3.0	-	3.0	uA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC} =2.7V to 5.5V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis			0.15	0.3	0.5	V
Audio Switch							
I_{ON}	On Leakage Current of Audio Switch	DN_L, DP_R = -3V to 3.0V, DP, DN, R, L = Float	V_{CC} = 2.7V to 5.5V	-2.5	-	2.5	uA
I_{OFF}	Power-Off Leakage Current of L and R	L, R = 0V to 3V, DP_R, DN_L = Float	Power off	-1.0	-	1.0	uA
R_{ON}	Switch On Resistance	I_{SW} = 100mA, V_{SW} = -3V to 3V	V_{CC} = 2.7V to 5.5V	0.7	1	1.3	Ω
R_{SHUNT}	Pull-down Resistor on R/L Pin when Audio Switch is Off	L = R = 3V		6	10	14	kΩ
USB Switch							
I_{ON}	On Leakage Current of USB Switch	DN_L, DP_R = 0V to 3.6V, DP, DN, R, L = Float	V_{CC} = 2.7V to 5.5V	-4.0	-	4.0	uA
I_{OZ}	Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V		-3.0	-	3.0	uA
I_{OFF}	Power-Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V	Power off	-3.0	-	3.0	uA
R_{ON_USB}	USB Switch On Resistance	I_{SW} = 8mA, V_{SW} = 0.4V	V_{CC} =2.7V to 5.5V	2.4	3.5	4.6	Ω
SENSE Switch							
I_{ON}	Sense Path Leakage Current	GSBUx = 0V to 1V, SENSE is floating	V_{CC} = 2.7V to 5.5V	-2.0	-	2.0	uA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
R_{ON}	SENSE Switch On Resistance	I_{OUT} = 100mA, V_{SW} = 1V	V_{CC} = 2.7V to 5.5V	240	350	460	mΩ
I_{OZ}	Off Leakage Current of SENSE	Sense = 0V to 1.0V		-2.0	-	2.0	uA
	Off Leakage Current of GSBUx	GSBUx = 0V to 1.0V		-2.0	-	2.0	uA
		GSBUx = 1V to 3.6V		-3.0	-	3.0	
I_{OFF}	Power-Off Leakage Current of SENSE	Sense = 0V to 1.0V	Power off	-2.0	-	2.0	uA
	Power-Off Leakage Current of GSBUx	GSBUx = 0V to 3.6V		-3.0	-	3.0	
V_{OV_TRIP}	Input OVP Lockout on GSBUx	Rising edge	V_{CC} = 2.7V to 5.5V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis of GSBUx			-	0.3	0.5	V
SBUX Pins							
I_{OZ}	Off Leakage Current of SBUx	SBUx = 0V to 3.6V	V_{CC} = 2.7V to 5.5V	-3.0	-	3.0	uA
I_{OFF}	Power-Off Leakage Current Port SBUx	SBUx = 0V to 3.6V	Power off	-3.0	-	3.0	uA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC} = 2.7V to 5.5V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis			-	0.3	0.5	V
MIC Switch							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0V to 3.6V, MIC is floating	V_{CC} = 2.7V to 5.5V	-3.0	-	3.0	uA
I_{OZ}	Off Leakage Current of MIC	MIC = 0V to 3.6V		-1.0	-	1.0	uA
I_{OFF}	Power Off Leakage Current of MIC	MIC = 0V to 3.6V	Power off	-1.0	-	1.0	uA
R_{ON}	MIC Switch On Resistance	V_{SW} = 3.6V, I_{SW} = 30mA	V_{CC} = 2.7V to 5.5V	3	4	5	Ω
SBUX_H Switch							
I_{ON}	On Leakage Current of SBUx_H Switch	SBUx = 0V to 3.6V, SBUx_H is floating	V_{CC} =2.7V to 5.5V	-3.0	-	3.0	uA
I_{OZ}	Off Leakage of SBUx_H	SBUx_H =0 V to 3.6 V		-1	-	1	uA
I_{OFF}	Power Off Leakage Current of SBUx_H	SBUx_H = 0V to 3.6V	Power off	-1.0	-	1.0	uA
R_{ON}	SBUx_H Switch On Resistance	V_{SW} = 0V to 3.6V, I_{SW} = 30mA	V_{CC} = 2.7V to 5.5V	2.4	3.5	4.6	Ω

DC Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
Audio Ground Switch Pin: AGND TO SBUX							
R_{ON}	AGND Switch On Resistance	I_{SOURCE} = 100mA on SBUx	V_{CC} = 2.7V to 5.5V	25	50	90	mΩ
CC_IN Pin							
V_{TH_L}	Input Low Threshold		V_{CC} = 2.7V to 5.5V	1.05	1.2	-	V
V_{TH_H}	Input High Threshold			-	1.5	1.65	V
I_{IN}	Input Leakage of CC_IN	CC_IN = 0V to 5.5V		-	-	1.0	uA
INT, DET Pins							
V_{OH}	Output High Voltage for DET Pin	I_O = -2mA	V_{CC} = 2.7V to 5.5V	1.5	1.8	2	V
V_{OL}	Output Low Voltage for DET and INT Pins	I_O = 2mA		-	-	0.4	V
ADDR Pin							
V_{IH}	Input voltage High		V_{CC} = 2.7V to 5.5V	1.1	-	-	V
V_{IL}	Input voltage Low			-	-	0.45	V
I_{IN}	Control Input Leakage	ADDR = 0V to V_{CC}		-1	-	1	uA
ENN Pin							
V_{IH}	Input Voltage High		V_{CC} = 2.7V to 5.5V	1.1	-	-	V
V_{IL}	Input Voltage Low			-	-	0.45	V
R_{PD}	Internal Pull Down Resistor			330	470	610	KΩ
SDA, SCL Pins							
V_{ILI2C}	Low-Level Input Voltage		V_{CC} = 2.7V to 5.5V	-	-	0.4	V
V_{IHI2C}	High-Level Input Voltage			1.1	-	-	V
I_{I2C}	Input Current of SDA and SCL Pins	SCL/SDA = 0V to 3.6V		-2	-	2	uA
V_{OLSDA}	Low-Level Output Voltage	I_{OL} = 2mA		-	-	0.3	V
I_{OLSDA}	Low-Level Output Current	V_{OLSDA} = 0.2V	V_{CC} = 2.7V to 5.5V	10	-	-	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC Electrical Characteristics

V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ) = 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
Audio Switch							
t_{DELAY}	Audio Switch Turn On Delay Time	DP_R = DN_L = 1V, R_L = 32Ω	V_{CC} =3.3V	-	110	130	us
t_{RISE}	Audio Switch Turn On Rising Time (1)	DP_R = DN_L = 1V, R_L = 32Ω		-	240	350	us
t_{OFF}	Audio Switch Turn Off Time	DP_R = DN_L = 1V, R_L = 32Ω		-	20	40	us
X_{TALK}	Cross Talk (Adjacent)	f = 1kHz, R_L = 50Ω, V_{SW} = $1V_{RMS}$		-	-100	-	dB
BW	-3 dB Bandwidth	R_L = 50Ω		-	600	-	MHz
O_{IRR}	Off Isolation	f = 1 kHz, R_L = 50Ω, C_L = 0pF,V_{SW} = $1V_{RMS}$		-	-100	-	dB
THD+N	Total Harmonic Distortion + Noise Performance with A-weighting Filter	R_L = 600Ω, f = 20Hz~20kHz, V_{SW} = $2V_{RMS}$		-	-110	-	dB
		R_L = 32Ω, f = 20Hz~20kHz, V_{SW} = $1V_{RMS}$		-	-110	-	
		R_L = 16Ω, f = 20Hz~20kHz, V_{SW} = $0.5V_{RMS}$		-	-108	-	
USB Switch							
t_{ON}	USB Switch Turn-on Time	DP_R = DN_L = 1.5V, R_L = 50Ω	V_{CC}=3.3V	-	70	120	us
t_{OFF}	USB Switch Turn -off Time	DP_R = DN_L = 1.5V, R_L = 50Ω		-	20	40	us
BW	-3 dB Bandwidth	R_L = 50Ω		-	750	-	MHz
O_{IRR}	Off Isolation between DP, DN and Common Node Pins	f = 1kHz, R_L = 50Ω, C_L = 0pF, V_{SW} = $1V_{RMS}$		-	-100	-	dB
t_{OVP}	DP_R and DN_L pins OVP Response Time(2)	V_{SW} = 3.5V to 5.5V		-	0.8	1.5	us

AC Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
MIC/AUDIO GROUND Switch							
t_{DELAY_MIC}	MIC Switch Turn On Delay Time	SBUx = 1V, R_L = 50Ω	V_{CC} =3.3V	-	100	135	us
t_{RISE_MIC}	MIC Switch Turn On Rising Time (1)			-	350	400	us
t_{DELAY_AGND}	AGND Switch Turn On Time	SBUx pulled up to 0.5V by 16Ω, AGND connect to GND		-	140	165	us
t_{RISE_AGND}	AGND Switch Turn On Rising Time (1)			-	2.5	3.2	ms
t_{OFF_MIC}	MIC Switch Turn Off Time	SBUx = 2.5V, R_L = 50Ω		-	20	40	us
$t_{OFF\_Audio\_GND}$	AGND Switch Turn Off Time	SBUx: I_{SOURCE} = 10mA, clamp to 2.5V		-	20	40	us
BW	MIC Switch Bandwidth	R_L = 50Ω		-	50	-	MHz
SBUX_H Switch							
t_{ON}	SBUx_H Switch Turn On Time	SBUx = 2.5V, R_L = 50Ω	V_{CC} =3.3V	-	120	140	us
t_{OFF}	SBUx_H Switch Turn Off Time			-	20	40	us
BW	Bandwidth	R_L = 50Ω		-	50	-	MHz
t_{OVP}	SBUx Pins OVP ResponseTime (2)	V_{SW} = 3.5V to 5.5V		-	0.5	1	us
SENSE Switch							
t_{DELAY}	Sense Switch Turn On Delay Time	GSBUx = 1V, R_L = 50Ω	V_{CC} =3.3V	-	110	150	us
t_{RISE}	Sense Switch Turn On Rising Time (1)			-	260	320	us
t_{OFF}	Sense Switch Turn Off Time			-	20	40	us
t_{OVP}	GSBUx Pins OVP Response Time	V_{SW} =3.5V to 5.5V	V_{CC} =3.3V	-	0.5	1.5	us
BW	Bandwidth	R_L = 50Ω		-	150	-	MHz
DET Delay							
t_{DELAY_DET}	DET Response Delay	Transition from 0 to 1.8V	V_{CC} =3.3V	-	2.5	5.5	us
		Transition from 1.8V to 0		-	0.2	0.4	

I²C Specification

(V_{CC} = 2.7 V to 5.5, V_{CC} (Typ) = 3.3 V ,T_A = -40°C to 85°C. T_A (Typ) = 25°C, unless otherwise specified)

Symbol	Parameter	Fast Mode		Unit
		Min	Max	
f_{SCL}	I²C_SCL Clock Frequency		400	kHz
$t_{HD;\ STA}$	Hold Time (Repeated) START Condition	0.6		us
t_{LOW}	Low Period of I²C _SCL Clock	1.3		us
t_{HIGH}	High Period of I²C _SCL Clock	0.6		us
$t_{SU;\ STA}$	Set-up Time for Repeated START Condition	0.6		us
$t_{HD;\ DAT}$	Data Hold Time (2)	0	0.9	us
$t_{SU;\ DAT}$	Data Set-up Time (3)	100		ns
t_r	Rise Time of I2C_SDA and I²C _SCL Signals (3)		300	ns
t_f	Fall Time of I2C_SDA and I²C _SCL Signals (3)		300	ns
$t_{SU;\ STO}$	Set-up Time for STOP Condition	0.6		us
t_{BUF}	Bus-Free Time between STOP and START Conditions	1.3		us
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Note1. Turn on timing can be controlled by I²C register.

Note2. Guaranteed by design, not production tested.

Note3. A fast-mode I²C -bus device can be used in a standard-mode I²C -bus system, but the requirement t_{SU}; DAT≥250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C _SCL signal. If such a device does stretch the LOW period of the I²C _SCL signal, it must output the next data bit to the I²C _SDA line t_r_max + t_{SU}; DAT = 1000 + 250 = 1250ns (according to the standard-mode I²C bus specification) before the I²C _SCL line is released.

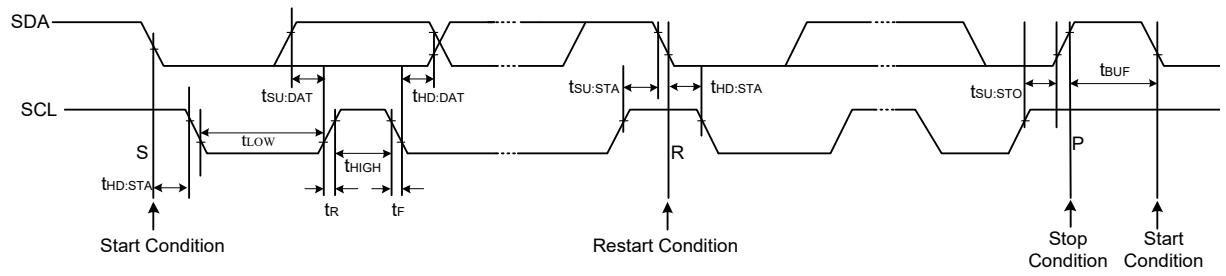


Figure5. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Capacitance

V_{CC}= 2.7 V to 5.5 V, V_{CC} (Typ) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ) = 25°C [(4)]

Symbol	Parameter	Condition		Power	T_A =- 40℃ to +85℃			Unit
					Min	Typ	Max	
$C_{ON\_USB/Audio}$	On Capacitance (Common Port)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias		V_{CC} =3.3V		9		pF
$C_{OFF\_USB/Audio}$	Off Capacitance (Common Port)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				7.5		pF
C_{OFF_USB}	Off Capacitance (Non-Common Ports)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				3		pF
$C_{ON\_SENSE\_SW}$	On Capacitance (Common Ports)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				55		pF
$C_{OFF\_SENSE\_SW}$	Off Capacitance (Common Ports)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				88		pF
$C_{ON\_MIC\_SW}$	On Capacitance (Common Ports)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				200		pF
$C_{OFF\_MIC\_SW}$	Off Capacitance (Common Ports)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				10		pF
$C_{ON\_AGND\_SW}$	On Capacitance (Common Port)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				125		pF
$C_{ON\_SBUx\_H\_SW}$	On Capacitance (Common Port)	f = 1 MHz, 100mV_{PK-PK}, 100mV DC bias				200		pF
C_{CNTRL}	Control Input Pin Capacitance	f = 1MHz, 100mV_{PP}, 100mV DC bias	ENN			3		pF

Note4. All capacitance values guaranteed by design.

Test Diagrams

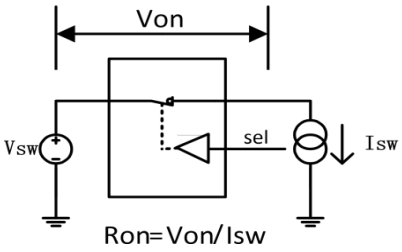


Figure6. on resistance R_{ON}= V_{ON}/I_{SW}

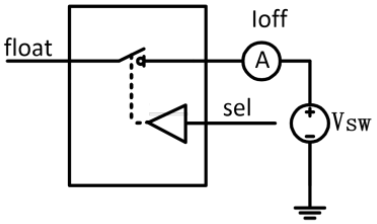


Figure7. off leakage(I_{OZ})

Note: each switch port is tested separately

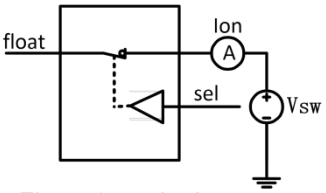


Figure8. on leakage

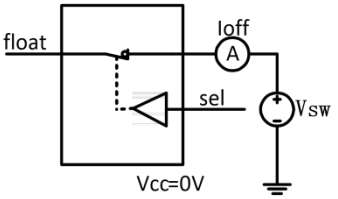


Figure9. power off leakage(I_{OFF})

Note: each switch port is tested separately

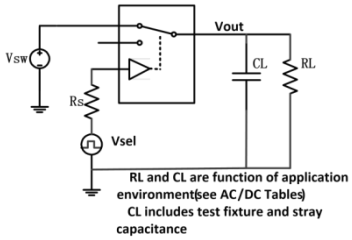


Figure10. Test Circuit Load

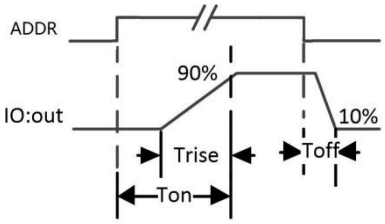


Figure11-A. Turn on/off Waveforms under Manual Mode(Audio switch)

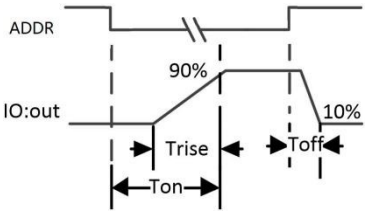


Figure11-B. Turn on/off Waveforms under Manual Mode (USB switch)

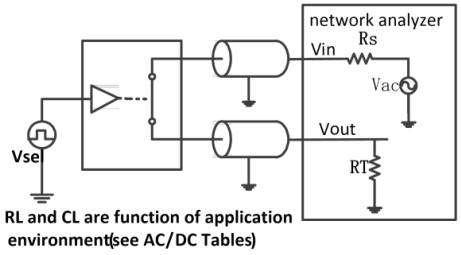


Figure12. Bandwidth

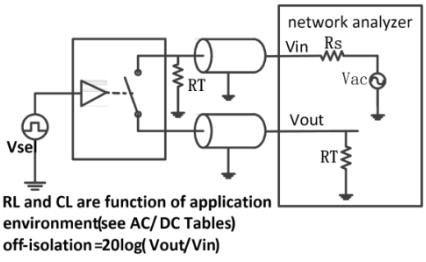


Figure13. Channel Off Isolation

Test Diagrams(Continued)

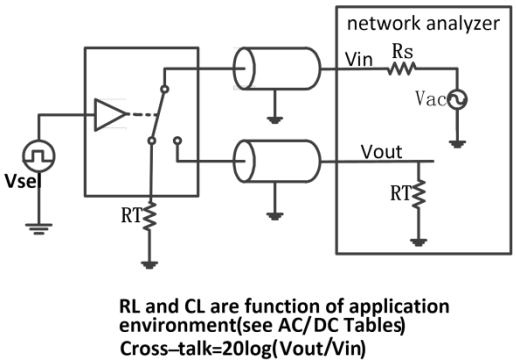


Figure14. Adjacent Channel Crosstalk

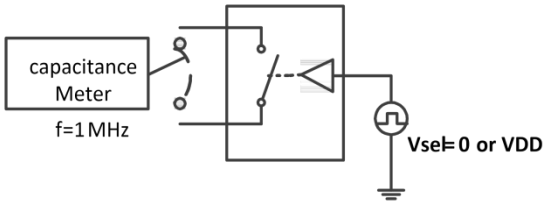


Figure15. Adjacent Off Capacitance

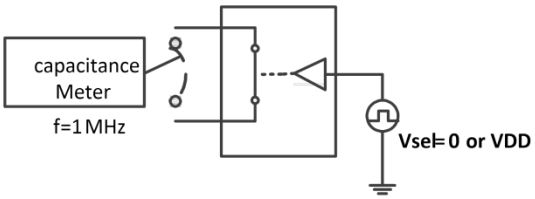


Figure16. Channel On Capacitance

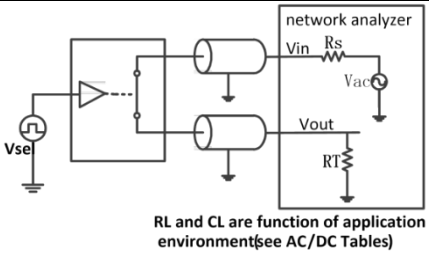
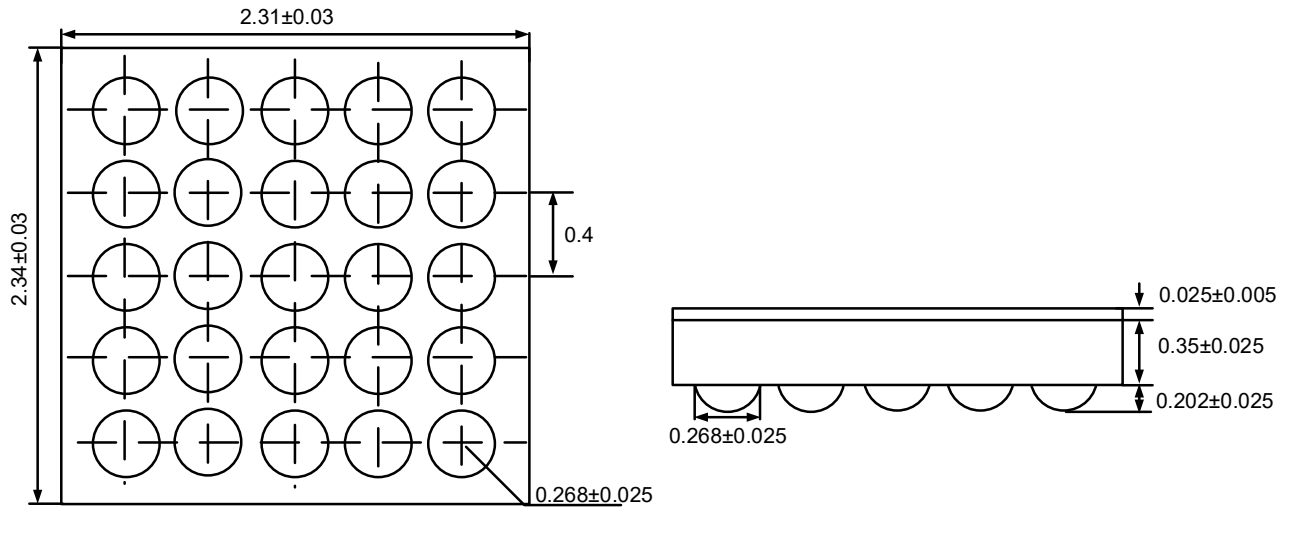
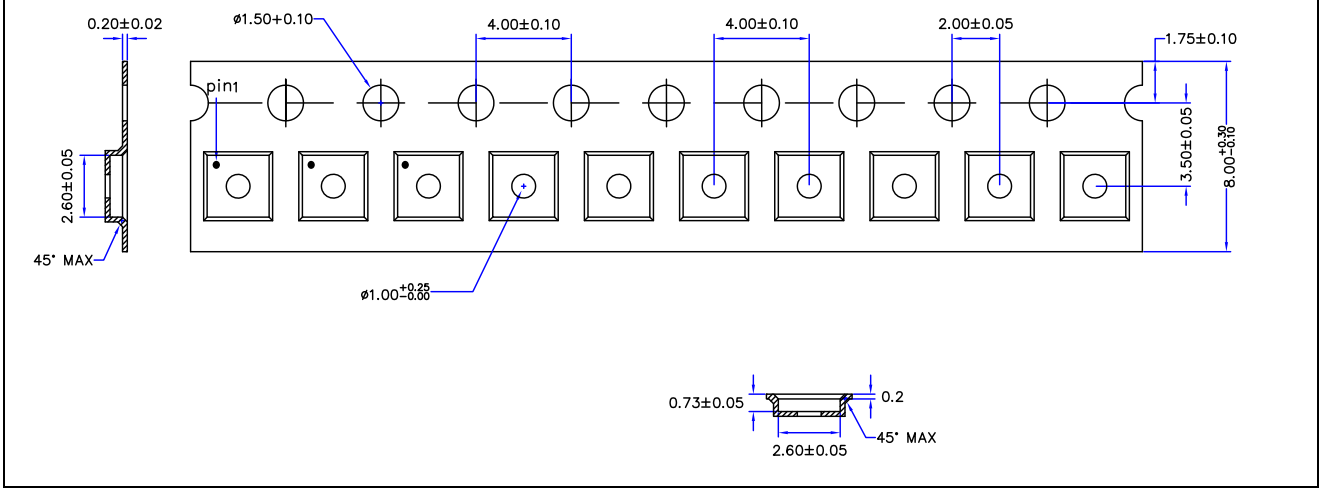


Figure17. Total Harmonic Distortion(THD+N)

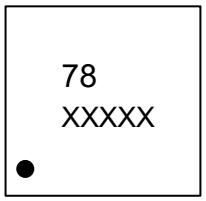
Package Dimension



Tape Information



Marking Information



78 - Part Number

XXXXX - Tracking Number

Note：X (Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2021-03-05	Preliminary Version	Luhao	Luhao	Zhujl
1.1	2023-03-22	Add Marking Information	Yinp	Luhao	Zhujl