# High-Voltage Protect USB 2.0 DPDT Switch

## General Description

ET7429 is a Hi-Speed (up to 480Mbps) USB dual SPDT switch with over-voltage protection. It operates over a 2.7V to 5.5V supply range with over-voltage fault protection up to 20V. The device features independent control bits for each switch pair and an on/off enable ( $\overline{EN}$ ) for shutdown mode. Additional features include low switch on resistance and capacitance along with a fault flag ( $\overline{FLAG}$ ) to alert the system processor to over-voltage fault events.

ET7429 has low power consumption and is available in an ultra-small CSP12 1.15mm×1.55mm package making it an ideal solution for USB interface switching and protection in mobile applications.

## Features

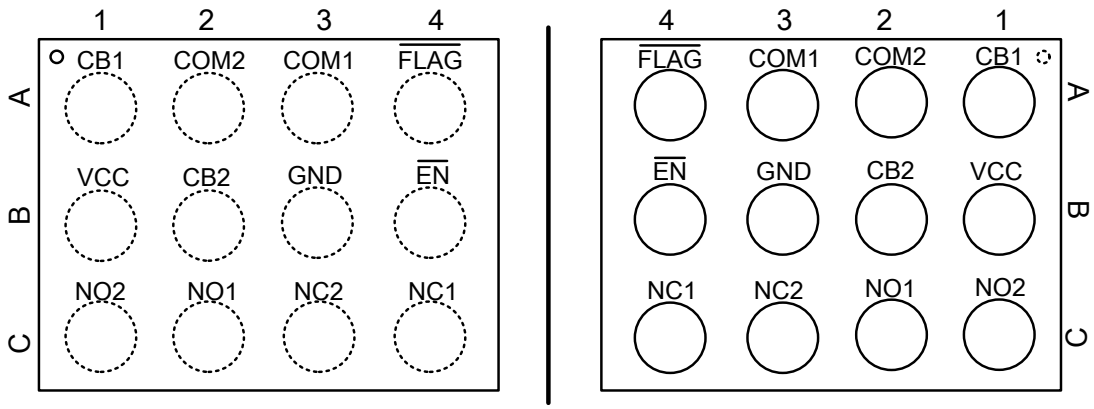
- Operating Range from 2.7V to 5.5V
- For USB D+/D- Hi-Speed or SBU 1/2 Signals
- Reverse Blocking Back-to-back MOSFETs
- >1GHz -3dB Bandwidth
- Low 6Ω Switch On-Resistance
- Typical 6.0pF Switch On-Capacitance
- Over-voltage Protection Up to +22V
- $\overline{FLAG}$ Open Drain Output Over-voltage Indicator
- $\overline{EN}$ to Disable Switch Output
- -40°C to +85°C Temperature Range
- MSL1
- Part No. and Package

| Part No. | Package |
|---|---|
| ET7429 | CSP12(1.15mm × 1.55mm, Ball pitch = 0.4mm) |

## Applications

- Smartphones
- USB Type-C
- Mobile Internet Devices
- Tablet Computers
- Peripheral

## Pin Configuration



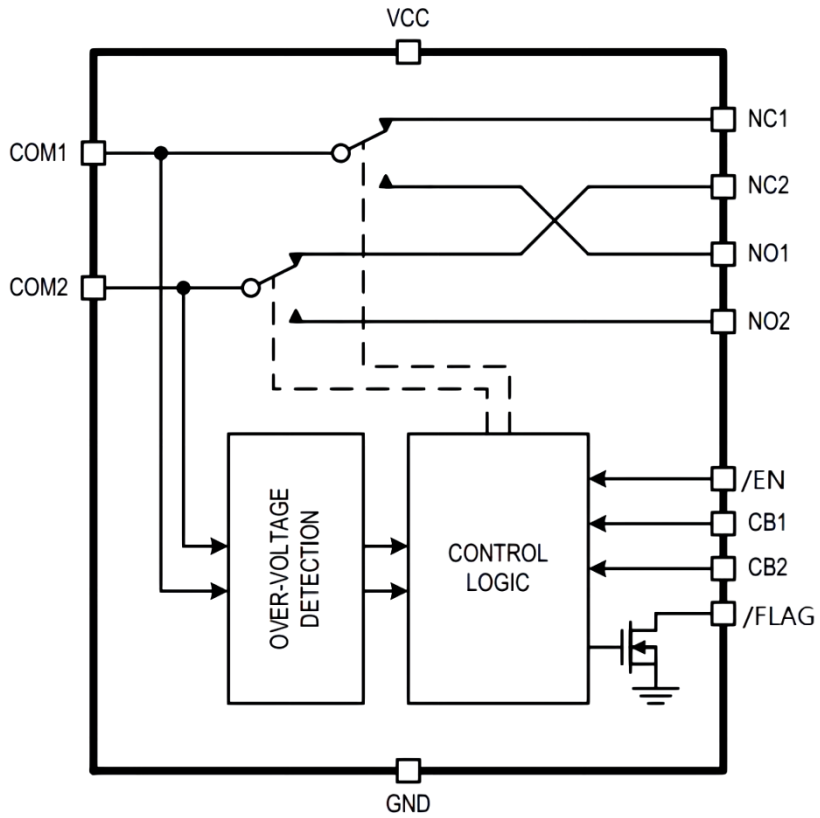

## Pin Function

| Pin | Name | Description |
|---|---|---|
| A1 | CB1 | Digital Control Input 1 |
| A2 | COM2 | Common Terminal for I/O Switch 1 (Connect to D+, D-, SBU1 or SBU2) |
| A3 | COM1 | Common Terminal for I/O Switch 2 (Connect to D+, D-, SBU1 or SBU2) |
| A4 | $\overline{FLAG}$ | Active low fault flag output signal to alert fault event |
| B1 | VCC | Input Supply Voltage input pin |
| B2 | CB2 | Digital Control Input 2 |
| B3 | GND | Ground pin |
| B4 | $\overline{EN}$ | Active low enable input pin.Drive EN to a logic high level to disable the device and place switches to a high impedance state. |
| C1 | NO2 | Normally Open Terminal for USB I/O Switch 2 |
| C2 | NO1 | Normally Open Terminal for USB I/O Switch 1 |
| C3 | NC2 | Normally Open Terminal for USB I/O Switch 2 |
| C4 | NC1 | Normally Open Terminal for USB I/O Switch 1 |

## Truth Table

| $\overline{EN}$ | CB1 | CB2 | COM1 Connection | COM2 Connection |
|---|---|---|---|---|
| H | × | × | High-Z | High-Z |
| L | L | L | COM1 to NC1 | COM2 to NC2 |
| L | L | H | COM1 to NC1 | COM2 to NO2 |
| L | H | L | COM1 to NO1 | COM2 to NC2 |
| L | H | H | COM1 to NO1 | COM2 to NO2 |

## Block Diagram




Functional Block Diagram

## Absolute Maximum Ratings

| Symbol | Pins | Parameter | | Value | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | VCC | Positive DC Supply Voltage | | -0.5 to +6.0 | V |
| $V_{IS}$ | NC1/NO1,NC2/NO2 | Analog Signal Voltage | | -0.3 to +6.0 | V |
| | COM1, COM2 | | | -0.5 to +20 | |
| $V_{IN}$ | CB1、CB2、$\overline{EN}$ | Control Input Voltage | | -0.5 to +6.0 | V |
| $T_{STG}$ | | Storage Temperature | | -65 to +150 | ℃ |
| ESD | All Pins | Electrostatic Discharge Capability | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | ±2.5 | KV |
| | | | Charged Device Model, JESD22-C101 | ±2.0 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Recommended Operating Conditions

| Symbol | Pins | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | VCC | Positive DC Supply Voltage | 2.7 | 5.5 | V |
| $V_{I/O}$ | NC1, NO1, NC2, NO2 | Analog Input/output Voltage | 0 | 3.6 | V |
| | COM1, COM2 | | 0 | 18 | |
| $V_{IN}$ | $\overline{EN}$ , CB1, CB2 | Digital Select Input Voltage | 0 | 5.5 | V |
| $V_O$ | $\overline{FLAG}$ | Digital Output Voltage | 0 | 5.5 | V |
| $I_{I/O}$ | COM1,COM2, NC1,NO1,NC2,NO2 | Analog Input/output Port Continuous Current | -50 | 50 | mA |
| $I_{OL}$ | | Digital Output Current | | 1 | mA |
| $T_A$ | | Operating Temperature Range | -40 | +85 | ˚C |

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

## DC Electrical Characteristics

**Digital Characteristics** (Typical: $T_A$ = 25°C, $V_{CC}$ = 3.3 V)

| Symbol | Pin Name | Parameter | Test Conditions | $V_{CC}$(V) | -40˚C to +85˚C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | $\overline{EN}$, CB1, CB2 | Control Input High Voltage | | 2.7~5.5 | 1.2 | - | - | V |
| $V_{IL}$ | $\overline{EN}$, CB1, CB2 | Control Input Low Voltage | | 2.7~5.5 | - | | 0.4 | V |
| $V_{OL}$ | $\overline{FLAG}$ | Output Logic Low | $I_{OL}$=1mA | 2.7~5.5 | | | 0.5 | V |
| $I_{IH}$ | $\overline{EN}$, CB1, CB2 | Input High leakage Current | $\overline{EN}$, CB1, CB2=1.8V | 2.7~5.5 | -1 | 0.5 | 5 | uA |
| $I_{IL}$ | $\overline{EN}$, CB1, CB2 | Input Low Leakage Current | $\overline{EN}$, CB1, CB2=0V | 2.7~5.5 | -1 | ±0.1 | 5 | uA |
| $R_{PD}$ | $\overline{EN}$, CB1,CB2 | Internal Pull-down Resistor on Digital Input Pins | | | | 5 | | MΩ |

**Supply and Leakage Current Characteristics** (Typical: $T_A$ = 25°C, $V_{CC}$ = 3.3 V)

| Symbol | Pin Name | Parameter | Test Conditions | $V_{CC}$(V) | -40℃ to +85℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{CC}$ | $V_{CC}$ | Active Supply Current | $\overline{EN}$ =0V<br>CB1,CB2=0V or $V_{CC}$<br>0v<$V_{I/O}$<3.6V | 5.5 | | 30 | | uA |
| $I_{CC\_PD}$ | $V_{CC}$ | Standby Powered Down Supply Current | $\overline{EN}$ =$V_{CC}$<br>CB1,CB2=0V or $V_{CC}$<br>or CB1,CB2= $V_{CC}$ | 5.5 | | 2.2 | 10 | uA |
| $I_{ON}$ | $V_{I/O}$ | ON Leakage Current | $V_{COMn}$=0V or 3.6v<br>$V_{Nn}$=high-Z, Figure 3 | | | 1 | | uA |
| $I_{OFF}$ | $V_{I/O}$ | I/O pin OFF Leakage Current | $V_{COMn}$=0V or 3.6V<br>$V_{CC}$=2.7V to 5.5V<br>$V_{Nn}$=3.6V or 0V, Figure 2 | | | 1 | | uA |
| | | | $V_{COMn}$=20V,<br>$V_{CC}$=2.7V to 5.5V<br>$V_{Nn}$= 0V, Figure 2 | | | 15 | | |

**Protection Characteristics**

| Symbol | Parameter | Test Conditions | -40℃ to +85℃ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OVP\_TH}$ | OVP positive threshold | | 4.5 | 4.8 | 5.2 | V |
| $V_{OVP\_HYST}$ | OVP threshold hysteresis | | | 250 | | mV |
| $V_{CLAMP\_V}$ | Maximum voltage to appear on NCn and Non pins during OVP scenario(1) | $V_{COMn}$=0 to 18V<br>$t_{RISE}$ and $t_{FALL}$(10% to 90%)=100ns<br>$R_L$=50Ω, Switch on or off, $\overline{EN}$ =0V | 0 | | 9.0 | V |
| $t_{EN\_OVP}$ | OVP enable time(1) | $R_{PU}$=10KΩ to $V_{CC}$ ( $\overline{FLAG}$ )<br>$C_L$=35pF , Figure 9 | | 60 | | ns |
| $t_{REC\_OVP}$ | OVP recovery time(1) | $R_{PU}$=10KΩ to $V_{CC}$ ( $\overline{FLAG}$ )<br>$C_L$=35pF , Figure 9 | | 0.4 | | us |
| $t_{OFF\_RES}$ | Switch turn-off response time(1) | $R_L$=50Ω, No $C_L$ , $V_{COM}$ > $V_{OVP\_TH}$<br>to $V_{NX}$ stop rising | | 60 | | ns |

**High Speed on Resistance** (Typical: $T_A$ = 25°C, $V_{CC}$ = 3.3 V)

| Symbol | Parameter | Test Conditions | $V_{CC}$(V) | -40℃ to +85℃ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $R_{ON}$ | On-Resistance | $V_{IO}$ = 0.4V, $I_{SINK}$ =8mA,Figure 1 | 3.3 | | 6.0 | 9.0 | Ω |
| $R_{FLAT}$ | On-Resistance Flatness | $V_{I/O}$ = 0V to 0.4V,<br>$I_{SINK}$ =8mA, Figure 1 | 3.3 | | 0.05 | 0.4 | Ω |
| △$R_{ON}$ | On-Resistance Match between Channels | $V_{I/O}$ = 0.4V, $I_{SINK}$ =8mA, Figure 1 | 3.3 | | 0.1 | 0.3 | Ω |

## AC Electrical Characteristics

**Timing/Frequency** (Typical: $T_A$ = 25°C, $V_{CC}$ = 3.3V, $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz)

| Symbol | Parameter | Test Conditions | $V_{CC}$(V) | -40℃ to +85℃ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{SWITCH}$ | Switch Time between Channel (CB1,CB2 to Output) | $V_{COMn}$=0.8V, $R_L$=50Ω $C_L$=5pF, Figure 4 | 2.7~5.5 | | 5.5 | | us |
| $t_{ON}$ | Device turn on time ($\overline{EN}$ to Output) | $V_{COMn}$=0.8V, $R_L$=50Ω $C_L$=5pF, Figure 5 | 2.7~5.5 | | 120 | 250 | us |
| $t_{OFF}$ | Device Turn Off Time(1) ($\overline{EN}$ to Output) | $V_{COMn}$=0.8V, $R_L$=50Ω $C_L$=5pF, Figure 5 | 2.7~5.5 | | 0.015 | 0.5 | us |
| $t_{SK(P)}$ | Skew of Opposite Transitions of Same Output(1) (Between COM1 and COM2) | $V_{COMn}$=0.4V, $R_L$=50Ω $C_L$=1pF, Figure 11 | 2.7~5.5 | | 9 | 50 | ps |
| $t_{PD}$ | Propagation Delay(1) | $V_{COMn}$=0.4V, $R_L$=50Ω $C_L$=5pF, Figure 10 | 2.7~5.5 | | 130 | 180 | ps |
| BW | -3dB Bandwidth(1) | Switch on, $R_L$ =50Ω, Figure 8 | 4.2 | | 1.0 | | GHz |

**Isolation** (Typical: $T_A$ = 25°C, $V_{CC}$ = 3.3V, $R_L$ = 50Ω, $C_L$ = 5pF, f = 1 MHz)

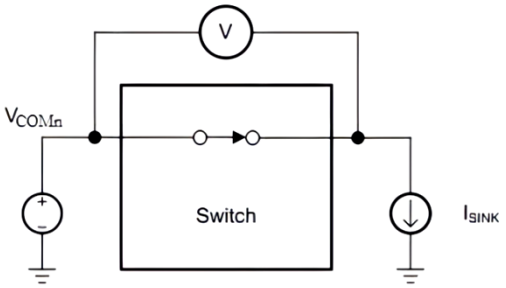
| Symbol | Pin Name | Parameter | Test Conditions | $V_{CC}$(V) | -40℃ to +85℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $O_{IRR}$ | NO/NC | OFF-Isolation(1) (Figure 6) | Switch off, $R_L$=50Ω $C_L$=5pF, f=100kHz | 2.7~5.5 | | -90 | | dB |
| | | | Switch off, $R_L$=50Ω $C_L$=5pF, f=240MHz | 2.7~5.5 | | -28 | | dB |
| $X_{TALK}$ | COM1/ COM2 | Non-Adjacent Channel Crosstalk(1) | Switch on, $R_L$=50Ω $C_L$=5pF, f=100kHz Figure 7 | 2.7~5.5 | | -90 | | dB |

**Capacitance** (Typical: $T_A$ = 25°C, $V_{CC}$ = 3.3 V)

| Symbol | Pin Name | Parameter | Test Conditions | $V_{CC}$(V) | -40℃ to +85℃ | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $C_I$ | $\overline{EN}$ CB1, CB2 | Digital Input Capacitance(1) | f=1MHz | 2.7-5.5 | | 3.4 | | pF |
| $C_{ON}$ | I/O | I/O Pins ON Capacitance(1) | $\overline{EN}$ =0V f=1MHz | 2.7-5.5 | | 6.0 | | pF |
| $C_{OFF}$ | COM1 COM2 | COM1 COM2 Off Capacitance(1) | Switch off $\overline{EN}$ =$V_{CC}$ ,f=1MHz | 2.7-5.5 | | 5.5 | | pF |
| | NC1 NO1 NC2 NO2 | NC1 NO1 NC2 NO2 Off Capacitance(1) | Switch off $\overline{EN}$ =$V_{CC}$ ,f=1MHz | 2.7-5.5 | | 2.2 | | pF |

***Note1***：Guaranteed by design.

## Test Reference Circuit




Channel ON, $R_{ON}=V/I_{SINK}$

Figure 1. ON-State Resistance ($R_{ON}$)

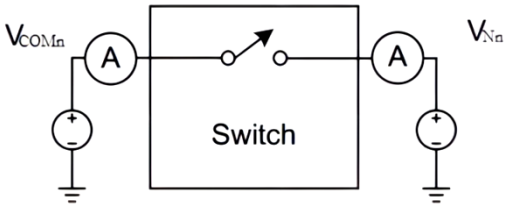



Figure 2. Off Leakage

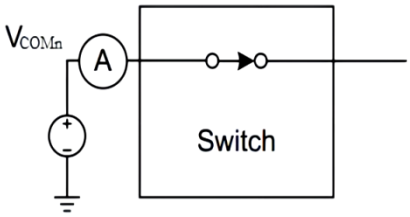
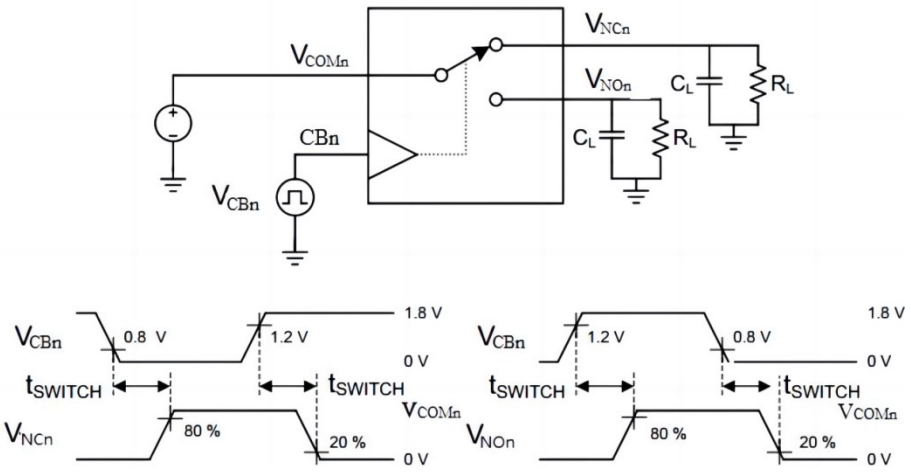


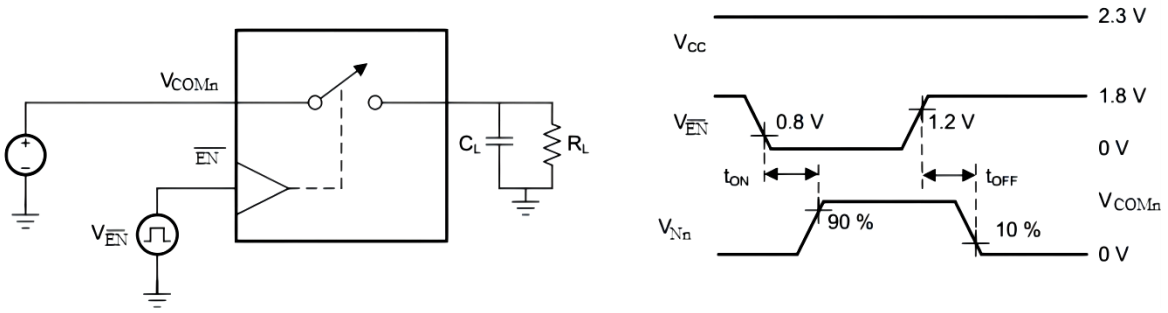

Figure 3. On Leakage




(1) All input pulses are supplied by generators having the following characteristics:
$P_{RR}$≤10MHz,$Z_O$=50Ω, $t_r$<500ps, $t_f$<500ps

(2) $C_L$ include probe and jig capacitance

Figure 4. $t_{SWITCH}$ Timing




(1) All input pulses are supplied by generators having the following characteristics:
$P_{RR}$≤10MHz,$Z_O$=50Ω, $t_r$<500ps, $t_f$<500ps

(2) $C_L$ include probe and jig capacitance

Figure 5. $t_{ON}$ $t_{OFF}$ for /EN

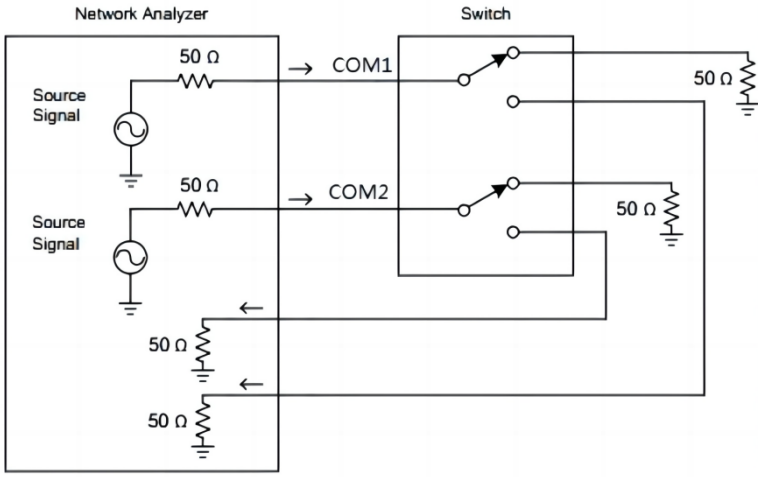



Figure 6. Off Isolation

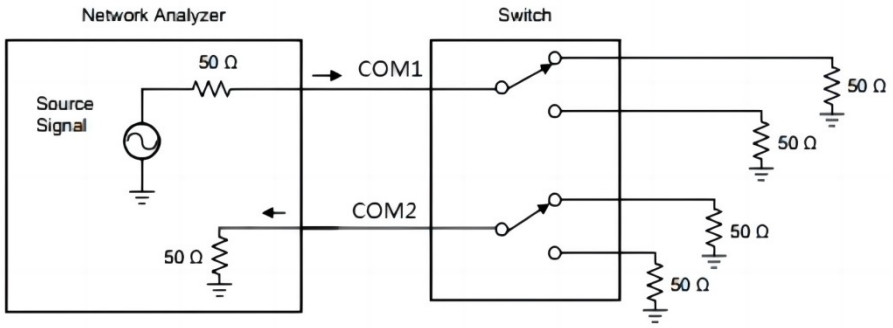



Figure 7. Cross Talk

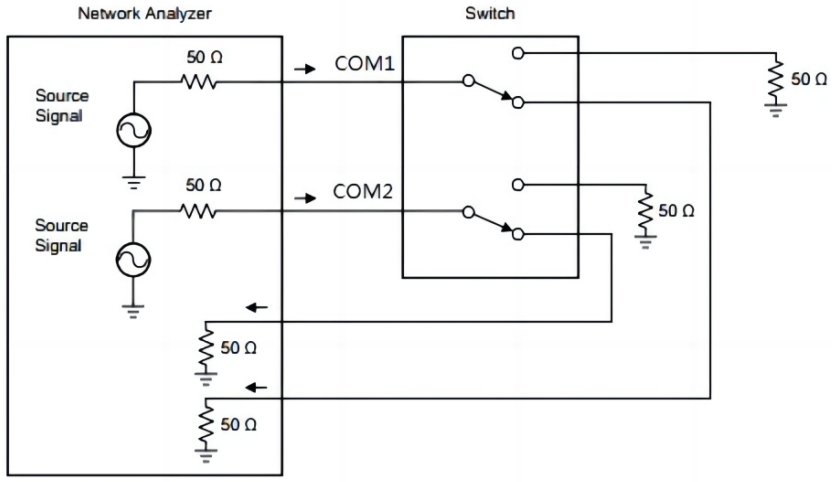



Figure 8. BW

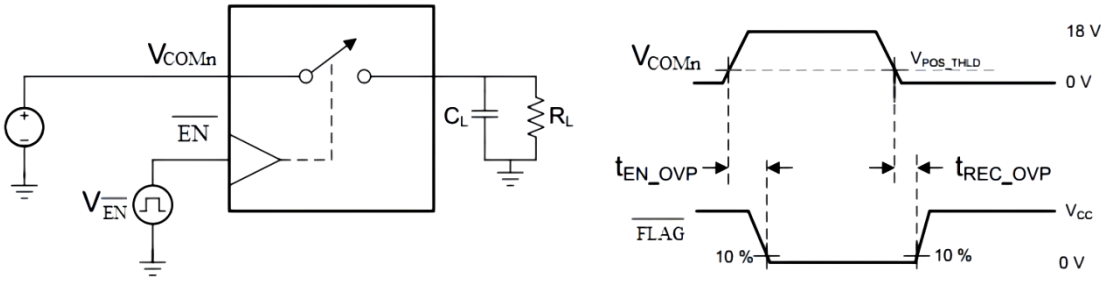
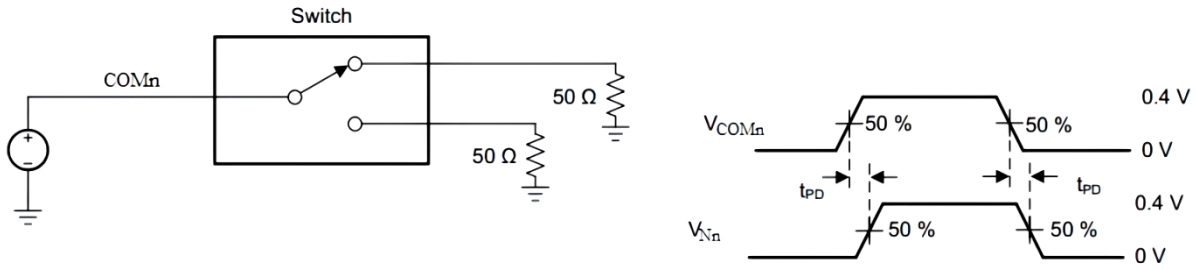


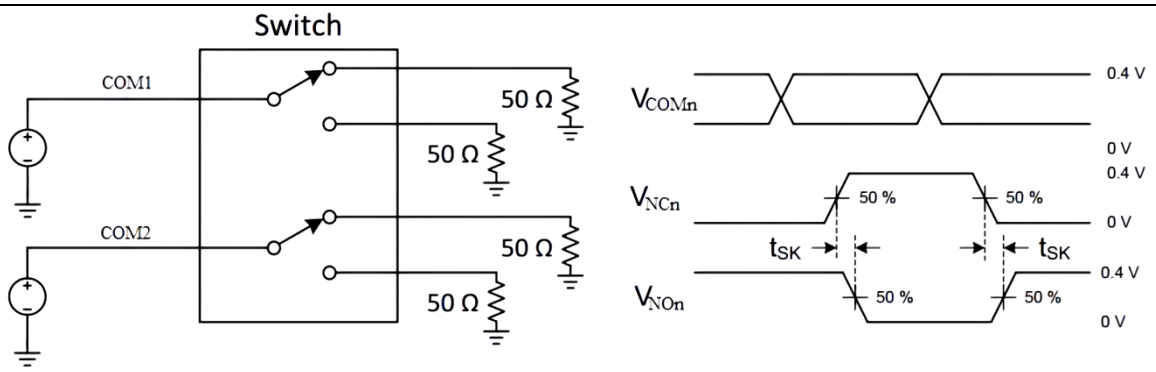

Figure 9. $t_{EN\_OVP}$ and $t_{DIS\_OVP}$ Timing Diagram




(1) All input pulses are supplied by generators having the following characteristics:
$P_{RR}$≤10MHz,$Z_O$=50Ω, $t_r$<500ps, $t_f$<500ps

(2) $C_L$ include probe and jig capacitance

Figure 10. $t_{PD}$



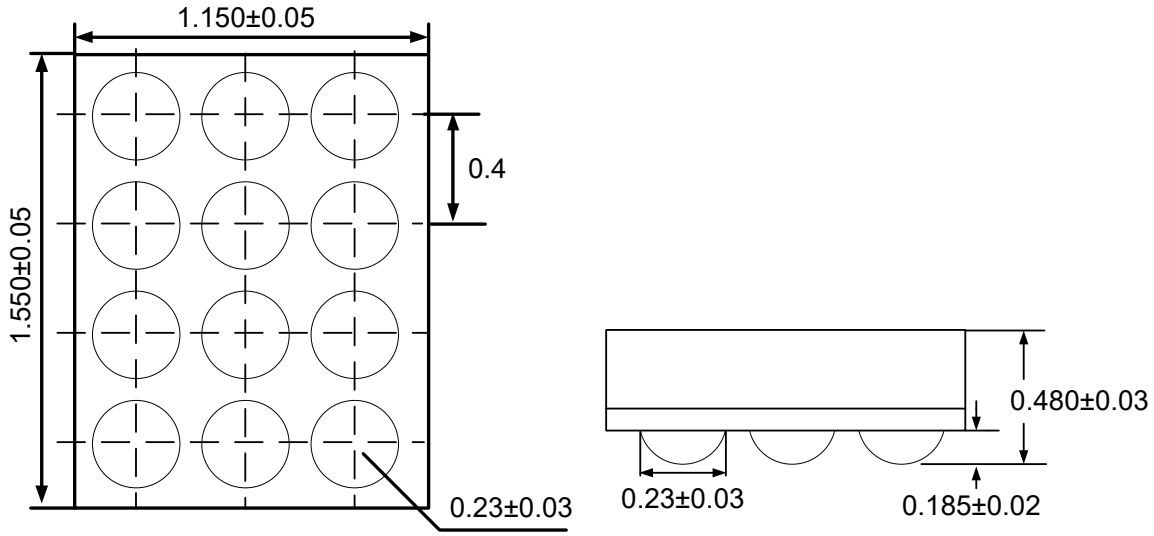

(1) All input pulses are supplied by generators having the following characteristics:
$P_{RR}$≤10MHz,$Z_O$=50Ω, $t_r$<500ps, $t_f$<500ps

(2) $C_L$ include probe and jig capacitance

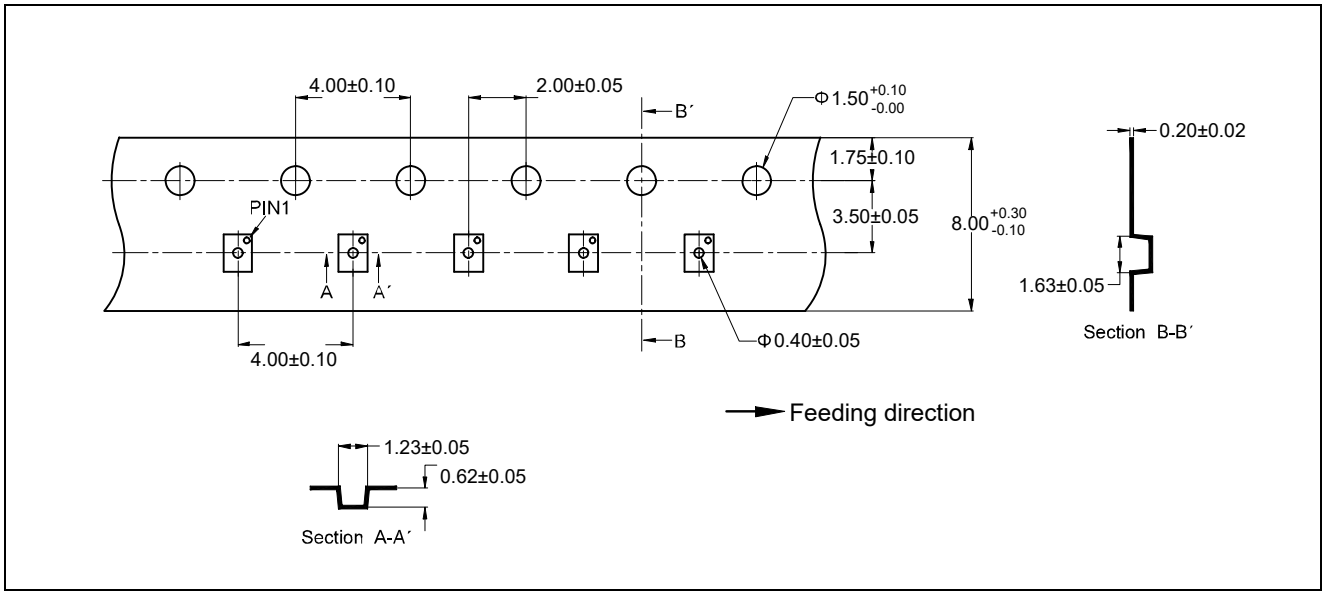
Figure 11. $t_{SK}$

## Package Dimension

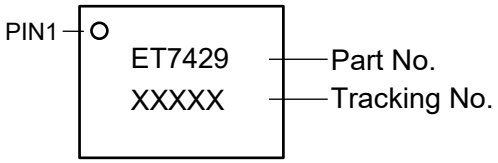
CSP12



## Tape




## Marking




## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 1.0 | 2019-12-20 | Released Version | Luh | Luh | Zhujl |
| 1.1 | 2020-03-13 | Documents check and formalize | Shib | Shib | Liujy |
| 1.2 | 2020-03-17 | Add MSL level | Luh | Luh | Zhujl |
| 1.3 | 2020-05-11 | Update tape information | Luh | Luh | Liujy |
| 1.4 | 2023-4-2 | Update Typeset | Shibo | Luh | Liujy |
| 1.5 | 2023-8-15 | Package to lossless format | Shibo | | |
| 1.6 | 2023-9-1 | Correct packaging height | Shibo | Luh | Liujy |