Low Voltage 1.0Ω Max Dual SP3T Switch

With Break Before Make Feature

General Description

The ET3856 is a high-speed CMOS low voltage dual analog SP3T (Single Pole Triple Throw) switch or Dual 3:1 Multiplexer/Demultiplexer Switch fabricated in silicon gate CMOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

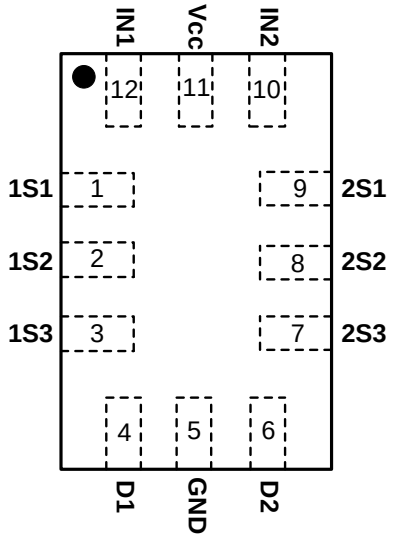
The device offers very low ON-Resistance (<1.0Ω) at V_{CC} = 4.3V. The disabling and enabling of switches are done by setting the IN1 and IN2 control pins. Additional key features are fast switching speed, and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Features

- High Speed:
  - t_{PD} = 0.3ns (TYP.) @ V_{CC} = 3.0V
  - t_{PD} = 0.4ns (TYP.) @ V_{CC} = 2.3V
- Ultra Low Power Dissipation:
  - I_{CC} = 0.2μA (MAX.) @ T_A = 85°C
- Low “ON” Resistance V_{IN} = 0V:
  - R_{ON} = 1.1Ω(MAX. T_A = 25ºC) @ V_{CC}=4.3V
  - R_{ON} = 1.5Ω(MAX. T_A = 25ºC) @ V_{CC}=3.0V
  - R_{ON} = 1.8Ω(MAX. T_A = 25ºC) @ V_{CC}=2.3V
- Wide Operating Voltage Range:
  - V_{CC} = 1.65V to 4.3V Single Supply
- 4.3V Tolerant And 1.8V Compatible Threshold On Digital Control Input at V_{CC} = 2.3 to 4.3V
- Latch-Up Performance Exceeds 300mA
- ESD Performance (Analog Channel. Vs. GND): HBM >2kV
- Part No. and package

Part No.	Package	MSL
ET3856	QFN12L (2.2 mm×1.4 mm)	Level 1

Pin Configuration

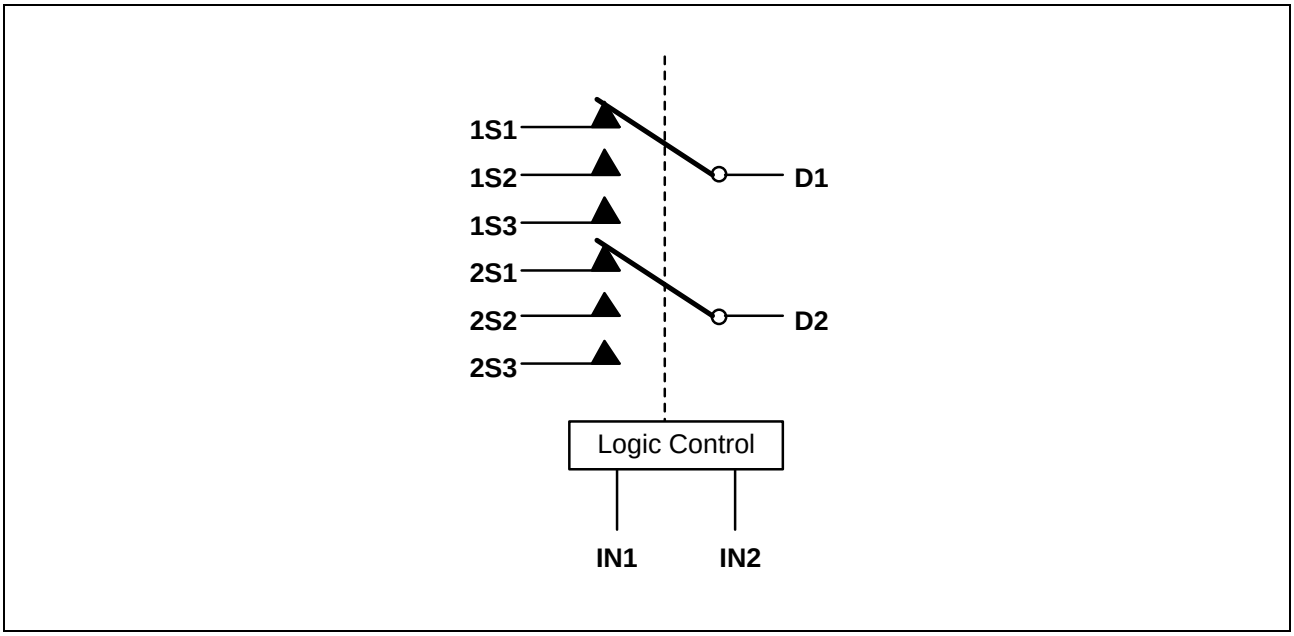


Top View

Pin Function

Pin No.	Symbol	Function
1	1S1	Independent Channels
2	1S2	Independent Channels
3	1S3	Independent Channels
4	D1	Common Channels
5	GND	Ground (0V)
6	D2	Common Channels
7	2S3	Independent Channels
8	2S2	Independent Channels
9	2S1	Independent Channels
10	IN2	Controls
11	V_{CC}	Positive Supply Voltage
12	IN1	Controls

Analog Symbol



Truth Table

IN1	IN2	Switch State
L	L	High-Impedance
L	H	D1-1S1, D2-2S1
H	L	D1-1S2, D2-2S2
H	H	D1-1S3, D2-2S3

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 5.5	V
V_I	DC Input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC Control Input Voltage	-0.5 to 5.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC Input Diode Current on Control Pin (V_{IN} < 0V)	-50	mA
I_{IK}	DC Input Diode Current (V_{IN} < 0V)	±50	mA
I_{OK}	DC Output Diode Current	±20	mA
I_O	DC Output Current	±150	mA
I_{OP}	DC Output Current Peak (pulse at 1ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	±100	mA
P_D	Power Dissipation at T_A = 70ºC (1)	0.25	W
T_{STG}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Note1: Derate above 70ºC by 18.5mW/ºC

Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		1.4 to 4.3	V
V_I	Input Voltage		0 to V_{CC}	V
V_{IC}	Control Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{OP}	Operating Temperature		-40 to 85	°C
dt/dv	Input rise and Fall Time Control Input	V_{CC} =1.65V to 2.7V	0 to 20	ns/V
		V_{CC} =3.0 to 4.3V	0 to 10	

DC Electrical Characteristics

Symbol	Parameter	Test Condition		T_A = 25°C			Unit
		V_{CC} (V)		Min	Typ	Max	
V_{IH}	High Level Input Voltage	1.65-1.95		0.65V_{CC}			V
		2.3 - 2.5		1.4			
		2.7 - 3.0		1.4			
		3.3 - 4.3		1.7			
V_{IL}	Low Level Input Voltage	1.65-1.95				0.40	V
		2.3 - 2.5				0.50	
		2.7 - 3.0				0.50	
		3.3 - 4.3				0.50	
R_{ON}	Switch ON Resistance	4.3	V_S=0V to V_{CC} I_S=100mA		0.6	1.1	Ω
		3.0			1.3	1.5	
		2.7			1.5	1.8	
		2.3			2.0	2.2	
		1.8			2.5	3.0	
		1.65			3.3	4.0	
ΔR_{ON}	ON Resistance Match between channels	2.7	V_S @ R_{ON} Max I_S=100mA		0.01		Ω
R_{FLAT}	ON Resistance FLATNESS(2) (3)	2.7	V_S=0V to V_{CC} I_S=100mA		0.22	0.35	Ω
I_{OFF}	OFF State Leakage Current (nSN),(Dn)	4.3	V_S=0.3 or 4V			±0.5	μA
I_{IN}	Input Leakage Current	0 - 4.3	V_{IN}=0 to 4.3V			±0.5	μA
I_{CC}	Quiescent Supply Current	1.65 - 4.3	V_{IN}=V_{CC} or GND			±0.5	μA
I_{CCLV}	Quiescent Supply Current Low Voltage Driving	4.3	V_{IN1},V_{IN2} = 1.65V		±37	±70	μA
			V_{IN1},V_{IN2} = 1.80V		±33	±60	
			V_{IN1},V_{IN2} = 2.60V		±12	±20	

Note2: ΔR_{ON} = max |mSN-nSN|, where m = 1 and n = 2, N = 1..3

Note3: Flatness is defined as the difference between the maximum and minimum value of ON-resistance as measured over the specified analog signal ranges.

AC Electrical Characteristics (C_L = 35pF, R_L = 50Ω, tr = tf ≤ 5ns)

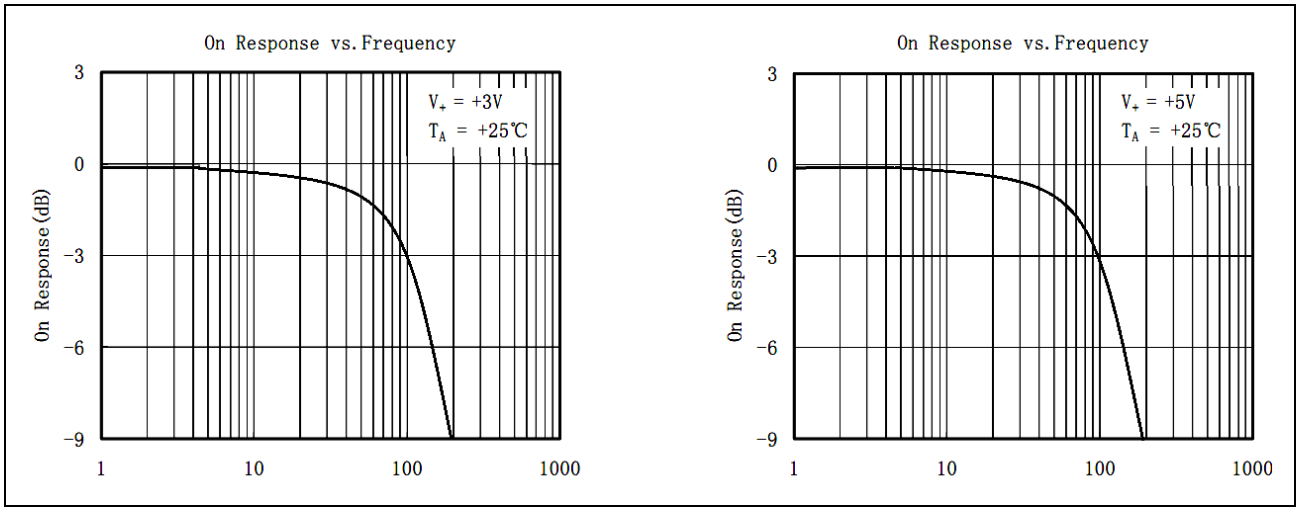
Symbol	Parameter	Test Condition		T_A = 25°C			Unit
		V_{CC} (V)		Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay	1.65-1.95			0.45		ns
		2.3 - 2.7			0.40		
		3.0 - 3.3			0.30		
		3.6 - 4.3			0.30		
t_{ON}	Turn-On time	1.65-1.95	V_S=0.8V		56		ns
		2.3-2.7	V_S=1.5V		33	50	
		3.0-3.3			21	40	
		3.6-4.3			19	40	
t_{OFF}	Turn-Off time	1.65-1.95	V_S=0.8V		24		ns
		2.3-2.7	V_S=1.5V		17	25	
		3.0-3.3			14	20	
		3.6-4.3			12	20	
t_D	Break Before Make Time Delay	1.65-1.95	V_S=0.8V	10	31		ns
		2.3-2.7	V_S=1.5V	10	22	40	
		3.0-3.3		10	18	30	
		3.6-4.3		10	7	25	
Q	Charge Injection	1.65-1.95	C_L=100pF		25		pC
		2.3-2.7	R_L=1MΩ		35		
		3.0-3.3	V_{GEN}=0V		40		
		3.6-4.3	R_{GEN}=0Ω		55		

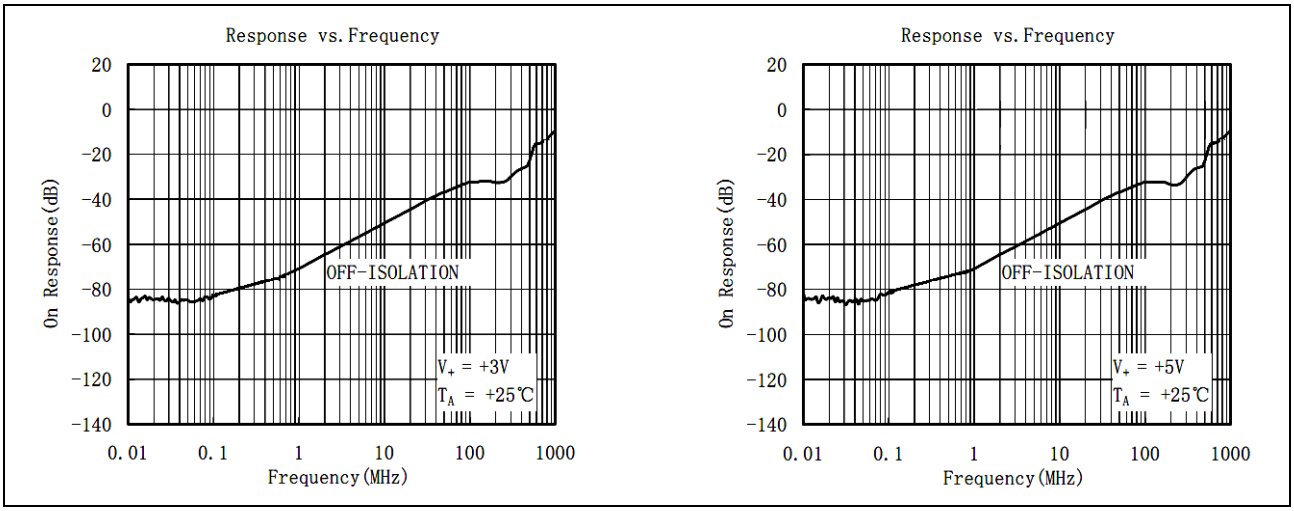
Analog Switch Characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test Condition		T_A = 25°C			Unit
		V_{CC} (V)		Min.	Typ	Max.	
O_{IRR}	Off Isolation (4)	1.65-4.3	V_S=1V_{RMS} f=100kHz		-82		dB
X_{TALK}	Crosstalk	1.6-4.3	V_S=1V_{RMS} f=100kHz		-84		dB
THD	Total Harmonic Distortion	2.3-4.3	R_L=600Ω V_{IN}=2V_{PP} f=20Hz to 20kHz		0.03		%
BW	-3dB、Bandwidth	1.65-4.3	R_L=50Ω		50		MHz
C_{IN}	Control Pin Input Capacitance				5		pF
$C_{Sn(OFF)}$	Sn Port OFF Capacitance	3.3	f = 1MHz		23		
$C_{Sn(ON)}$	Sn Port ON Capacitance	3.3	f = 1MHz		70		
C_D	D Port Capacitance when Switch is Enabled	3.3	f = 1MHz		70		

Note4: OFF Isolation = 20Log_{10} (V_D/V_S), V_D = output, V_S = input at off switch

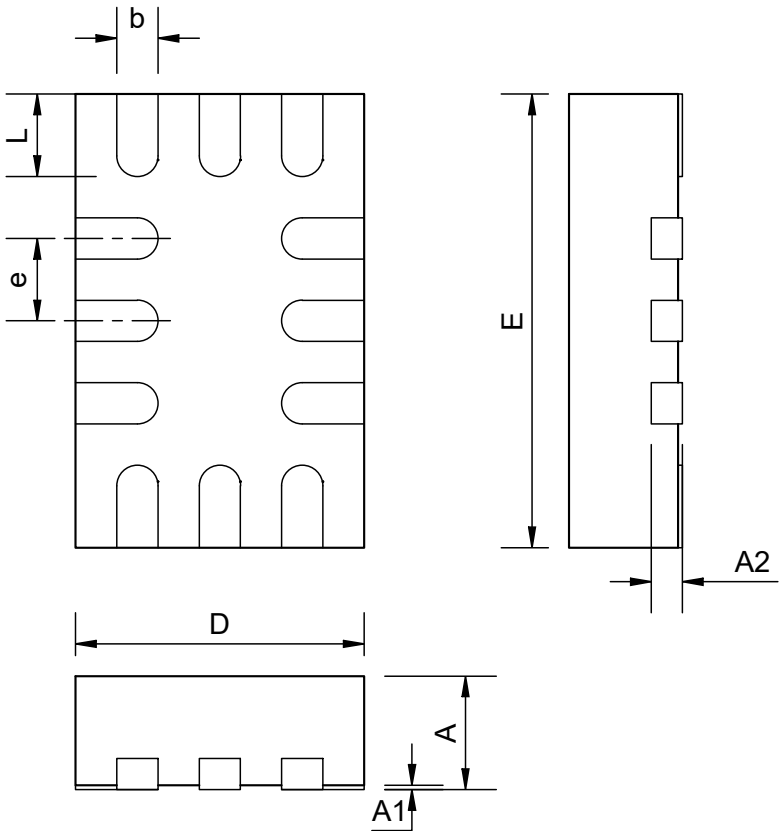
Typical Performance Characteristics





Package Dimension

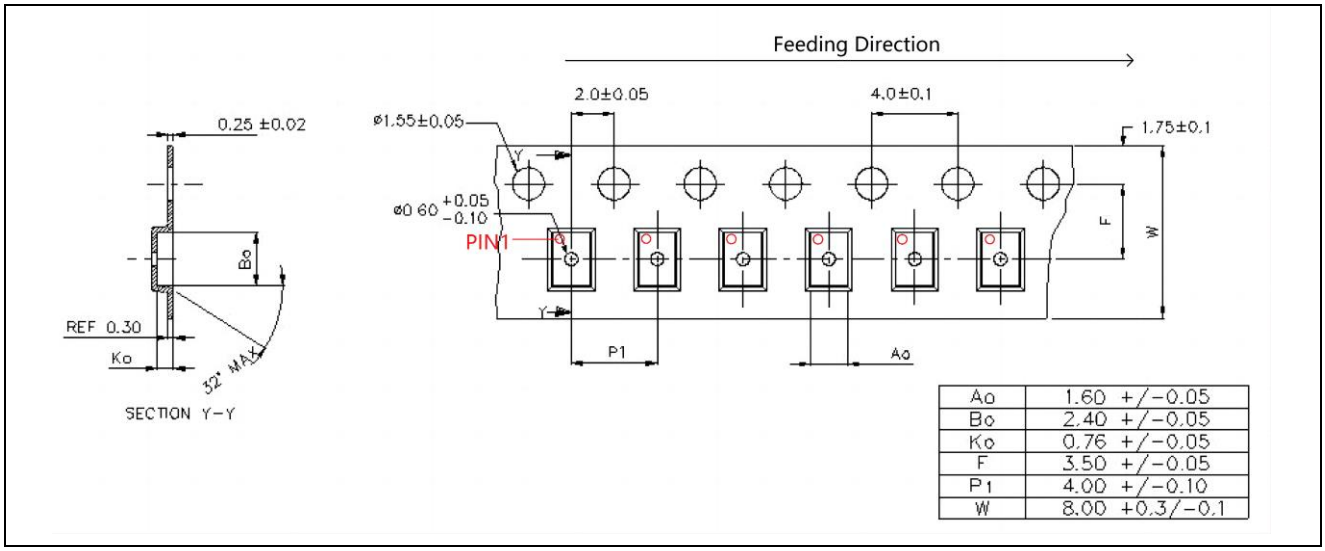
QFN12L



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	0	0.02	0.05
A2		0.15REF	
b	0.15	0.2	0.25
D	1.35	1.4	1.45
E	2.15	2.2	2.25
e		0.4BSC	
L	0.3	0.4	0.5

Tape



Ao	1.60 +/−0.05
Bo	2.40 +/−0.05
Ko	0.76 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-09-09	Original Version	Liu Xiao Min	Liu Xiao Min	Zhu Jun Li
1.1	2017-04-28	Updated some parameters	Liu Xiao Min	Liu Xiao Min	Zhu Jun Li
1.2	2017-05-08	Updated V_{IH} & I_{CCLV} spec	Liu Xiao Min	Liu Xiao Min	Zhu Jun Li
1.3	2023-02-01	Update Typeset	Qinpl	Qinpl	