0.6Ω Dual SPDT Negative Signal Handing Analog Switch

General Description

The ET5229H is an advanced CMOS analog switch fabricated in Sub−micron silicon gate CMOS technology. The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver. The switches can handle negative signal down to -2.5V.

ET5229H is offered in a small QFN10L package, which is ideal for small form factor portable equipment.

Features

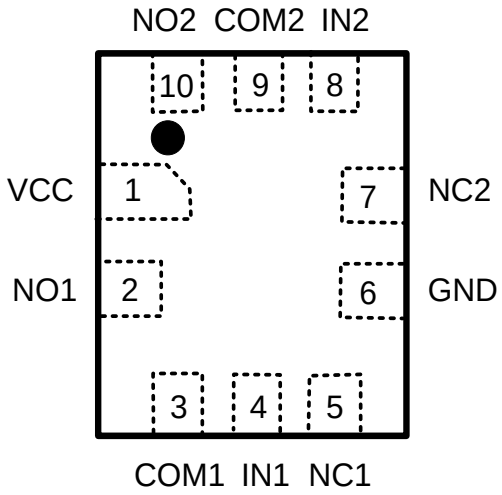
- Low R_{ON} is typical 0.6Ω @ V_{CC} =3.3V
- Single supply operation from 1.65V to 5.5V
- Full -2.5V to V_{CC} signal handling capability
- High off-channel isolation
- Very low standby current
- Very low distortion
- Break-Before-Make(BBM) switching
- High continuous current capability is ±300mA through each switch
- Package information:

Part No.	Package	MSL
ET5229H	QFN10L (1.8mm×1.4mm)	Level 1

Application

- Smart Phones and Cellular Phones
- Cell Phone Audio Block/ Speaker
- Earphone Switching Ring-Tone Chip
- Amplifier Switching/Modems

Pin Configuration



Top View

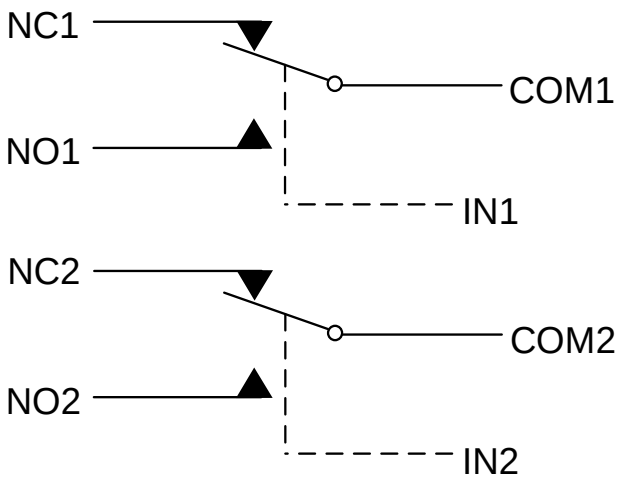
Pin Function

Pin NO.	Pin Name	Description
1	VCC	Power supply
2	NO1	Independent Channels
3	COM1	Common Channels
4	IN1	Controls
5	NC1	Independent Channels
6	GND	Ground (V)
7	NC2	Independent Channels
8	IN2	Controls
9	COM2	Common Channels
10	NO2	Independent Channels

Truth Table

IN1/2	NO1/2 to COM1/2	NC1/2 to COM1/2
0	OFF	ON
1	ON	OFF

Analog Symbol



Analog Symbol

Absolute Maximum Ratings

Symbol	Characteristic	Value	Unit
V_{CC}	Supply Voltage	-0.5～+6.5	V
V_{IS}	Analog Input Voltage	-3～V_{CC}+0.3 $\|V_{CC}-V_{IS}\|$ <6.5V	V
V_{IN}	Digital Select Input Voltage	-0.5～+6.5	V
V_O	Output Voltage	-3～V_{CC}+0.3 $\|V_{CC}-V_O\|$ <6.5V	V
I_{AN1}	Continuous DC Current from COM to NC/NO	±300	mA
I_{AN-PK1}	Peak Current from COM to NC/NO, 10 Duty Cycle (1)	±500	mA
I_{CLMP}	Continuous DC Current into COM/NO/NC with Respect to V_{CC}	±100	mA
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_S	Storage Temperature	-55 to 150	°C
V_{ESD}	Human Body Model (2)	±6000	V
	Charge-Device Mode (2)	±1500	V
I_{LU}	Latch Up (Current Maximum Rating) (2)	200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Note1.Defined as 10% ON, 90% off duty cycle.

Note2.This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per ESDA/JEDEC JS-001-2017

CDM tested per ESDA/JEDEC JS-002-2018

Latch up Current Maximum Rating tested per JEDEC78

Recommended Operating Conditions

Symbol	Characteristic	Min	Max	Unit
V_{CC}	DC Supply Voltage	1.65	5.5	V
V_{IN}	Digital Select Input Voltage	GND	5.5	V
V_{IS}	Analog Input Voltage (3)	-2.5	V_{CC}	V
T_A	Operating Temperature Range	-40	+85	°C
tr , t_f	Input Rise or Fall Time, SELECT	0	20	ns/V

Note3. To ensure normal transmission of V_{IS}, please follow $|V_{CC}-V_{IS}|$ <5.5V.

Electrical Characteristics

Symbol	Parameter	Test Conditions		T_A=25°C			T_A=-40~85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage, Select Inputs	V_{CC} = 1.65~5.5	1.65	0.9			1.0		V
			3.7	1.4			1.5		
			5.5	1.5			1.6		
V_{IL}	Low-Level Input Voltage, Select Inputs	V_{CC}= 1.65~5.5	1.65			0.4		0.35	V
			3.7			0.5		0.45	
			5.5			0.6		0.55	
I_{IN}	Maximum Input Leakage Current, Select Inputs	V_{IN} =V_{CC} or GND V_{CC} =5.5V				±0.3		±1.0	uA
I_{OFF}	Power Off Leakage Current	V_{IN} =5.5V V_{CC} =0V				±0.5		±1.0	uA
I_{CC}	Maximum Quiescent Supply Current (4)	V_{CC} =5.5V, I_{OUT} =0 V_{IN} = V_{CC} or GND				±0.5		±1.0	uA
I_{CCT}	Increase in I_{CC} per Input	IN1=2.6V, IN2=0V, or IN2=2.6V, IN1=0V, V_{CC} =4.3V		0.5	1.5	3.0		10	uA
		IN1=1.8V, IN2=0V, or IN2=1.8V, IN1=0V, V_{CC} =4.3V		1	4.5	7.0		20	
$I_{COM(ON)}$	COM ON leakage Current (5)	V_{IN} = V_{IL} or $V_{IH.}$, V_{NO}=0.3V or 4.7V V_{NC} floating V_{NC}=0.3V or 4.7V V_{NO} floating V_{COM}=0.3Vor 4.7V V_{CC} =5.5V		-20		20	-100	100	nA
R_{ON}	On−Resistance (4) (5)	I_{COM} = 20mA V_{IS}=-0.5V~0.5V, V_{CC} =4.3V		0.2	0.5	0.8	0.1	0.9	Ω
		I_{COM} = 20mA, V_{IS}=-0.5V~0.5V, V_{CC} =3.3V		0.3	0.6	0.9	0.2	1.0	
R_{FLAT}	On−Resistance Flatness (4) (5) (7)	I_{COM}=20mA V_{IS}=-0.5V~0.5V, V_{CC} =4.3V		0	0.05	0.2	0	0.3	Ω
ΔR_{ON}	On−Resistance Match Between Channels (4) (5) (6)	I_{COM}=20mA V_{IS}=0.5V V_{CC} =4.3V		0	0.1	0.2	0	0.3	Ω

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	T_A=25°C			T_A=-40~85°C		Unit
			Min	Typ	Max	Min	Max	
t_{ON}	Turn−On Time (4) (Figure 1)	V_{IS}=0.5V, V_{CC} =2.5~3.3V	10	35	55	5	70	ns
		V_{IS}=0.5V, V_{CC} =3.3~5.5V	5	25	45	3	65	
t_{OFF}	Turn−Off Time (4) (Figure 1)	V_{IS}=0.5V, V_{CC} =2.5~3.3V	5	26	50	3	60	ns
		V_{IS}=0.5V, V_{CC} =3.3~5.5V	3	20	40	1	50	
t_{BBM}	Break-Before-Make Time (4) (Figure 2)	C_L=35pF, R_L=50Ω V_{IS}=0.5V, V_{CC} =2.5~3.3V	3	15	30	3	40	ns
		C_L=35pF, R_L=50Ω V_{IS}=0.5V, V_{CC} =3.3~5.5V	1	7	25	1	35	
BW	On-Channel -3dB Bandwidth or Frequency Response (4) (Figure 4)	R_{IS}=50Ω	45	65				MHz
V_{ISO}	Off−Channel Isolation (4) (Figure 5)	F_{IS} = 100kHz, V_{IN} =GND or V_{CC} C_L=5pF， R_L= 50Ω V_{IS}=1V V_{PP}	-45	-65				dB
Q	Charge Injection Select Input to Common I/O (4) (Figure 3)	V_{IN} = 0 or V_{CC} R_{IS}=0Ω,C_L=100pF R_L=1MΩ $Q=C_L \times \Delta V_{OUT}$		25				pC
THD	Total Harmonic Distortion THD +Noise (4)	F_{IS}=20Hz to 20KHz R_L=50Ω,C_L=5pF V_{IS}=2V RMS V_{CC} =3.6V		0.06	0.3			%
		F_{IS}=20Hz to 20KHz R_L=50Ω,C_L=5pF V_{IS}=2V RMS V_{CC} =5V		0.03	0.2			%
V_{CT}	Channel−to−Channel Crosstalk (4) (Figure 6)	F_{IS}= 100KHz, V_{IN} =GND or V_{CC} R_L= 50Ω,C_L=5pF V_{IS}=1V V_{PP}	-60	-90				dB

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	T_A=25°C			T_A=-40~85°C		Unit
			Min	Typ	Max	Min	Max	
C_{IN}	Control Pin Input Capacitance (4)	V_{CC} =3.6V		4.5	8			pF
C_{NC}/C_{NO}	NC/NO Port Capacitance (4)	V_{CC} =3.6V		20	30			pF
C_{COM}	COM Port Capacitance When Switch is Enabled (4)	V_{CC} =3.6V		80	120			pF

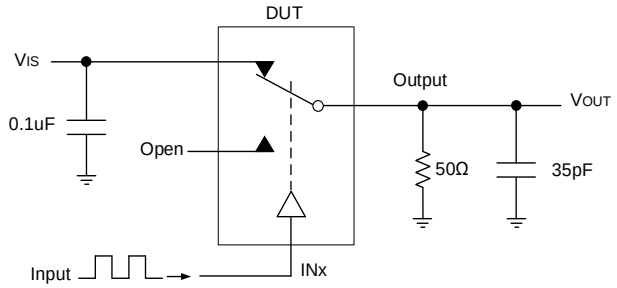
Note4. Guaranteed by design.

Note5. Guaranteed by design. Resistance measurements do not include test circuit.

Note6. $\Delta R_{ON} = R_{ON(NC1)} - R_{ON(NC2)}$ or $R_{ON(No1)} - R_{ON(No2)}$ when V_{IS} is same.

Note7. Flatness is defined as the difference between the maximum and minimum value of on−resistance as measured over the specified analog signal ranges.

Test Circuit



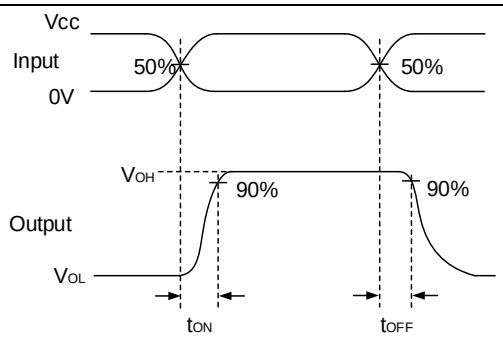
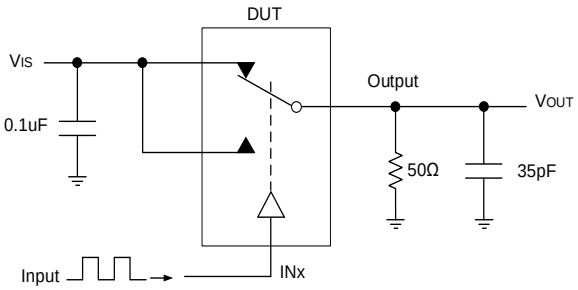


Figure1. t_{ON} /t_{OFF}



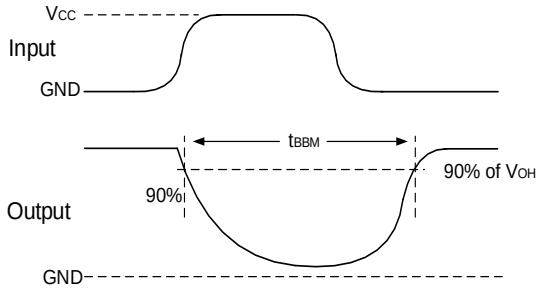
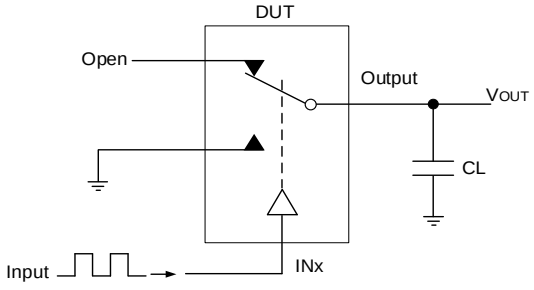


Figure2. t_{BBM}



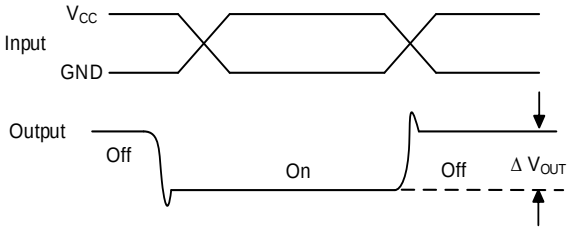


Figure3. Charge Injection

Test Circuit (Continued)

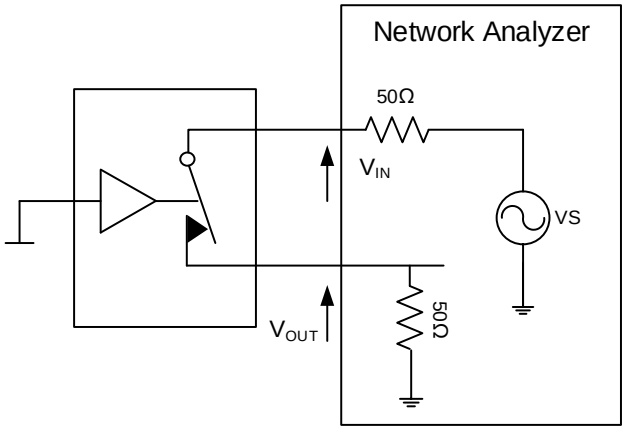
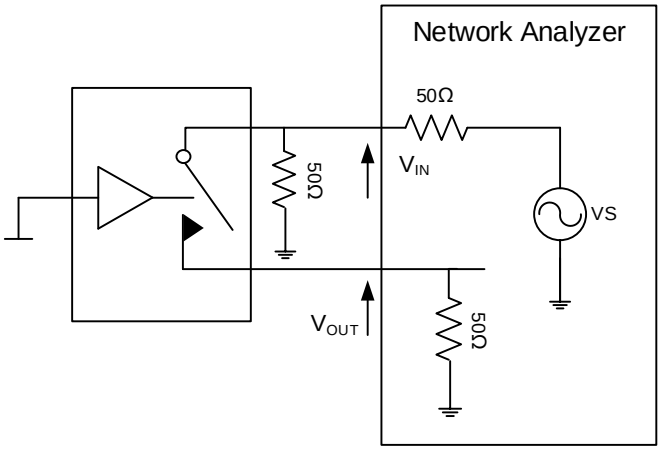
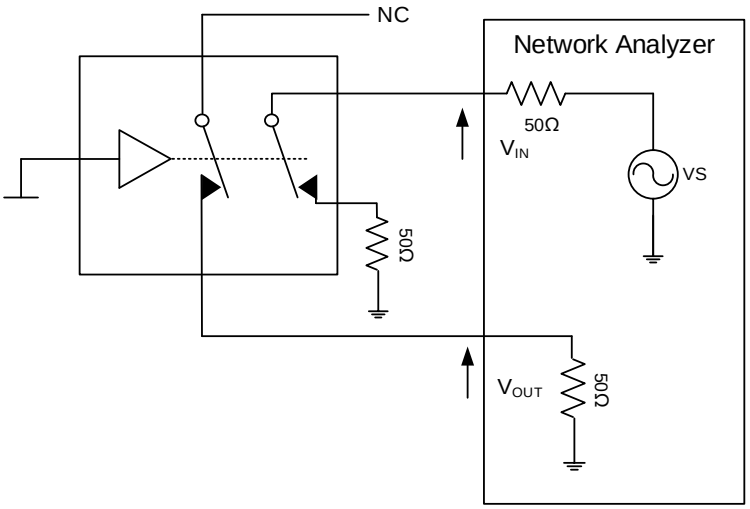


Figure4. Bandwidth



Off-Isolation=20 Log(V_{OUT}/V_{IN})

Figure5. Channel Off Isolation

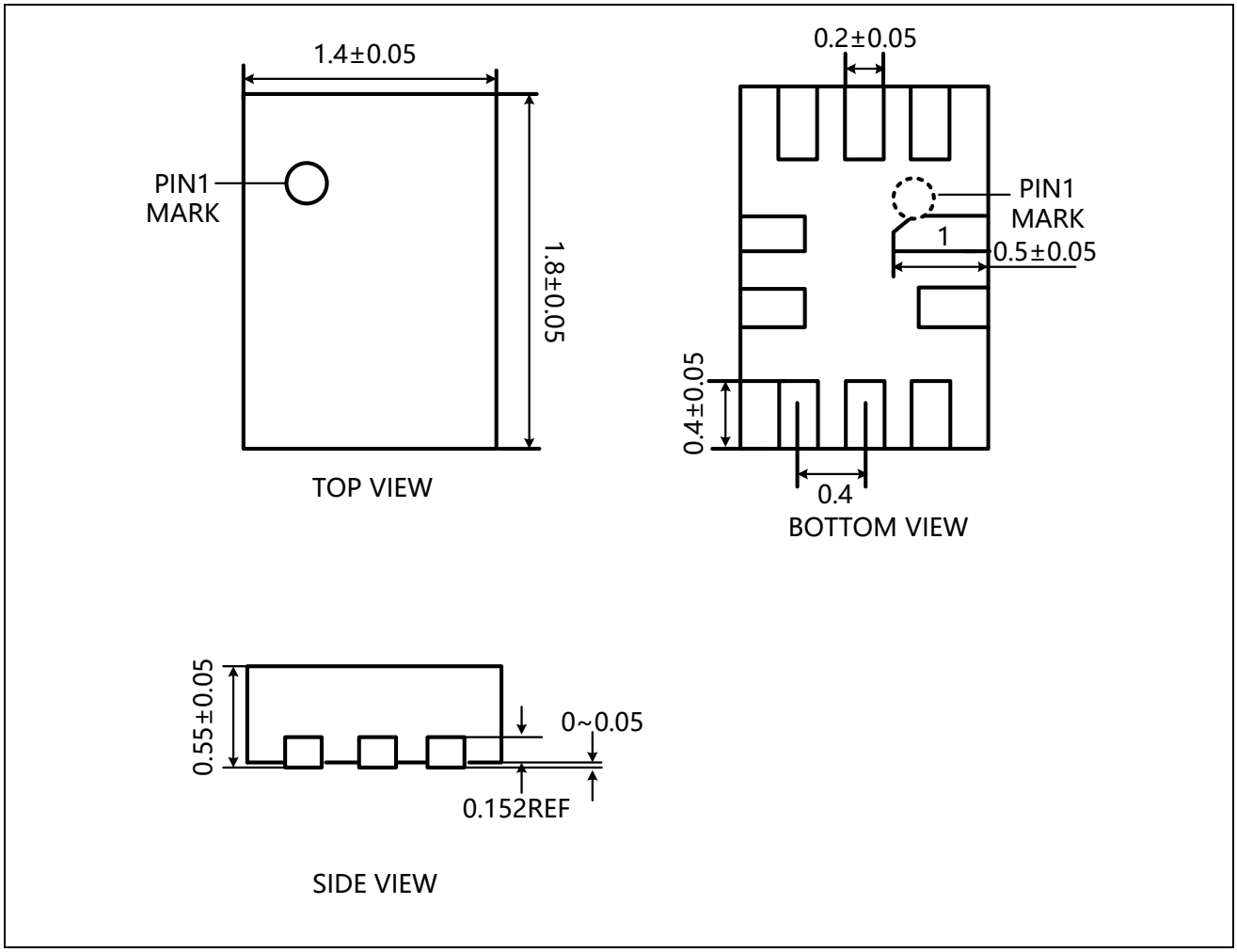


CROSSTALK=20 Log(V_{OUT}/$_{VIN}$)

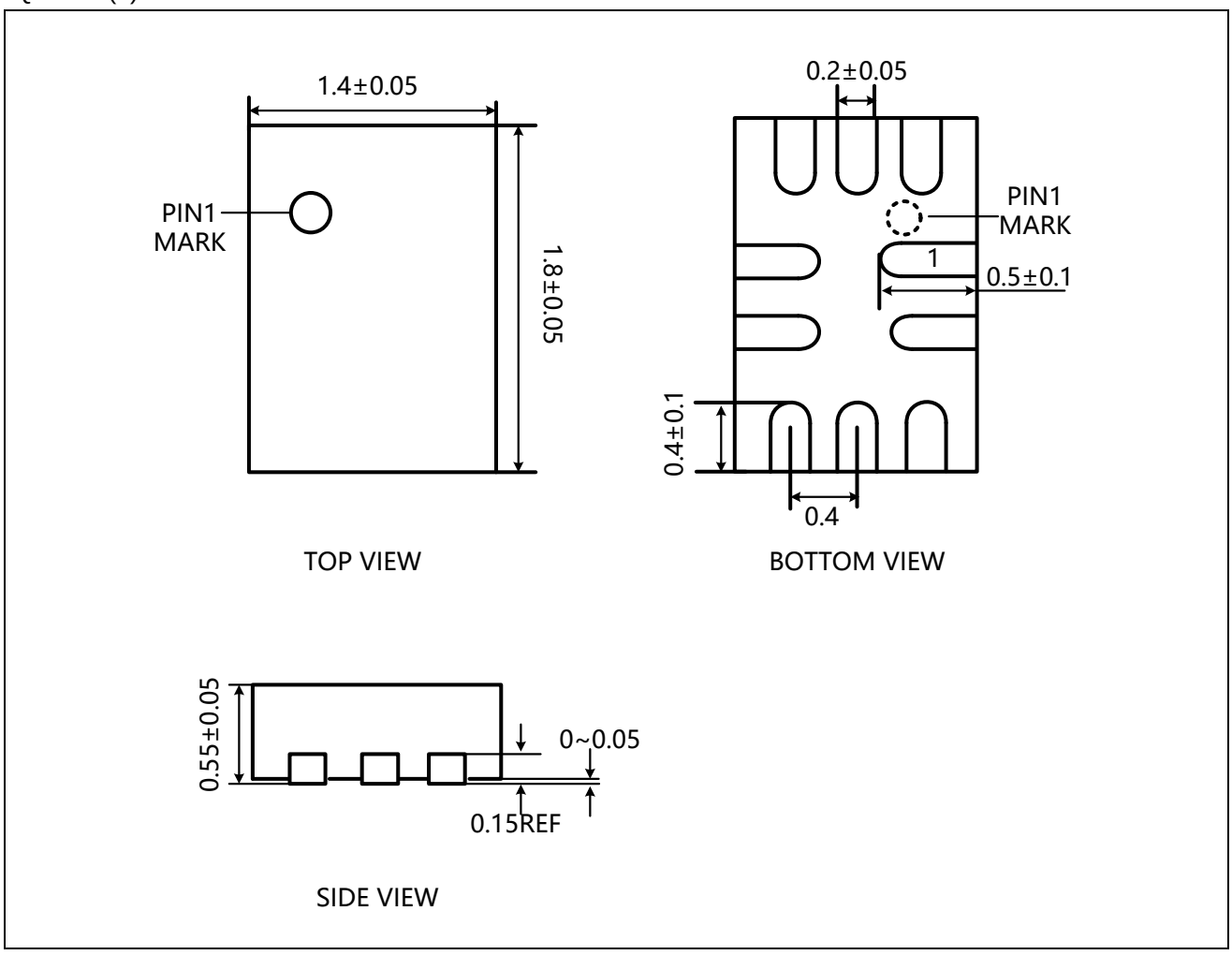
Figure6. Non-Adjacent Channel-to-Channel Crosstalk

Package Dimension

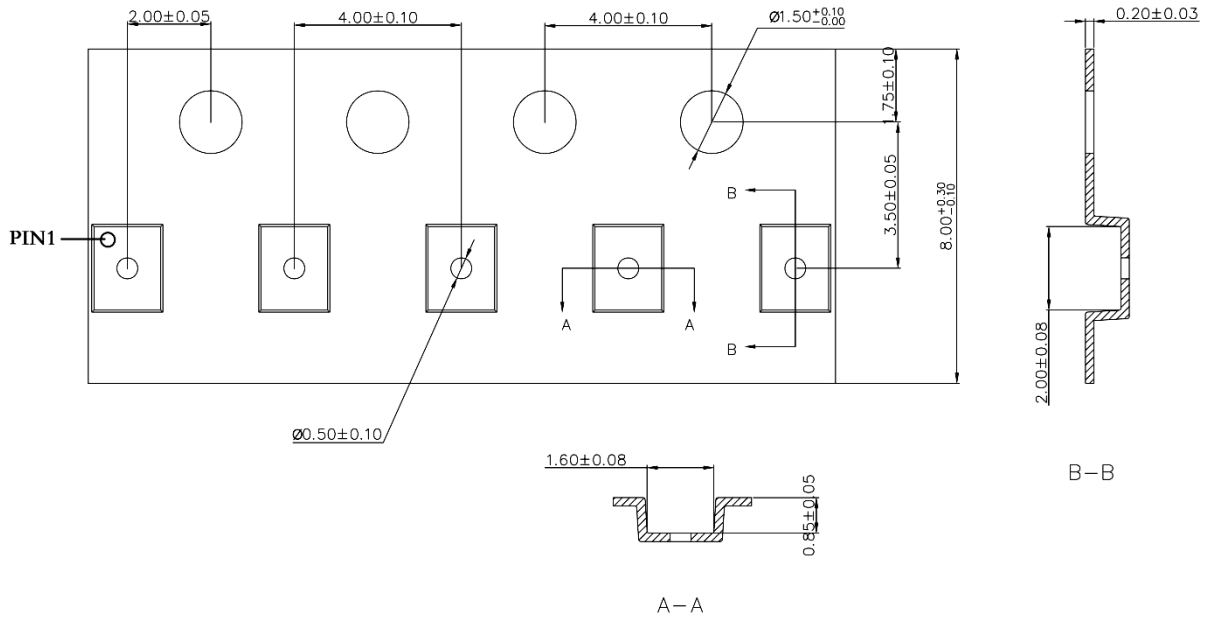
QFN10L(1)



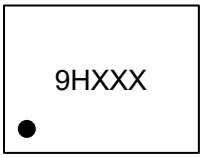
QFN10L(2)


1.4±0.05
PIN1
MARK
1.8±0.05
TOP VIEW
0.2±0.05
PIN1
MARK
1
0.5±0.1
0.4±0.1
0.4
BOTTOM VIEW
0.55±0.05
0~0.05
0.15REF
SIDE VIEW

Tape Information



Marking Information



9H - Part Number

XXX - Tracking Number

Note: XXX (Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-05-09	Preliminary Version	Yin peng	Lu hao	Liu Jia Ying
1.0	2024-08-23	Original Version	Yin peng	Lu hao	Liu Jia Ying