

0.6Ω Dual SPDT Negative Signal Handling Analog Switch

General Description

The ET5228H is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver. The switches can handle negative signal down to -2.5V.

ET5228H is offered in a small QFN10L package, which is ideal for small form factor portable equipment.

Features

- Low R_{ON} is typical 0.6Ω @ $V_{CC} = 3.3V$
- Single supply operation from 1.65V to 5.5V
- Full -2.5V to V_{CC} signal handling capability
- High off-channel isolation
- Very low standby current
- Very low distortion
- Break-Before-Make(BBM) switching
- High continuous current capability is $\pm 300mA$ through each switch
- Package information:

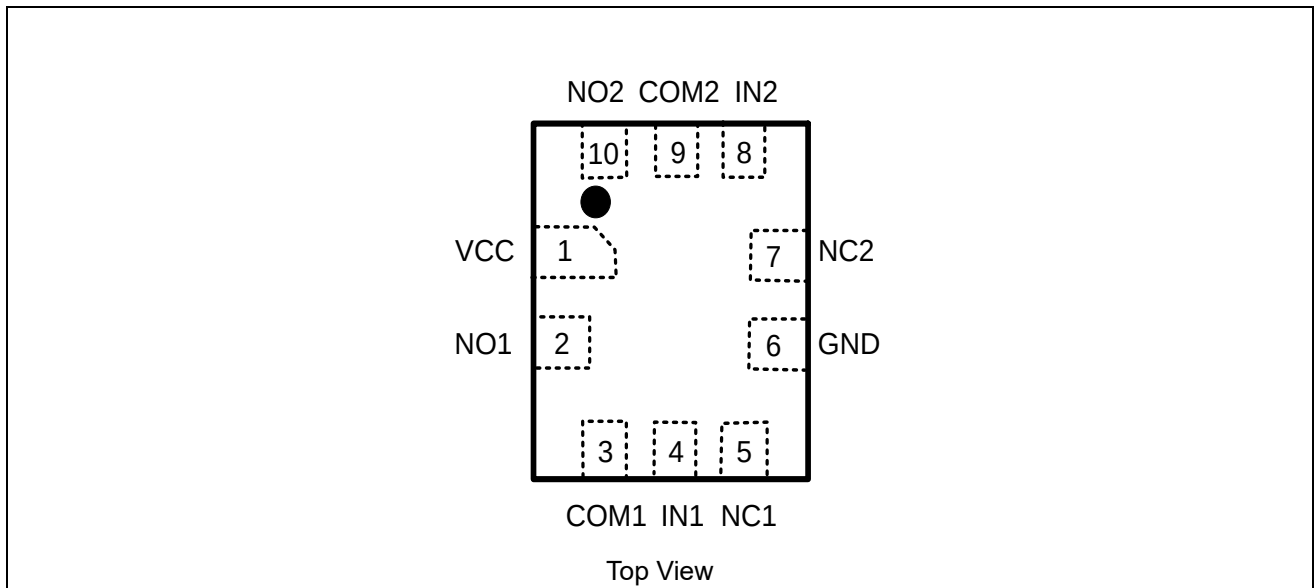
Part No.	Package	MSL
ET5228H	QFN10L (1.8mm×1.4mm)	Level 1

Application

- Smart Phones and Cellular Phones
- Cell Phone Audio Block/ Speaker
- Earphone Switching Ring-Tone Chip
- Amplifier Switching/Modems

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Pin Configuration



Pin Function

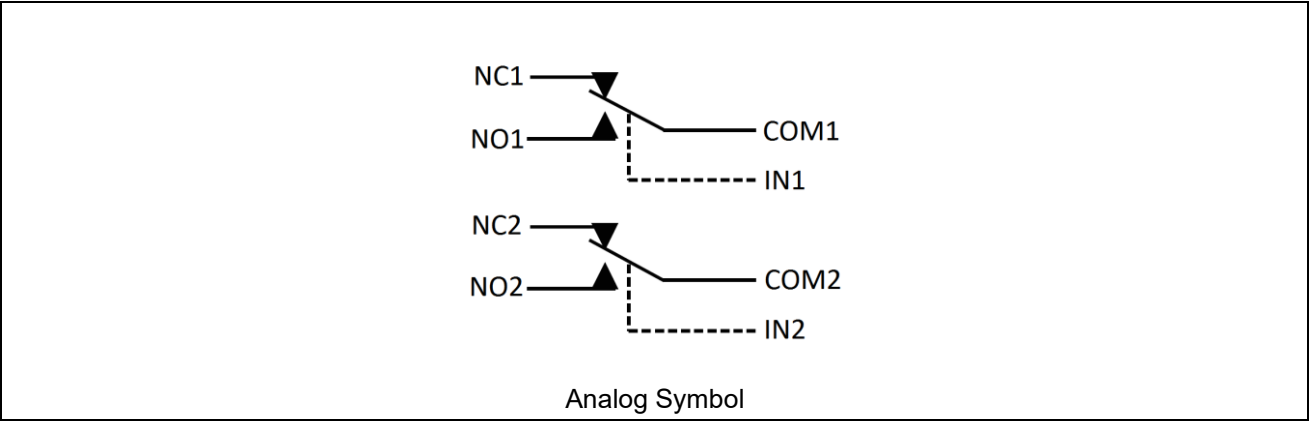
Pin NO.	Pin Name	Description
1	VCC	Power supply
2	NO1	Independent Channels
3	COM1	Common Channels
4	IN1	Controls
5	NC1	Independent Channels
6	GND	Ground (V)
7	NC2	Independent Channels
8	IN2	Controls
9	COM2	Common Channels
10	NO2	Independent Channels

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Truth Table

IN1/2	NO1/2 to COM1/2	NC1/2 to COM1/2
0	OFF	ON
1	ON	OFF

Analog Symbol



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Absolute Maximum Ratings

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5~+6.5	V
Analog Input Voltage		V_{IS}	-3~ $V_{CC}+0.3$ $ V_{CC}-V_{IS} < 6.5V$	V
Digital Select Input Voltage		V_{IN}	-0.5~+6.5	V
Output Voltage		V_O	-3~ $V_{CC}+0.3$ $ V_{CC}-V_O < 6.5V$	V
Continuous DC Current from COM to NC/NO		I_{AN1}	±300	mA
Peak Current from COM to NC/NO, 10 Duty Cycle ⁽¹⁾		I_{AN-PK1}	±500	mA
Continuous DC Current into COM/NO/NC with Respect to V_{CC}		I_{CLMP}	±100	mA
Maximum Junction Temperature		$T_{J(MAX)}$	150	°C
Storage Temperature		T_S	-55 to 150	°C
ESD	Human Body Model ⁽²⁾	HBM	±6000	V
	Charge-Device Mode ⁽²⁾	CDM	±1500	V
Latch Up (Current Maximum Rating) ⁽²⁾		I_{LU}	200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Note1. Defined as 10% ON, 90% off duty cycle.

Note2. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per ESDA/JEDEC JS-001-2017

CDM tested per ESDA/JEDEC JS-002-2018

Latch up Current Maximum Rating tested per JEDEC78

Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	1.65	5.5	V
Digital Select Input Voltage	V_{IN}	GND	5.5	V
Analog Input Voltage ⁽³⁾	V_{IS}	-2.5	V_{CC}	V
Operating Temperature Range	T_A	-40	+85	°C
Input Rise or Fall Time, SELECT	t_r, t_f	0	20	ns/V

Note3. To ensure normal transmission of V_{IS} , please follow $|V_{CC}-V_{IS}| < 5.5V$.

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Electrical Characteristics

Symbol	Parameter	Test Conditions	T _A =25°C			T _A =-40~85°C		Unit
			Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage, Select Inputs	V _{CC} = 1.65~5.5	1.65	0.9		1.0		V
			3.3	1.6		1.7		
			5.5	2.2		2.3		
V _{IL}	Low-Level Input Voltage, Select Inputs	V _{CC} = 1.65~5.5	1.65		0.4		0.35	V
			3.3		0.5		0.45	
			5.5		0.6		0.55	
I _{IN}	Maximum Input Leakage Current, Select Inputs	V _{IN} =V _{CC} or GND V _{CC} =5.5V			±0.3		±1.0	uA
I _{OFF}	Power Off Leakage Current	V _{IN} =5.5V V _{CC} =0V			±0.5		±1.0	uA
I _{CC}	Maximum Quiescent Supply Current ⁽⁴⁾	V _{CC} =5.5V, I _{OUT} =0 V _{IN} = V _{CC} or GND			±0.5		±1.0	uA
I _{CC} T	Increase in I _{CC} per Input	IN1=2.6V, IN2=0V, or IN2=2.6V, IN1=0V, V _{CC} =4.3V		1.5	3.0		10	uA
		IN1=1.8V, IN2=0V, or IN2=1.8V, IN1=0V, V _{CC} =4.3V		4.5	7.0		20	
I _{COM(ON)}	COM ON leakage Current ⁽⁵⁾	V _{IN} = V _{IL} or V _{IH} , V _{NO} =0.3V or 4.7V V _{NC} floating V _{NC} =0.3V or 4.7V V _{NO} floating V _{COM} =0.3Vor 4.7V V _{CC} =5.5V	-20		20	-100	100	nA
R _{ON}	On-Resistance ^{(4) (5)}	I _{COM} = 20mA V _{IS} =-0.5V~0.5V, V _{CC} =4.3V		0.5	0.8		0.9	Ω
		I _{COM} = 20mA, V _{IS} =-0.5V~0.5V, V _{CC} =3.3V		0.6	0.9		1.0	
R _{FLAT}	On-Resistance Flatness ^{(4) (5) (7)}	I _{COM} =20mA V _{IS} =-0.5V~0.5V, V _{CC} =4.3V			0.2		0.3	Ω
ΔR _{ON}	On-Resistance Match Between Channels ^{(4) (5) (6)}	I _{COM} =20mA V _{IS} =0.5V V _{CC} =4.3V		0.1	0.2		0.3	Ω

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Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	T _A =25°C			T _A =-40~85°C		Unit
			Min	Typ	Max	Min	Max	
t _{ON}	Turn-On Time ⁽⁴⁾ (Figure 1)	V _{IS} =0.5V, V _{CC} =2.5~3.3V		35	55			ns
		V _{IS} =0.5V, V _{CC} =3.3~5.5V		25	45			
t _{OFF}	Turn-Off Time ⁽⁴⁾ (Figure 1)	V _{IS} =0.5V, V _{CC} =2.5~3.3V		26	50			ns
		V _{IS} =0.5V, V _{CC} =3.3~5.5V		20	40			
t _{BBM}	Break-Before-Make Time ⁽⁴⁾ (Figure 2)	C _L =35pF, R _L =50Ω V _{IS} =0.5V, V _{CC} =2.5~3.3V		15		7		ns
		C _L =35pF, R _L =50Ω V _{IS} =0.5V, V _{CC} =3.3~5.5V		7		3		
BW	On-Channel -3dB Bandwidth or Frequency Response ⁽⁴⁾ (Figure 4)	R _{IS} =50Ω		65				MHz
V _{ISO}	Off-Channel Isolation ⁽⁴⁾ (Figure 5)	F _{IS} = 100kHz, V _{IN} =GND or V _{CC} C _L =5pF, R _L = 50Ω V _{IS} =1V V _{PP}		-65				dB
Q	Charge Injection Select Input to Common I/O ⁽⁴⁾ (Figure 3)	V _{IN} = 0 or V _{CC} R _{IS} =0Ω, C _L =100pF R _L =1MΩ Q=C _L ×ΔV _{OUT}		25				pC
THD	Total Harmonic Distortion THD +Noise ⁽⁴⁾	F _{IS} =20Hz to 20KHz R _L =50Ω, C _L =5pF V _{IS} =2V RMS V _{CC} =3.6V		0.06				%
		F _{IS} =20Hz to 20KHz R _L =50Ω, C _L =5pF V _{IS} =2V RMS V _{CC} =5V		0.03				%
V _{CT}	Channel-to-Channel Crosstalk ⁽⁴⁾ (Figure 6)	F _{IS} = 100KHz, V _{IN} =GND or V _{CC} R _L = 50Ω, C _L =5pF V _{IS} =1V V _{PP}		-90				dB

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Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	T _A =25°C			T _A =-40~85°C		Unit
			Min	Typ	Max	Min	Max	
C _{IN}	Control Pin Input Capacitance ⁽⁴⁾	V _{CC} =3.6V		4.5				pF
C _{NC/CNO}	NC/NO Port Capacitance ⁽⁴⁾	V _{CC} =3.6V		20.0				pF
C _{COM}	COM Port Capacitance When Switch is Enabled ⁽⁴⁾	V _{CC} =3.6V		80.0				pF

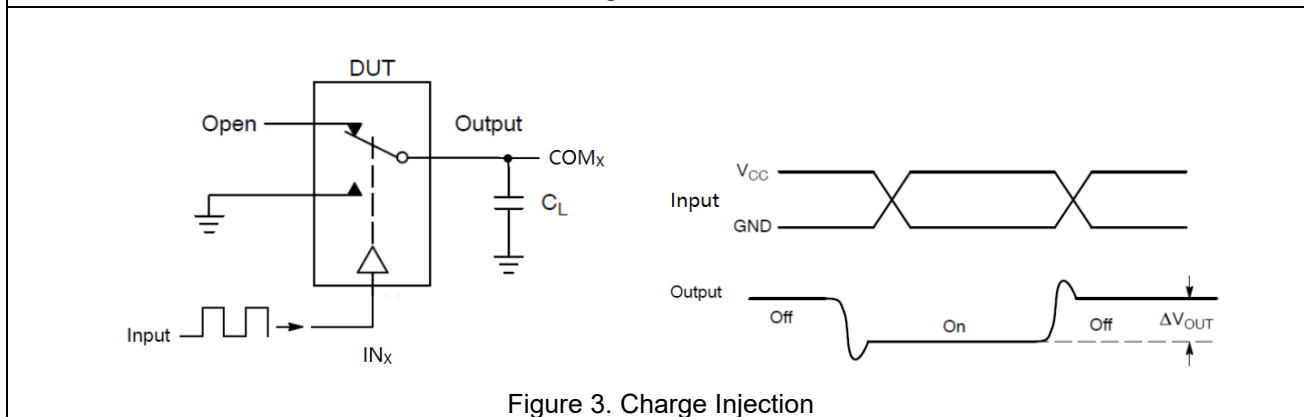
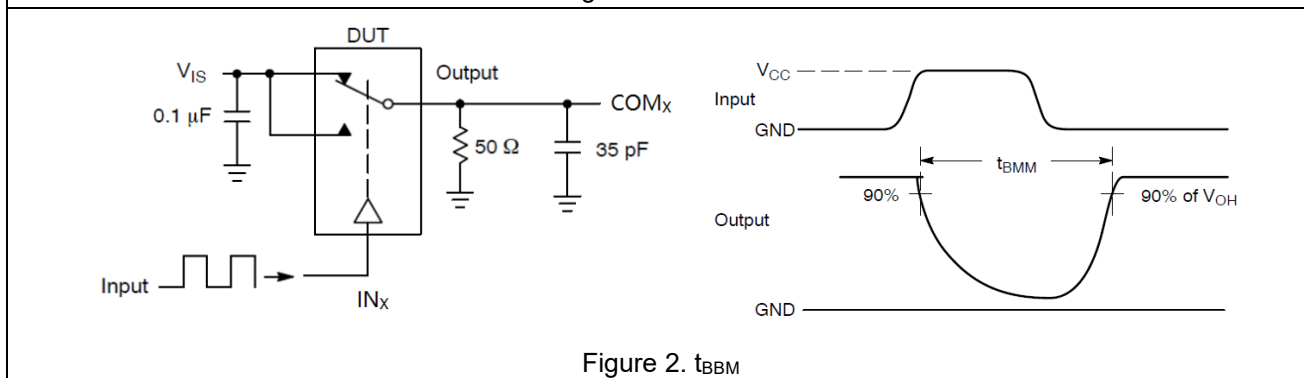
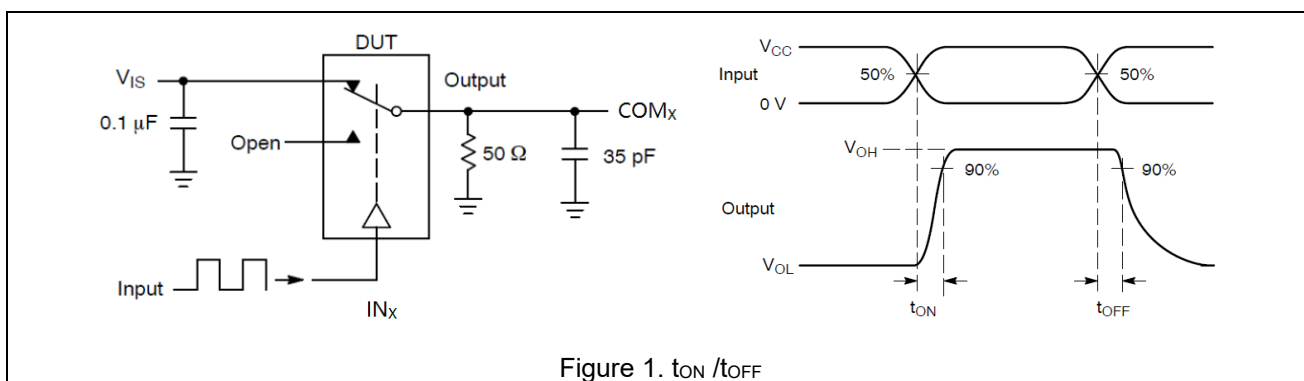
Note4. Guaranteed by design

Note5. Guaranteed by design. Resistance measurements do not include test circuit or package resistance

Note6. $\Delta R_{ON} = R_{ON(NC1)} - R_{ON(NC2)}$ or $R_{ON(NO1)} - R_{ON(NO2)}$ when V_{IS} is same.

Note7. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Test Circuit



Test Circuit (Continued)

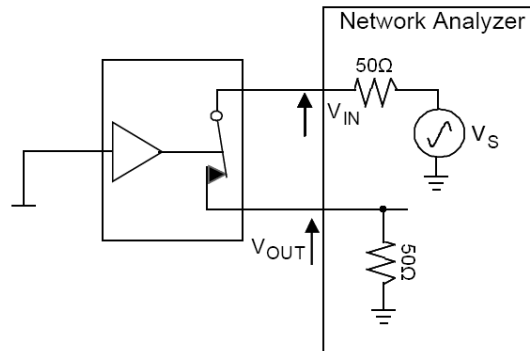
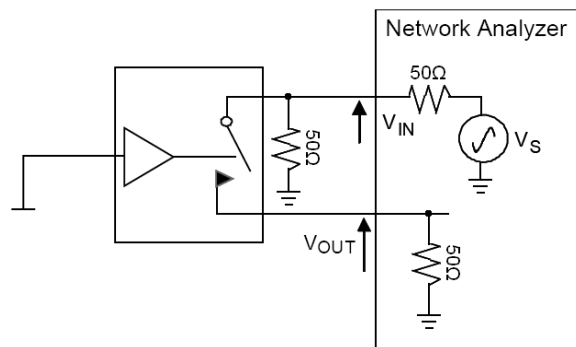
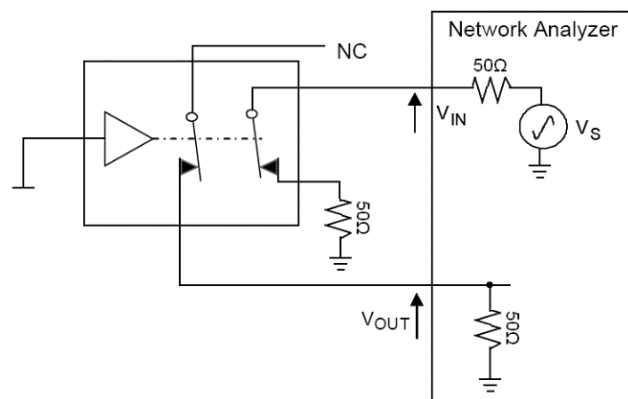


Figure 4. Bandwidth



$$\text{Off-Isolation} = 20 \log (V_{\text{OUT}} / V_{\text{IN}})$$

Figure 5. Channel Off Isolation



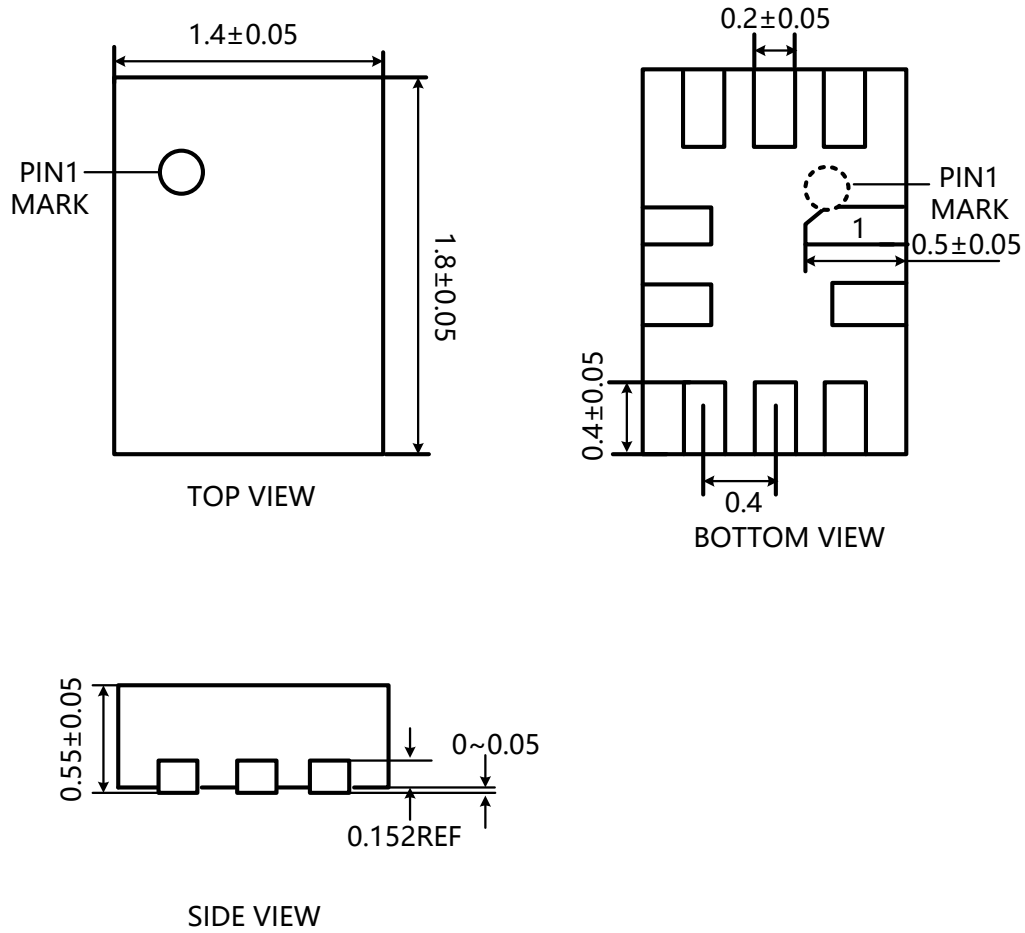
$$\text{CROSSTALK} = 20 \log (V_{\text{OUT}} / V_{\text{IN}})$$

Figure 6. Non-Adjacent Channel-to-Channel Crosstalk

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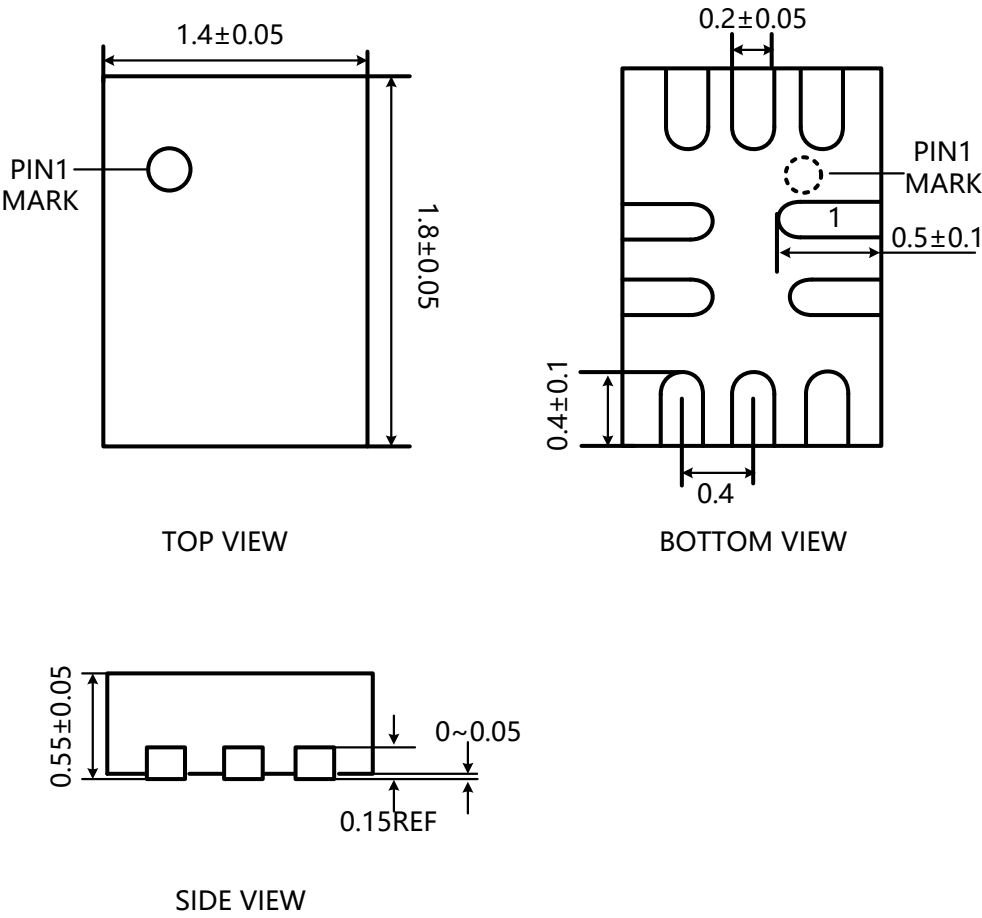
Package Dimension

QFN10L(1)



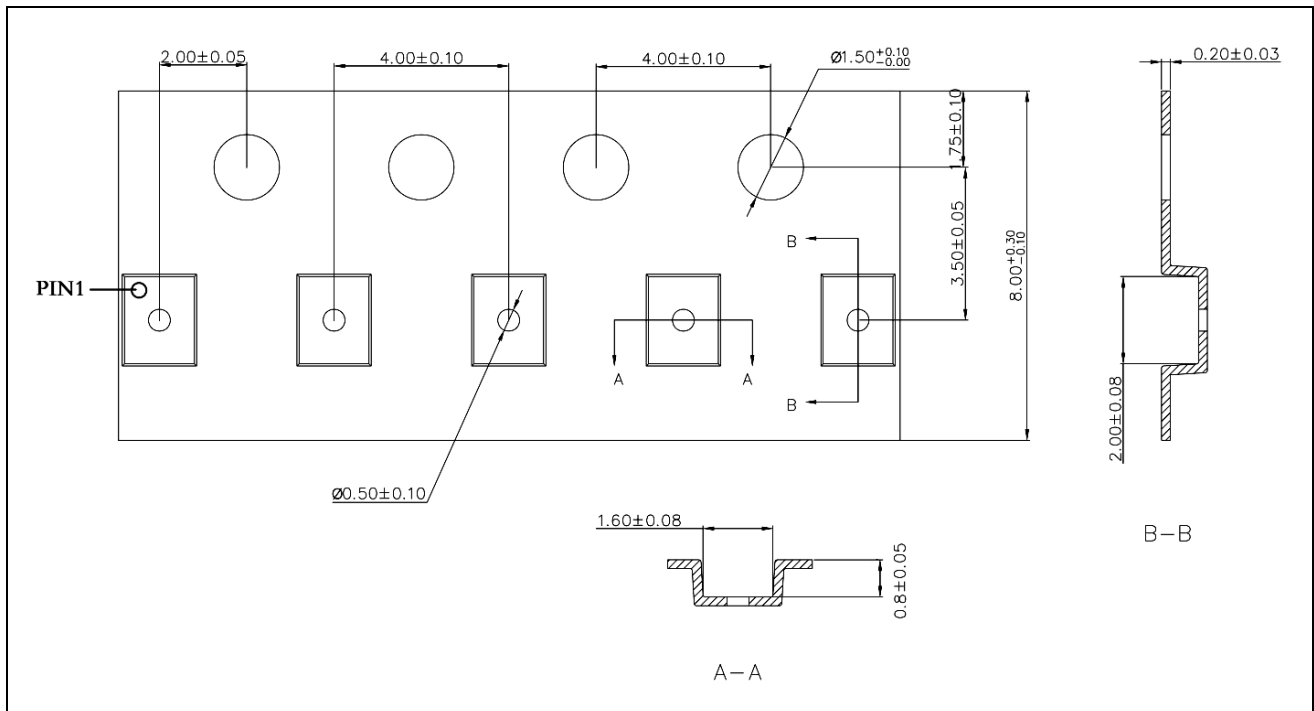
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QFN10L(2)

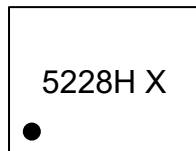


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Tape Information



Marking Information



5228H - Part Number

X - Tracking Number

Note: X (Tracking Number) is variable, according to the wafer lot number.

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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-10-17	Original Version	liuxm	liujy	liujy
1.1	2020-01-02	Add Tape Information	liuxm	Zhuji	Zhuji
1.2	2020-02-24	documents check and formalize	Shib	Liujiy	Liujiy
1.3	2020-02-28	Add ESD value and update package dimension picture	liuxm	liujy	liujy
1.4	2020-06-01	Correct Typo	Wuxj	liujy	liujy
1.5	2020-07-22	Update Vis and THD	Wuxj	liujy	liujy
1.6	2021-5-21	Update package	Wuxj	liujy	liujy
1.7	2022-8-10	Update Typeset	Wuxj	liujy	liujy