4.5 ~ 18V, 0.75 ~ 5A, Current Limit Power Switch with Reverse Block

General Description

The ET20170H is a current limit N-Channel MOSFET power switch. It is designed to protect circuitry on the output from transients on the input. It also protects the input from undesired shorts and transients coming from the output.

The current limit magnitude is controlled by an external resistor from ILIMIT to GND. It is fixed 0.73A when ILIMIT is floating. Programmable soft-start time controls the slew rate of the output voltage during the start-up time. It can be controlled by the DV/DT pin setting.

The ET20170H offer a GATE drive signal connected to an external N-Channel MOSFET gate to block current flowing from the output to the input when the IC is disable, power off or thermal shutdown.

In the event device temperature (T_J) exceeds $T_{SD}(155^{\circ}C)$, The ET20170H device remains off for 100ms until the temperature drops to T_{SD} - T_{SD_HYS} (30°C), after which it attempts to restart. This ON and OFF cycle continues until fault is cleared.

Features

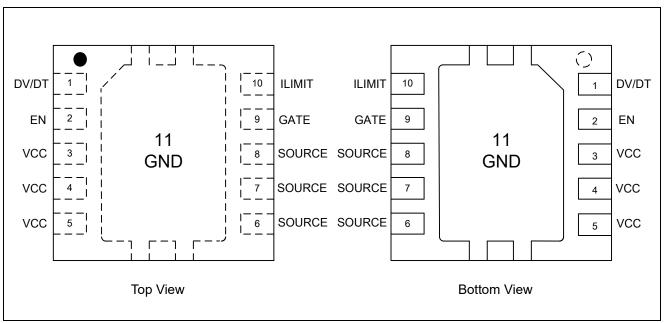
- V_{IN} Operating Range: 4.5V to 18V
- Programmable Current Limit and Soft-Start Time
- Short-Circuit Protection
- Typical R_{ON}: 31mΩ From Input to Output Power Path
- Very Low Quiescent Current: 110µA (Typ)
- Reverse-Blocking MOSFET Driver
- Over-Current Protection
- Internal Thermal Shutdown Protection
- ESD Human Body Model Protected: All pins ± 2KV Pass
- Package Information

Part No.	Package	MSL
ET20170H	DFN10 (3.0mm × 3.0mm)	Level 1

Application

- SSD Hard Disk
- PC Cards
- Wireless Modem Data Cards
- USB Power Distribution/USB Protection
- USB 3.1 Power Delivery
- Server PC

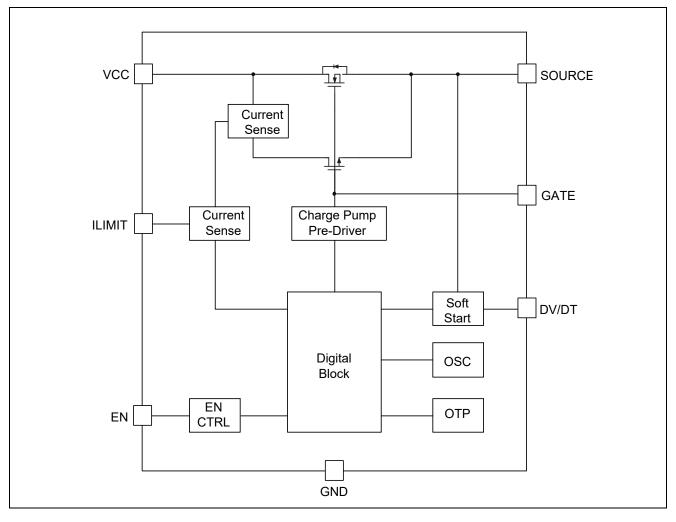
Pin Configuration



Pin Function

Pin	Name	Description		
1 DV/DT		Soft start programming pin. Connect a capacity from DV/DT to GND to set the		
I	00/01	DV/DT slew rate.		
		This is a dual function control pin. When used as an ENABLE pin and pulled down,		
		it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it		
2	EN	enables the device and BFET.		
		As an UVLO pin, it can be used to program different UVLO trip point via external		
		resistor divider.		
3,4,5	VCC	Power supply input. Must be closely decoupled to GND pins with a 1uF or greater		
3,4,5	VCC	ceramic capacitor. Connect VCC using a wide PCB trace.		
6,7,8	SOURCE	Source of internal power n-channel MOSFET and the output terminal.		
9	GATE	Gate pin for external reverse-current block MOSFET.		
10	ILIMIT	Current limit programming pin. Program the current limit by connecting a resistor		
10		to GND. Floating ILIMIT pin to achieve a 0.73A fixed current limit.		
11	GND	Ground pin.		

Block Diagram



Operation

ET20170H is an an integrated power switch with a low R_{DSON} N-Channel MOSFET.When the ET20170H turns on, it can deliver up to 5A continuous current to load. When the device is active, the device only consumes 110uA supply current if no load.

Power Supply Considerations

At least 1 μ F MLCC capacitor between VCC and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input and minimize the input voltage droops. Additionally, bypassing the output with a 10 μ F MLCC capacitor improves the immunity of the device to short-circuit transients.

Current Limit(ILIMIT)

A sense FET is employed to check for over current conditions. When an over current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. ET20170H will limit the current until the overload condition is removed or the device begins to thermal cycle.

The current limit can be programmed by an external resistor. It can be approximated with equation below.

$$I_{ILIMIT} = 0.7 + 3 \times 10^{-5} \times R_{LIMIT}$$

The ET20170H allows ILIMIT to be floated during operation. The internal fixed current limit threshold is set at 0.73A. The current limit response time is about 20us⁽¹⁾.

Short-Circuit Protection(SCP)

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the ET20170H incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT} > I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 50% higher than the programmed overload current limit ($I_{FASTRIP} = 1.5 \times I_{LIMIT}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to llimit.

To prevent safe operating area(SOA) damage during a high input voltage short-circuit protection(SCP) condition, the IC current limit folds back when the power MOSFET VDS voltage is above the typical 11V and the junction temperature is over 100°C.

Soft Start

The soft start time can be set by an external capacity connecting from DV/DT to GND. The soft start time can be calculated with Equation:

$$t_{DVDT} = \frac{VCC}{GAIN} \times (C_{DVDT} + 70 pF) / I_{DVDT} = 10^{6} \times VCC \times (C_{DVDT} + 70 pF)$$

where:

- GAIN=8V
- I_{DVDT}=125nA

The dV/dt slew rate is determined by external DVDT capacitor.

Reverse-Blocking MOSFET Driver

The ET20170H has a GATE pin to provide an external N-channel MOSFET gate drive signal for reverse-current protection (RCP).

If GATE pin float, there is no RCP function.

Thermal Protection - Auto-Retry

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The ET20170H implements a thermal sensing to monitor the operating junction temperature of the power MOSFET. In an over-current or short-circuit condition, the junction temperature rises due to excessive power dissipation.

Once the die temperature rises to approximately 155°C due to over-current conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. When the temperature drops below its lower threshold (typically 125°C), the chip is enable again after a 100ms delay.

Three events can pull down the GATE voltage: VIN below the under-voltage lockout (UVLO), the enable (EN) voltage below the low level threshold, or thermal shutdown. If any of these conditions occur, GATE sinks the current from the gate of the external MOSFET to initiate a fast turn-off.

Note1: Test condition is as V_{IN}=12V, I_{LIMIT}=3.7A, T_A=25°C, C_{OUT}=0uF. Current Limit Response Time is the time difference between I_{OUT} first exceeding ILIM and falling back to I_{LIM}, and falling back to I_{LIMIT}. Short-circuit Response Time is the time difference between I_{OUT} exceeding I_{FASTRIP} and falling back to 0A.

5

Symbol		Min	Max	Unit	
V _{CC} ,V _{SOURCE}	VCC,S	SOURCE to GND	-0.3	20	V
Vgate	G	ATE to GND	-0.3	V _{SOURCE} +5.5	V
VILIMIT, VEN, VDVDT	ILIMIT,	EN, DV/DT to GND	-0.3	7	V
PD	Power Dissipation at T_A = +85°C ⁽²⁾			1.05	W
TJ	Junction Temperature		-40	+150	°C
Tstg	Storage Junction Temperature		-65	+150	°C
Tsold	Soldering Temperature (reflow)			+260	°C
V _{ESD}	Electrostatic Discharge Capability	Human Body Mode, ESDA/JEDEC JS-001-2023	-2.0	+2.0	ΚV
		Charged Device Mode, ESDA/JEDEC JS-002-2022	-1.5	+1.5	KV

Absolute Maximum Ratings

Note2: The maximum allowable Power Dissipation is recording to maximum allowable Junction Temperature.

 $P_{D(MAX)} \textcircled{O} T_A = (T_{J(MAX)} - T_A) / \theta_{JA}.$

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
VIN	DC Input Voltage	4.5	18	V
Ιουτ	DC Output Current Limit	0.73	5.0	А
T _A	Operating Temperature Range	-40	+85	°C

Electrical Characteristics

Unless otherwise noted, V_{CC} =12V, R_{LIMIT} =NS, C_{DVDT} =FLOAT, C_{OUT} =10uF, T_A =-40°C to 85°C, typical value is tested at T_A =25°C.

Symbol	Parameters	Conditions	Min	Тур	Мах	Unit
Basic Opera	ation					
VIN	Input Voltage		4.5		18	V
lq	VIN Quiescent Current	EN = High		110	150	uA
ls	VIN Shutdown Current	EN = GND		11	25	uA
Power MOS	FET					
R _{ON}	On-Resistance of Switch IN-OUT	R _{LIMIT} =100KΩ, I _{OUT} =1A		31	60	mΩ
t DELAY	Turn-on Delay Time	EN/UVLO→H, I _{VCC} = 100mA, 1-A resistive load at SOURCE		280		us
IOFF	Off-state Leakage Current	V_{CC} = 12V, V_{EN} = GND		0.1	3	uA
Vuvlo_r	Under Voltage Lockout Threshold	Under Voltage Vin Rising 4 15		4.3	4.5	V
VUNLOHYS	UVLO Hysteresis			190		mV
DV/DT						
		$ EN \rightarrow H \text{ to } V_{SOURCE} = 11.7V, \\ V_{CC} = 12V, C_{DVDT} = 0 $	0.7	1	1.3	ms
tdvdt	Output Ramp Time	$EN \rightarrow H \text{ to } V_{SOURCE} = 11.7V,$ $V_{CC}=12V, C_{DVDT}=1nF$		15		ms
Vdvdt_max	DV/DT Max Capacitor Voltage			5		V
IDV/DT	DV/DT Current	$V_{DV/DT} = 0.5V$		125		nA
GAIN _{DVDT} (3)	DV/DT to OUT Gain			8		V/V
Current Lim	it					
		ILIMIT float, V _{CC} =12V		0.73		Α
		R _{LIMIT} = 0, V _{CC} =12V		0.84		Α
h a see	Current Limit at	R _{LIMIT} = 10KΩ, V _{CC} =12V		1.1		Α
LIMIT_NO	Normal Operation	$R_{\text{LIMIT}} = 45.3 \text{K}\Omega, V_{\text{CC}} = 12 \text{V}$	1.79	2.07	2.42	Α
		$R_{\text{LIMIT}} = 100 \text{k}\Omega, V_{\text{CC}} = 12 \text{V}$	3.46	3.7	4.03	Α
		R _{LIMIT} = 150kΩ, V _{CC} =12V	4.5	5.0	5.7	Α
Iilim_b	ILIM Bias Current	R _{LIMT} =0		10		uA
Enable (EN)						
Ven_rising	EN Rising Threshold		1.37	1.45	1.54	V
Ven_hys	EN Hysteresis			250		mV

7

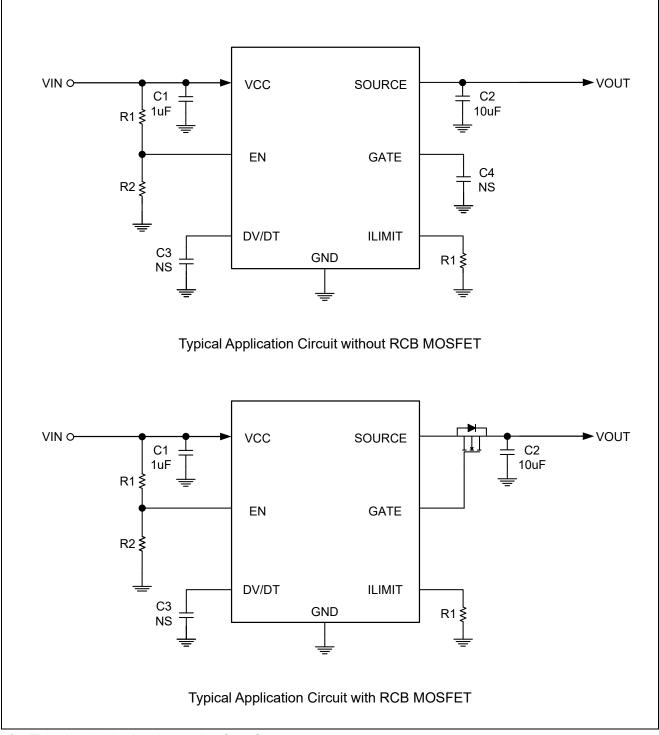
Electrical Characteristics (Continued)

Unless otherwise noted, V_{CC} =12V, R_{LIMIT} =NS, C_{DVDT} =FLOAT, C_{OUT} =10uF, T_A =-40°C to 85°C, typical value is tested at T_A =25°C.

Symbol	Parameters	Conditions	Min	Тур	Max	Unit
GATE						
Ig_source	DURCEGATE MaximumVcc=12V, EN=5V, VGATE=Vcc81		11	13	uA	
Ig_sink	GATE Maximum Sink Current	V _{CC} = V _{SOURCE} = 5.5V, V _{GATE} = 10.5V, EN=0		57		uA
V _{GATE}	GATE Voltage	R _{LIMIT} =100KΩ, I _{OUT} = 1A		V _{CC} +4.6		V
OTP						
Tsd	Thermal Shutdown			155		°C
T _{SD_HYS}	Thermal-shutdown Hysteresis			30		°C

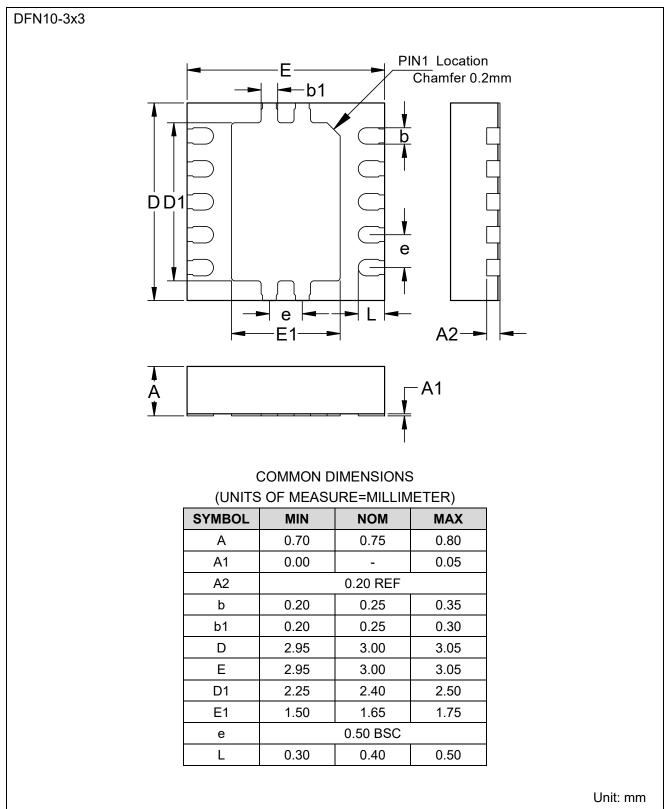
Note3: Guaranteed by design

Application Circuits

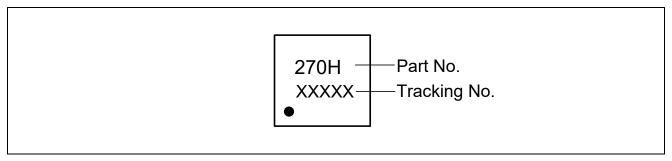


*: This electric circuit only supplies for reference.

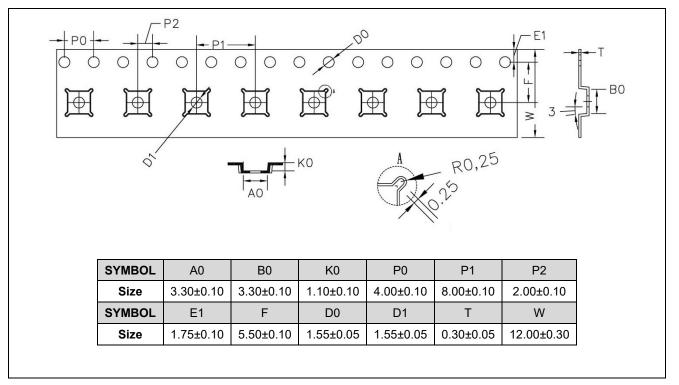
Package Dimension



Marking



Tape Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2023-12-1	Initial Version	Zoucm	Xuw	Shib
1.1	2023-12-13	Content and Package Dimension Upset	Zoucm	Xuw	Shib
1.2	2024-5-13	Update EC table	Zoucm	Xuw	Shib
1.3	2024-9-10	Update Application Circuits	Zoucm	Xuw	Shib