High-Current Over-Voltage Protectors

General Description

ET9668 can disconnect the systems from its output pin(OUT) in case wrong input operating conditions are detected. The input voltage can be up to 28V. The internal overvoltage thresholds (OVLO) can be selected by OVLO_SEL pin. When OVLO_SEL is HIGH, the overvoltage point is 21.9V, and the overvoltage point when OVLO_SEL is grounded is 12.4V. ET9668 has internal Thermal-Shutdown Protection function.

The device is packaged in advanced full-Green compliant Wafer Level Chip Scale Packaging (WLCSP20).

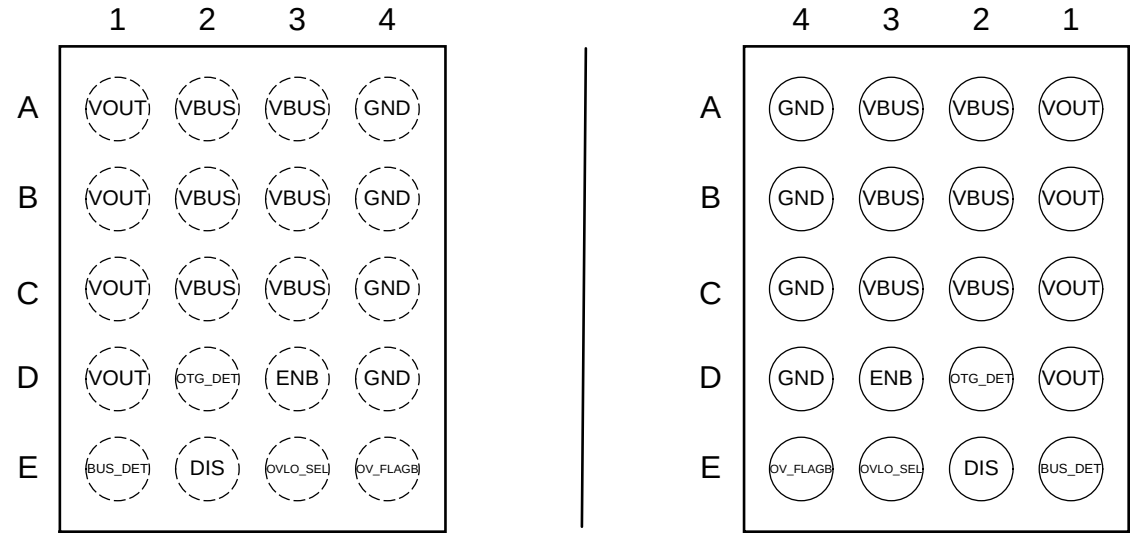
Features

- 6A Continuous Current Capability
- Typical RON: 9mΩ N-Channel MOSFET
- VIN Operating Range: 2.8V to 28V
- Overvoltage Lockout : OVLO=21.9V(OVLO_SEL=HIGH) / 12.4V(OVLO_SEL=GND)
- Overvoltage-Protection Response Time: 50ns(MAX)
- Startup Debounce Time: 15ms(TYP)
- Internal Thermal-Shutdown Protection
- Special OTG mode
- Surge Immunity to ±200V
- Active Discharge Path at VBUS
- ESD Protected(HBM):±4KV
- Small WLCSP20 Package (ball pitch=0.4mm)

Application

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

Pin Configuration

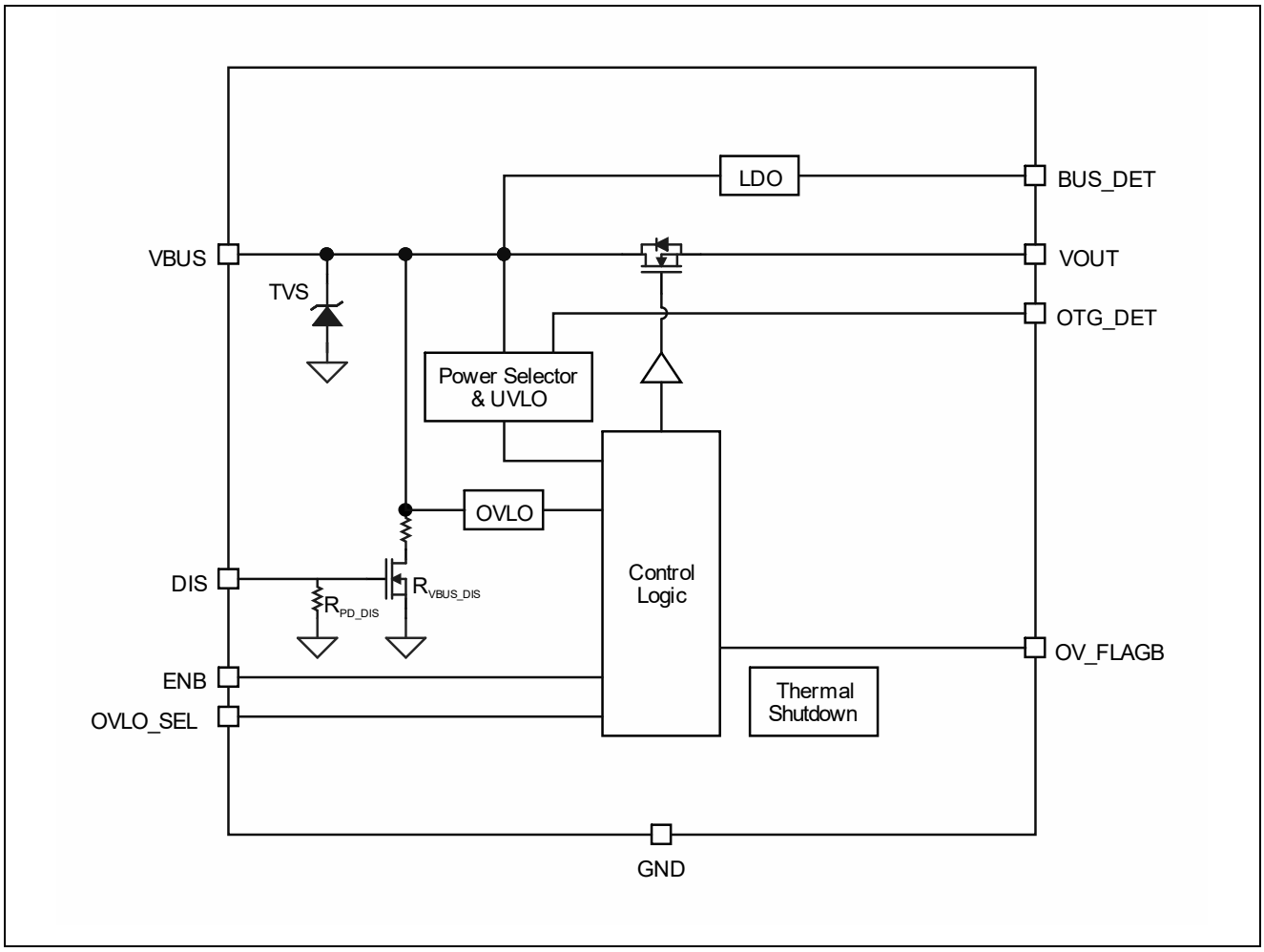


Top View Bottom View

Pin Function

Pin	Name	Description
E4	OV_FLAGB	Open-drain type signal indicating the OV state. (An external pull-up resistor is required)
A4, B4, C4, D4	GND	Ground. Connect GND pins together for proper operation.
A2~A3, B2~B3, C2~C3	VBUS	Voltage Input. Connect VBUS pins together for proper operation.
A1, B1, C1, D1	VOUT	Output Voltage. Output of internal switch. Connect VOUT pins together for proper operation.
D3	ENB	Enable signal for VBUS-VOUT path (Active Low) (An internal 1-MΩ pull-down resistor is integrated)
E2	DIS	Enable signal for active discharge path at VBUS (Active High) (An internal 1-MΩ pull-down resistor is integrated)
E3	OVLO_SEL	Selection of OVLO threshold (An internal 1-MΩ pull-down resistor is integrated) : OVLO_SEL = LOW → OVLO threshold = 12.4 V (typ) : OVLO_SEL = HIGH → OVLO threshold = 21.9 V (typ)
D2	OTG_DET	Power supply for charge pump circuit during startup in OTG mode.
E1	BUS_DET	Always on LDO output powered by VBUS.

Block Diagram



Functional Description

The OVP switch with overvoltage protection feature a low 9mΩ(TYP) on-resistance(RON) internal FET and protect low-voltage systems against voltage faults up to 28VDC. If ENB are in the logic low state, when the input voltage(VBUS) exceeds 12.4V(OVLO_SEL=LOW)/21.9V(OVLO_SEL=HIGH), the internal FET is quickly turned off to prevent damage to the protected downstream components. If ENB is in the logic high state, ET9668 will be shutdown immediately. The OVP switch features an open-drain output OV_FLAGB, when VUVLO<VBUS<VOVLO and the switch is ON, OV_FLAGB will be in high-impedance to indicate a good power input, otherwise it will be driven low.

The internal FET turns off when the junction temperature exceeds +145ºC(TYP). The device exits thermal shutdown after the junction temperature cools by 20ºC(TYP). The state of OV_FLAGB is not affected by over-temperature protection.

VBUS Active Discharge

There is an active discharge path at VBUS pin. It is used to satisfy the PD compliance. This function only can be controlled by DIS pin. When set DIS to High state, VBUS active discharge enable, and the VBUS pin will be connected to GND with a 550Ω resistor. When set DIS to low state, VBUS active discharge disable.

OTG Mode

ET9668 uses OTG_DET pin to control OTG mode. When OTG_DET is low, the chip works as a OVP switch. When a high voltage is applied to the OTG_DET pin(VOTG_DET>VOTG_DET_UVLO), the chip enters the OTG mode. At this time, the internal charge pump of the chip is turned on, and the switch MOSFET between VOUT and VBUS is turned on.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 1μF or lager must be placed between the VBUS and GND pins.

Output Capacitor

A 1μF or lager capacitor should be placed between the VOUT and GND pins.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Min	Max	Unit
V_{BUS}	VBUS to GND		-0.3	29	V
V_{OUT}	VOUT to GND		-0.3	See (NOTE1)	V
V_{BUS_DET}	BUS_DET to GND		-0.3	6	V
V_{ENB}, V_{OTG_DET}, V_{DIS}, V_{OV_FLAGB}, V_{OVLO_SEL}	ENB, OTG_DET, DIS, OV_FLAGB, OVLO_SEL to GND		-0.3	6	V
I_{SW1}	Maximum Continuous Current of switch VBUS-VOUT at Room Temp			6	A
I_{SW2}	Maximum Peak Current of switch VBUS-VOUT (5ms)			12	A
I_{BUS_DET}	Continuous BUS_DET current			20	mA
P_D	Power Dissipation at T_A= +25°C			1700	mW
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_A	Operating Temperature Range		-40	+85	°C
T_{SOLDER}	Soldering Temperature (reflow)			+260	°C
T_J	Junction Temperature			+150	°C
ESD	IEC 61000-4-2 System Level ESD	Air Discharge	±15.0		kV
		Contact Discharge	±8.0		
	Human Body Model, per JEDEC JS-001-2012	All Pins	±4.0		
	Charged Device Model, per JESD22-C101	All Pins	±1.5		
Surge	IEC 61000-4-5, Surge Protection	VBUS	-200	+200	V

NOTE1: 28V or VBUS+0.3V, whichever is smaller.

Electrical Characteristics

Unless otherwise noted, V_{BUS}=2.8V to 28V, T_A=-40°C to 85°C, typical values are at V_{BUS}=5V I_{VBUS}≤2A, C_{VBUS}=1uF and T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
TVS Characteristics						
V_{RW}	Reverse Working Voltage				28	V
V_{BR}	Breakdown Voltage	I_T=1mA	30	32	34	V
I_{PP}(1)	Peak Pulse Current	t_P=8/20μs	80		100	A
V_C(1)	Clamping voltage	V_{BUS}=5V, V_{ENB}=LOW, C_{VBUS}= C_{VOUT}=1uF, I_{OUT}=1A, +200V Surge	33	37	40	V
I_{PP_NEG}(1)	Reverse Peak Pulse Current	t_P=8/20μs(-200V surge) , T_A=25°C	-100		-80	A
V_{C_NEG}(1)	Reverse Clamping Voltage	I_{PP}= -100A, t_P=8/20μs, T_A=25°C	-6	-3	-1	V
V_F	Forward Voltage	I_F=10mA	0.2	0.6	0.8	V
Basic Operation						
V_{BUS}	Input Voltage		2.8		28	V
I_{Q_PWR}	Power Input Quiescent Current	V_{BUS} = 5 V, V_{ENB} = LOW	65	95	140	μA
		V_{BUS} = 5 V, V_{ENB} = HIGH	60	90	140	
I_{IN_OVLO}	OVLO Supply Current	V_{BUS} = 15 V, V_{OUT} = 0 V, V_{ENB} = LOW, V_{OVLO_SEL} = GND	85	115	160	μA
		V_{BUS} = 23 V, V_{OUT} = 0 V, V_{ENB} = LOW, V_{OVLO_SEL} = HIGH	95	130	180	
V_{BUS_UVLO}	Under voltage protect of VBUS	V_{BUS} Rising, T_A = -40 °C to 85 °C	2.3	2.5	2.7	V
		V_{BUS} Falling, T_A = -40 °C to 85 °C	2.2	2.35	2.5	
T_{SHDN}	Thermal Shutdown(1)		130	145	160	°C
T_{SHDN_HYS}	Thermal-shutdown Hysteresis(1)		10	20	30	°C
VBUS Active Discharge(DIS)						
R_{VBUS_PD}	VBUS Discharge Resistance	V_{BUS} = 5 V, V_{DIS} = 1.8V	300	550	1200	Ω
$T_{VBUS\_DIS\_ON}$(1)	VBUS Discharge ON Delay Time	V_{OUT} = 5 V ,Time from V_{DIS} = HIGH to Discharge path ON		0.5	3	μs
$T_{VBUS\_DIS\_OFF}$(1)	VBUS Discharge OFF Delay Time	V_{OUT} = 5 V ,Time from V_{DIS} = LOW to Discharge path OFF		1	3	μs

Electrical Characteristics(Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{VBUS_DIS}	VBUS Discharge Time	V_{OUT} = 5V, C_{BUS}=1uF, V_{DIS}=V_{ENB}=LOW to HIGH and remove V_{OUT} voltage at the same time, Time from V_{BUS}=5V to 0.5V		1.5	5	ms
VBUS to VOUT Switch						
V_{BUS_OVLO}	VBUS Over-Voltage Lockout Trip Level	V_{BUS} Rising, V_{OVLO_SEL} = GND T_A = -40 °C to 85 °C	12.1	12.4	12.7	V
		V_{BUS} Falling, V_{OVLO_SEL} = GND T_A = -40 °C to 85 °C	11.6	12.1	12.6	
		V_{BUS} Rising, V_{OVLO_SEL} = HIGH T_A = -40 °C to 85 °C	21.5	21.9	22.3	
		V_{BUS} Falling, V_{OVLO_SEL} = HIGH T_A = -40 °C to 85 °C	21.0	21.5	22.2	
R_{ON}	On-Resistance of Switch V_{BUS}-V_{OUT}	V_{BUS} = 5V, I_{OUT} = 0.2A, T_A =25°C	6	9	12	mΩ
		V_{BUS} = 12V, I_{OUT} = 0.2A, T_A=25°C	6	9	12	
		V_{BUS} = 21V, I_{OUT} = 0.2A, T_A =25°C	6	9	12	
t_{DEB_VOUT}	V_{BUS} Debounce Time	Time from V_{BUS_UVLO} ≤ V_{BUS} < V_{BUS_OVLO} to V_{OUT} = 0.1 x V_{BUS}		15	20	ms
t_{ON_VOUT}	Switch Turn-On Time	R_L = 100 Ω, C_{OUT} = 1μF, Time from V_{OUT} = 0.1 x V_{BUS} to 0.9 x V_{BUS}		1	3	ms
t_{DOFF_VOUT}(1)	Switch Turn-Off Response Time	R_L=100Ω, C_{OUT}=1μF, V_{OVLO_SEL}=LOW, Time from V_{BUS} = V_{BUS_OVLO} to V_{OUT} stop rising. Measured when V_{BUS} rises from 0 V to 15 V at 14 V/1μs			50	ns
		R_L = 100Ω, C_{OUT} = 1μF, V_{OVLO_SEL} = HIGH, Time from V_{BUS} = V_{BUS_OVLO} to V_{OUT} stop rising. Measured when V_{BUS} rises from 0 V to 25 V at 14 V/1μs			50	
OTG Mode Operation						
$V_{OTG\_DET\_UVLO}$	OTG_DET Under-Voltage Lockout Trip Level	OTG_DET Rising, V_{OUT}=2V, V_{ENB} = Low, T_A = -40 °C to 85 °C	2.80	2.95	3.10	V
		OTG_DET Falling, V_{OUT}=2V, V_{ENB} = Low, T_A = -40 °C to 85 °C	2.65	2.80	2.95	V

Electrical Characteristics(Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{IN\_OTG\_DET}$	Input Supply Current at OTG_DET	V_{OTG_DET} = 0V, V_{OUT} = 0V, V_{ENB} = LOW, VBUS = Open, T_A = -40 °C to 85 °C			1	uA
		V_{OTG_DET} = 5V, V_{OUT} = 0V, V_{ENB} = LOW, VBUS = Open, T_A = -40 °C to 85 °C	30	60	90	
		V_{OTG_DET} = 4.5 V, V_{OUT} = 5V, V_{ENB} = LOW, VBUS = Open, T_A = -40 °C to 85 °C			1	
		V_{OTG_DET} = 0 V, V_{OUT} = 5V, V_{ENB} = LOW, VBUS = Open, T_A = -40 °C to 85 °C			1	
R_{ON_OTG}	OTG On Resistance	V_{OUT} = 5 V, I_{BUS} = -200mA, T_A = 25 °C	6	9	12	mΩ
t_{DON_OTG}	OTG_DET Startup Delay Time	Time from OTG_DET ≥ $V_{OTG\_DET\_UVLO}$ to Charge Pump Output Enable, TA = -40 °C to 85 °C	0.05		1	ms
BUS_DET						
V_{BUS_DET}	BUS_DET Regulation Output Voltage	V_{BUS}=5V, I_{BUS_DET}=0mA, C_{BUS_DET}=1uF	3.8	4.0	4.2	V
		V_{BUS}=21V, I_{BUS_DET}=0mA, C_{BUS_DET}=1uF	3.8	4.0	4.2	V
		V_{BUS}=5V, I_{BUS_DET}=10mA, C_{BUS_DET}=1uF	3.8	4.0	4.2	V
		V_{BUS}=21V, I_{BUS_DET}=10mA, C_{BUS_DET}=1uF	3.8	4.0	4.2	V
$T_{START\_BUS\_DET}$	BUS_DET Startup Time	Time from VBUS≥V_{BUS_UVLO} to BUS_DET=10% of target value	20	30	40	ms
Digital Signals						
$V_{OV\_FLAGB\_OL}$	OV_FLAGB Output LOW Voltage	V_{IO} (Pull up voltage)=1.8 V, R_{PU} = 100 kΩ			0.36	V
$T_{OV\_FLAGB\_DELAY}$ (1)	OV_FLAGB Assertion Delay Time	V_{ENB}=LOW, Time from VBUS ≥ V_{BUS_OVLO} to OV_FLAGB assertion			3	us
		V_{ENB}=HIGH, Time from VBUS ≥ V_{BUS_OVLO} to OV_FLAGB assertion			3	us

Electrical Characteristics(Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{OV\_FLAGB\_REC}$	OV_FLAGB Recovery Debounce Time	V_{ENB}=LOW, Time from $V_{BUS} \le V_{BUS\_OLVO}$ to OV_FLAGB de-assertion(2)	16			ms
		V_{ENB}=HIGH, Time from $V_{BUS} \le V_{BUS\_OLVO}$ to OV_FLAGB de-assertion	100	200	300	us
V_{IH1}	Logic Enable HIGH Voltage for ENB, OVLO_SEL, DIS	VBUS operating range, V_{IO}=1.2V/1.8V	0.84			V
V_{IL1}	Logic Enable LOW Voltage for ENB, OVLO_SEL, DIS	VBUS operating range, V_{IO}=1.2V/1.8V			0.54	V
R_{PD}	Internal Pull-Down Resistor at ENB, DIS, OVLO_SEL		0.7	1	1.6	MΩ

Notes:

1： This parameter is guaranteed by design and characterization.

2： It is required that OV_FLAGB Recovery Debounce Time should be longer than VBUS debounce time + Switch Turn-on delay.

Sequence Diagram and Waveform

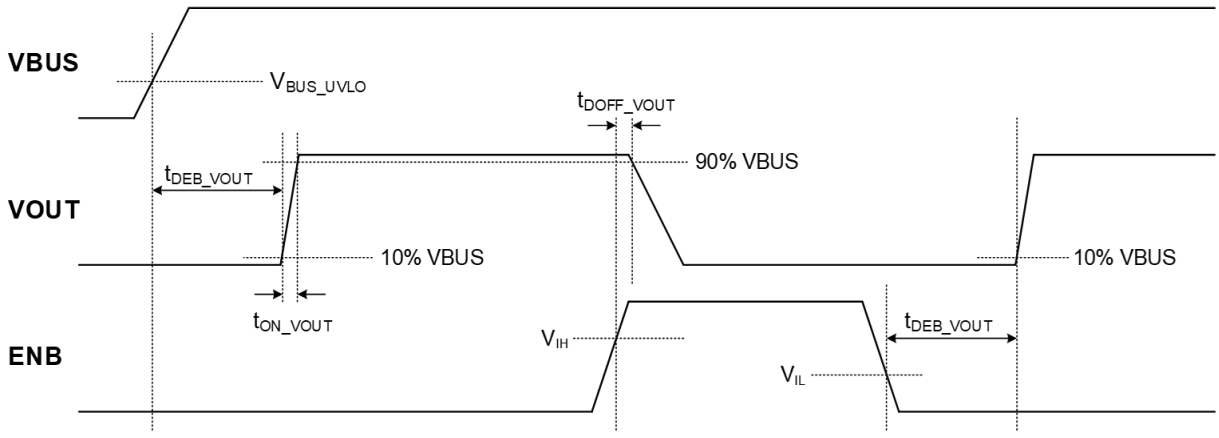


Figure1. VBUS-VOUT Power Up Operation

Sequence Diagram and Waveform(Continued)

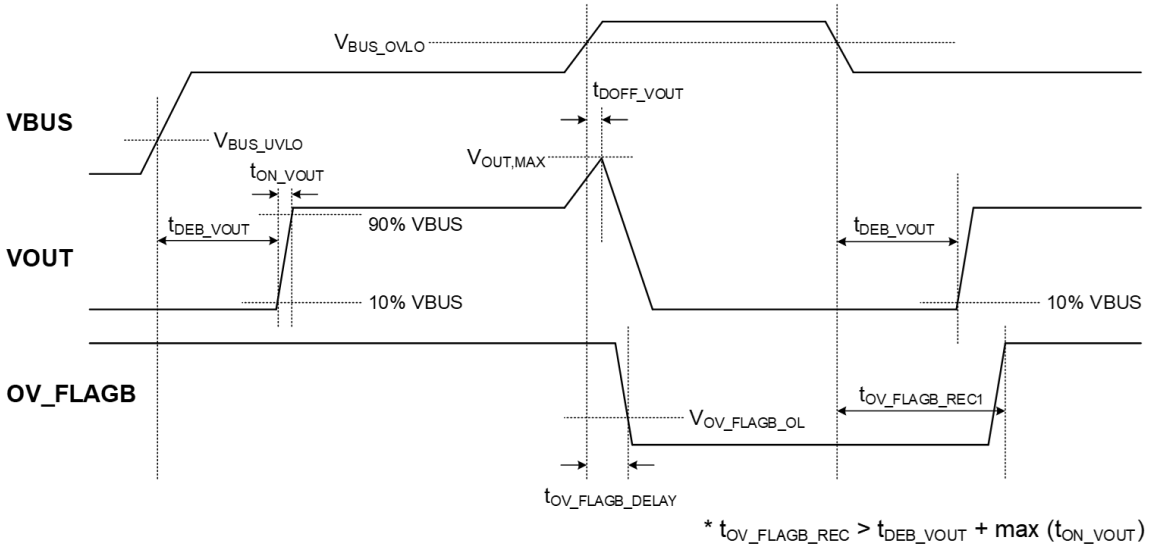


Figure2. VBUS OVLO Operation (ENB=LOW, Single OVLO event)

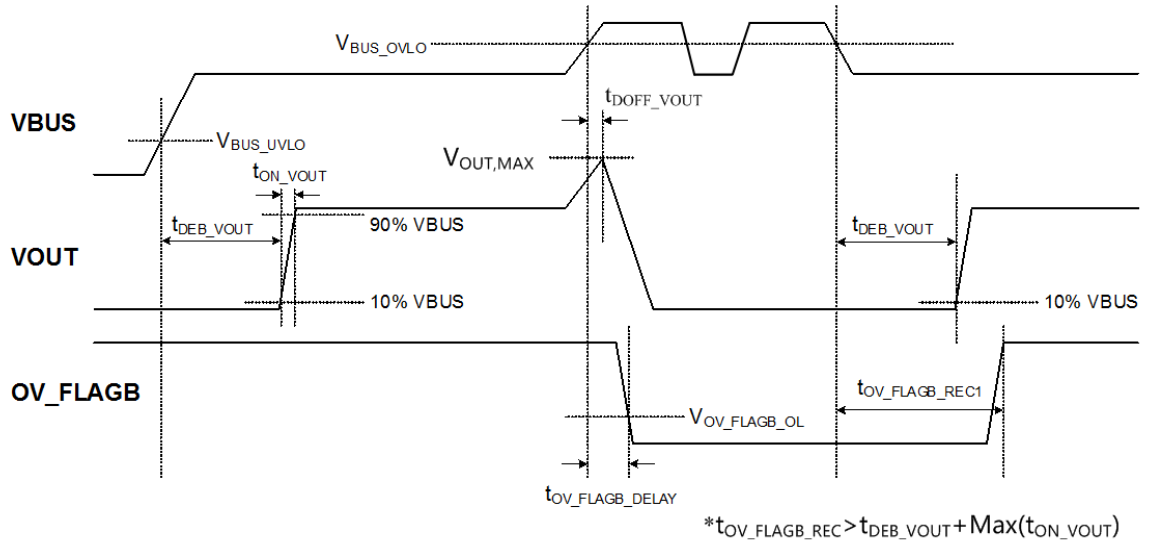


Figure3. VBUS OVLO Operation
(ENB=LOW, Two consecutive OVLO events, Time interval ≤ tDEB_VOUT)

Sequence Diagram and Waveform(Continued)

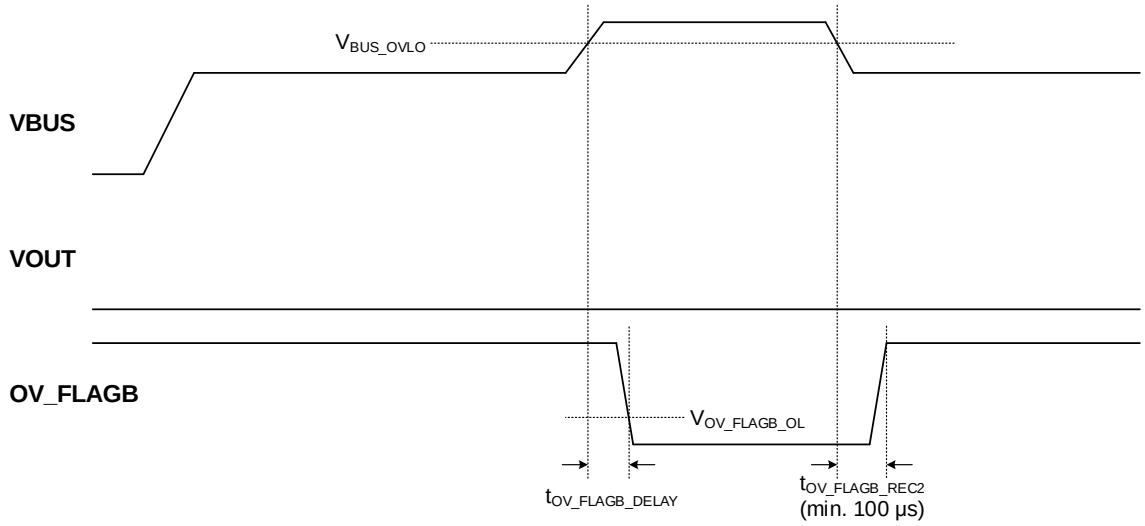


Figure4. VBUS OVLO Operation (ENB=High)

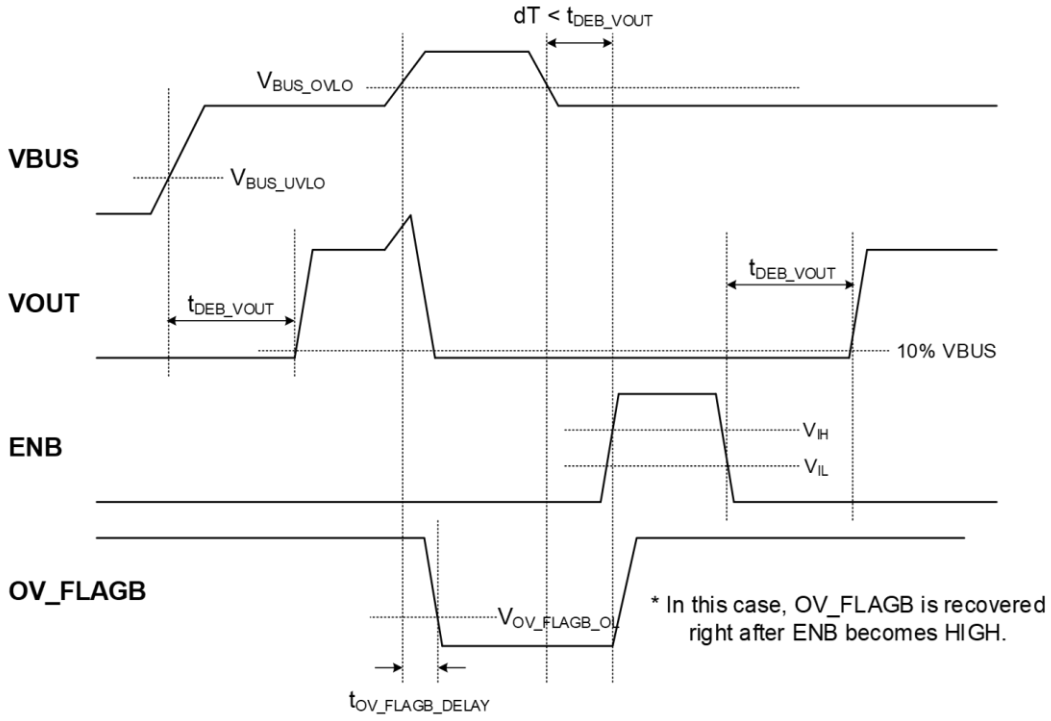


Figure5. VBUS OVLO Operation (ENB=Low -> High -> Low)

Sequence Diagram and Waveform(Continued)

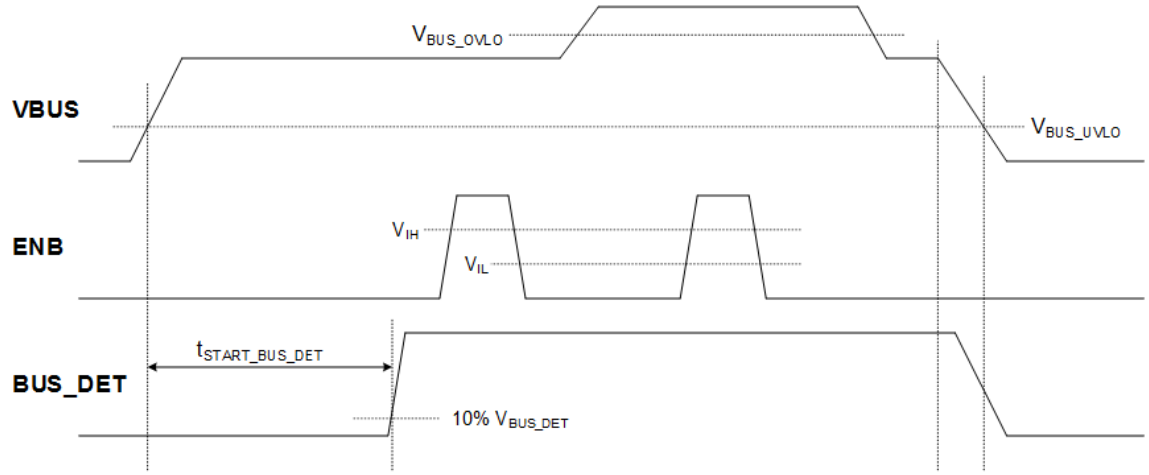


Figure6. VBUS_DET Operation

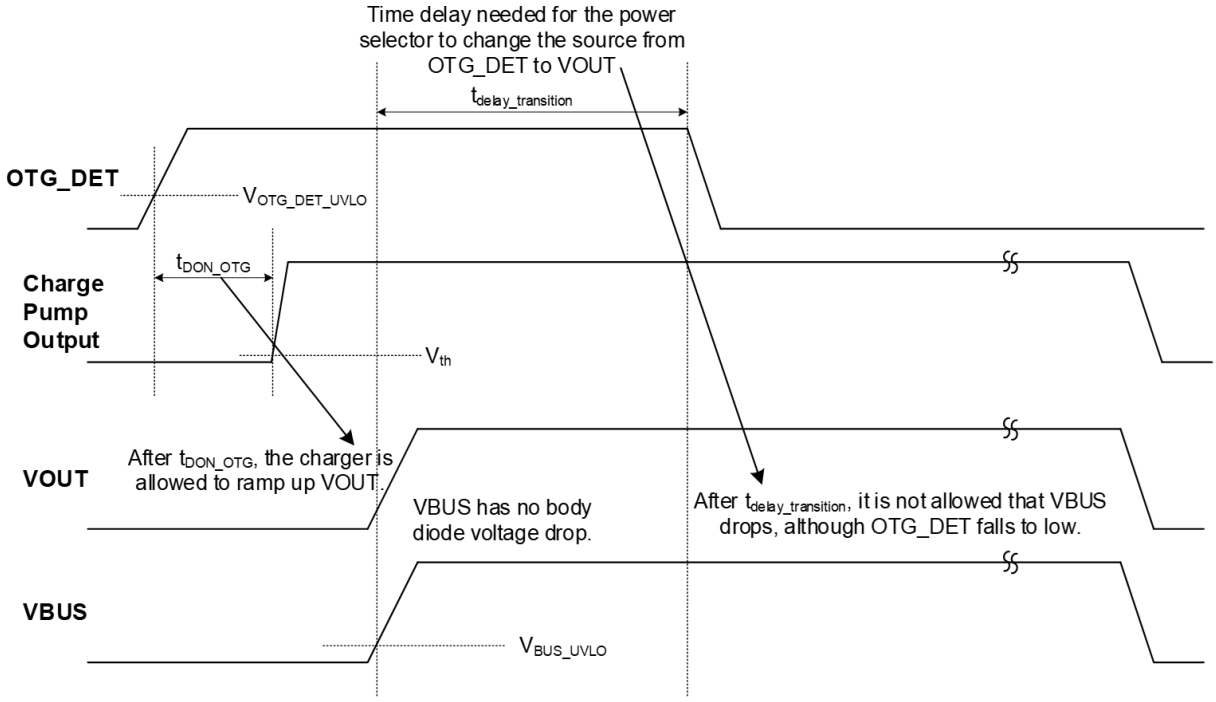


Figure7. OTG Mode: Using OTG_DET Function

Note: t_{DON_OTG} = Max. 1ms / $t_{delay\_transition}$ = Max. 20ms

Sequence Diagram and Waveform(Continued)

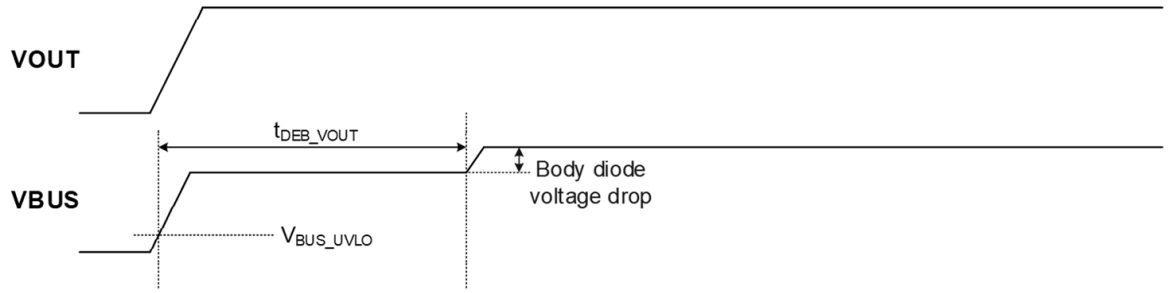


Figure8. OTG Mode: Not Using OTG_DET Function (When OTG_DET keeps 0V)

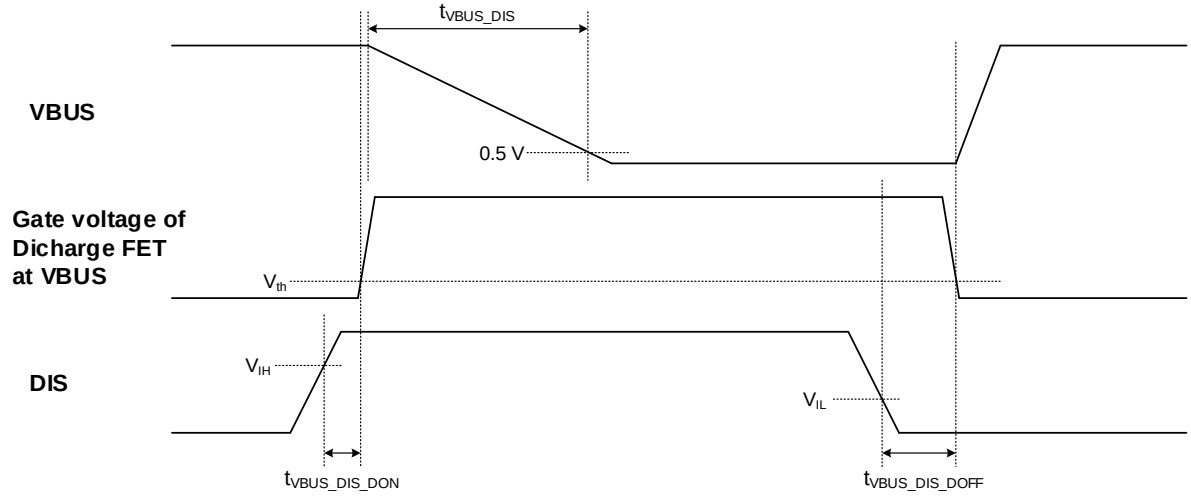
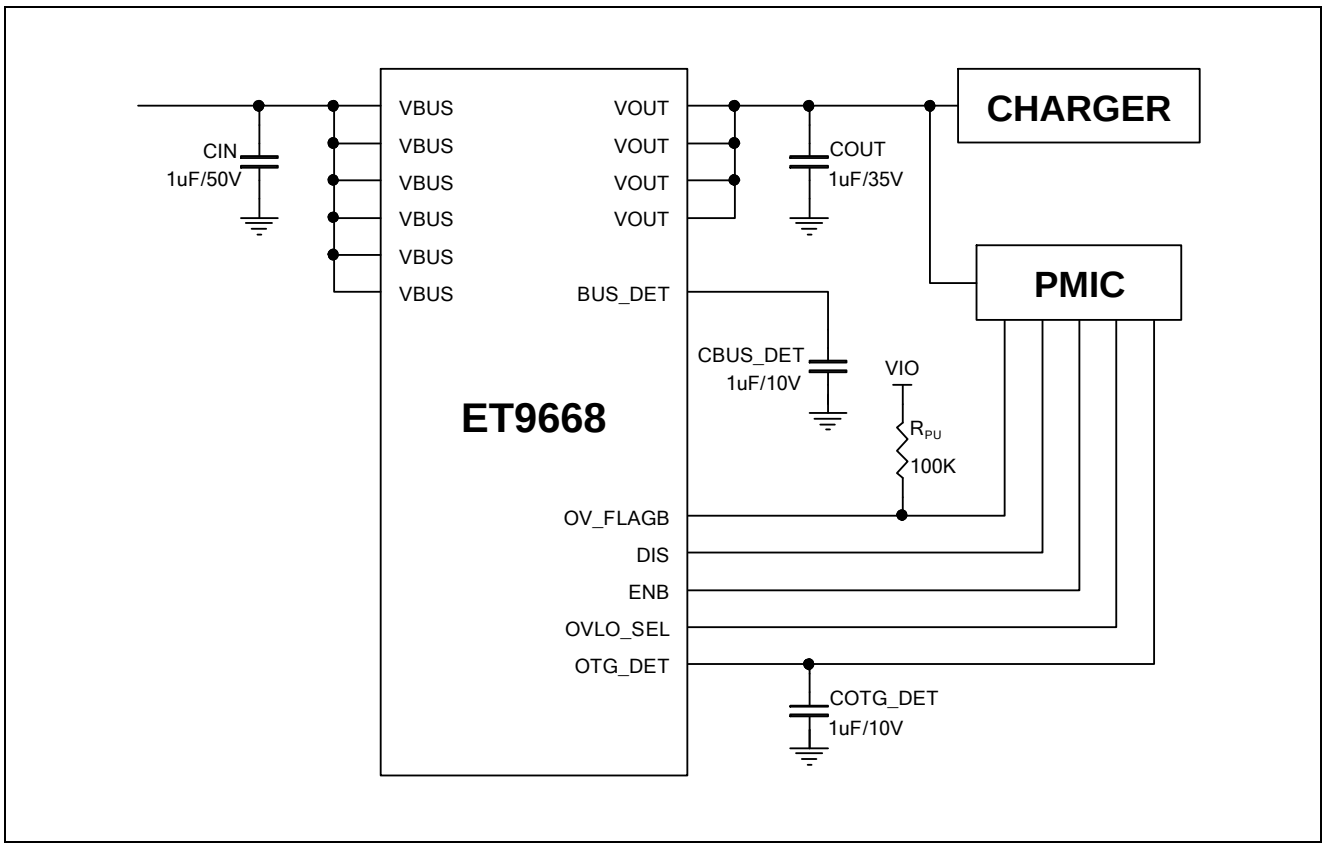


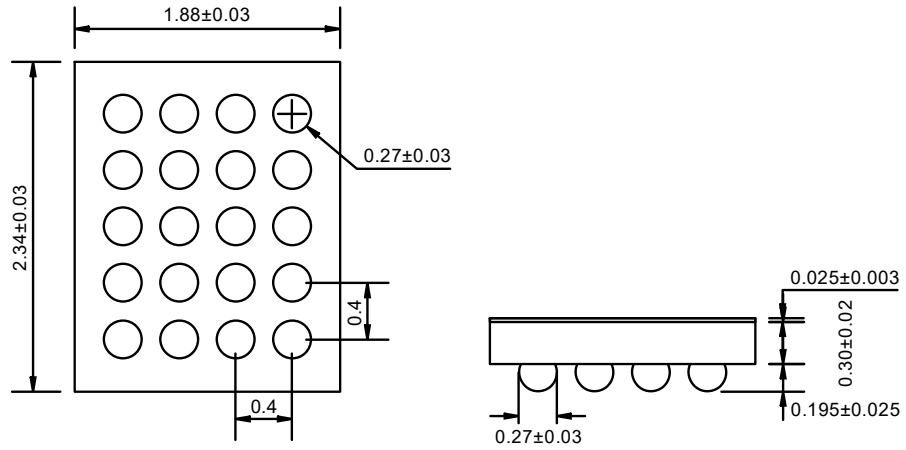
Figure9. Active VBUS Discharge Function

Application Circuits

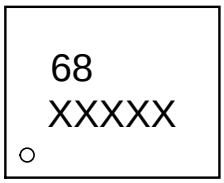


Note*: This electric circuit only supplies for reference.

Package Dimension



Marking



68 = Part NO.

XXXXX = Tracking NO.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-08-06	Preliminary Version	Wum	Wum	Liujy
1.0	2022-10-26	Offered Version	Wuhs	Wum	Liujy
1.1	2023-01-06	Update AMR	Wuhs	Wum	Liujy