High-Current Over-voltage Protectors with Adjustable OVLO

General Description

ET9553L can disconnect the systems from its output pin(OUT) in case wrong input operating conditions are detected. The input voltage can be up to 28V. The internal overvoltage threshold (OVLO) is 5.95V, and also can be adjusted by external resistors. ET9553L has internal Thermal-Shutdown Protection function.

The device is packaged in advanced full-Green compliant Wafer Level Chip Scale Packaging (WLCSP12).

Features

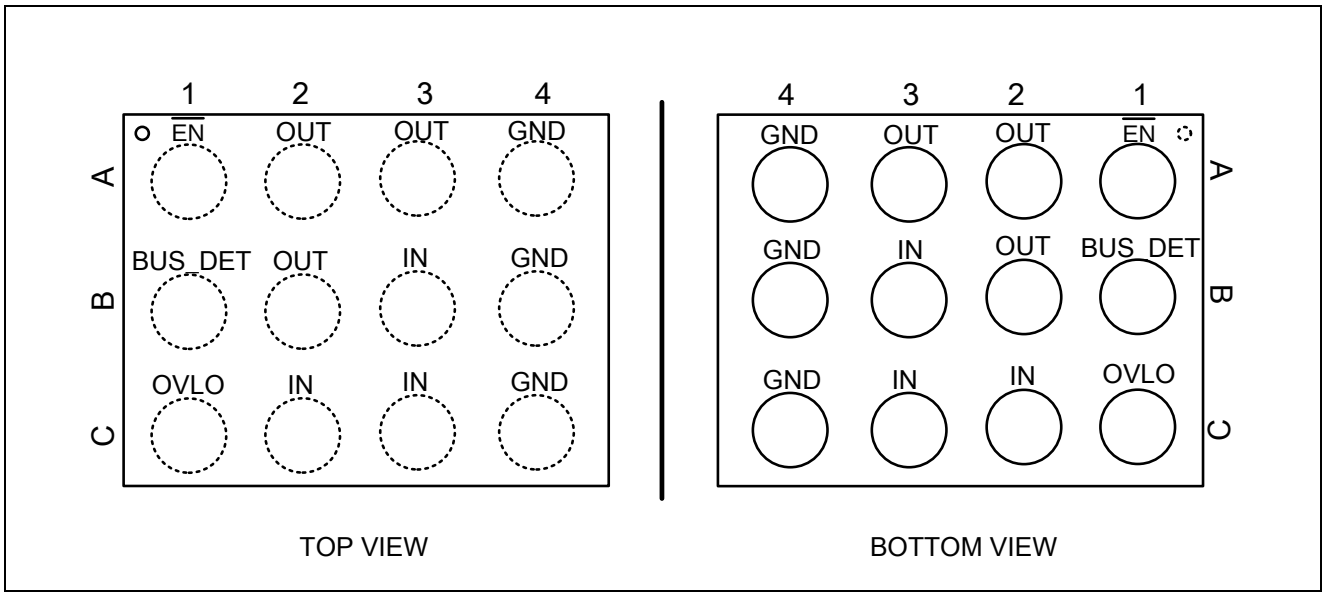
- 4.8A Continuous Current Capability
- Typical R_{ON}: 35mΩ N-Channel MOSFET
- V_{IN} Operating Range: 2.5V to 28V
- Overvoltage Lockout: V_{OVLO}=5.95V(TYP)
- Overvoltage-Protection Response Time：50ns(TYP)
- OVLO Threshold Range: +4V to +24V
- Startup Debounce Time:21ms(TYP)
- Internal Thermal-Shutdown Protection
- Surge immunity to ±100V
- ESD Protected(HBM) to ±4KV
- Pat No. and Package

Part No.	Package
ET9553L	WLCSP12 (1.58mm×1.18mm, ball pitch=0.4mm)

Application

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

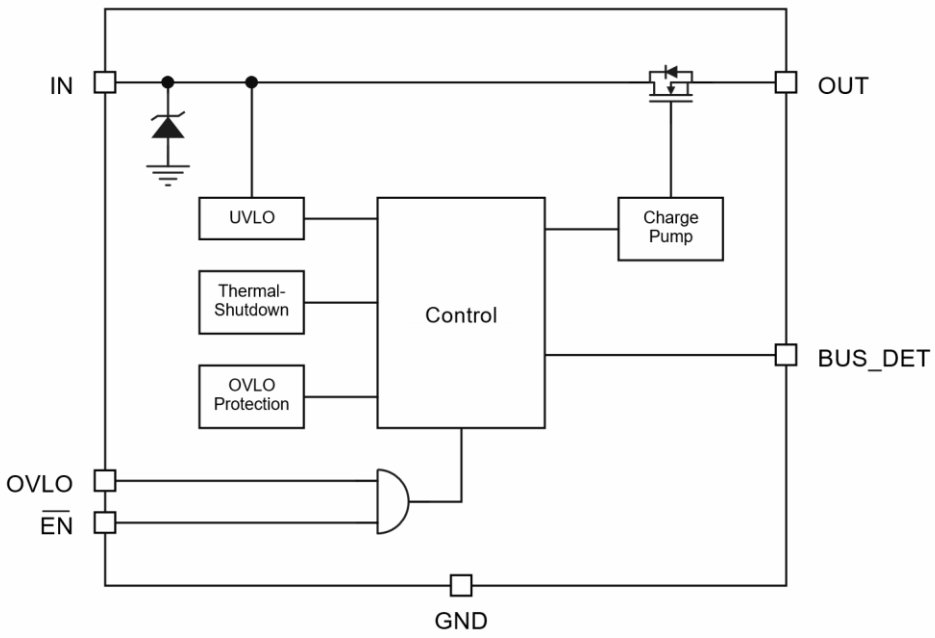
Pin Configuration



Pin Function

Pin	Name	Description
A1	$\overline{EN}$	Device Enable. Active low.
A2,A3,B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
A4,B4,C4	GND	Ground. Connect GND pins together for proper operation.
B1	BUS_DET	Regulation output of VBUS.
B3,C2,C3	IN	Voltage Input. Connect IN pins together for proper operation.
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.

Block Diagram



Functional Description

The OVP switch with overvoltage protection feature a low 35mΩ(TYP) on-resistance(R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 28V_{DC}. If $\overline{EN}$ is in the logic low state, when the input voltage(V_{IN}) exceeds 5.95V, the internal FET is quickly turned off to prevent damage to the protected downstream components. If $\overline{EN}$ is in the logic high state. The ET9553L will disables the protect low-voltage system.

Over-voltage Protection

When input (OVLO) is set lower than 0.2V. The overvoltage protection threshold is 5.95V.

The overvoltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

$$\mathbf{V_{IN\_OVLO} = V_{OVLO\_TH} \times (1+R1/R2)}$$

Note: V_{OVLO_TH} = 1.2V(TYP)

Thermal Shutdown

The internal FET turns off when the junction temperature exceeds +150ºC (TYP). The device exits thermal shutdown after the junction temperature cools by 20ºC (TYP).

USB OTG Operation

If V_{IN}=0V and OUT is supplied by OTG voltage, the body diode of the OVP switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When place $\overline{EN}$ pin in the logic low state and V_{IN}>V_{UVLO}, internal charge pump begins to open the OVP switch after debounce time. After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum. When place

$\overline{EN}$ pin in the high state, the OVP switch will not turn ON unless $\overline{EN}$ pin is pulled LOW, the high forward voltage drop of 0.7V and consequent high power dissipation will remain. It is highly recommended to place $\overline{EN}$ pin in the logic low state in all OTG applications.

Please note in OTG mode, under no circumstance should any load, or any voltage be connected to BUS_DET.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into load capacitor or short-circuit, a capacitor 1μF or lager must be placed between the IN and GND pins.

Output Capacitor

A 1μF or lager capacitor should be placed between the OUT and GND pins.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters			Min	Max	Unit
V_{IN}	VIN to GND			-2.0(1)	29	V
V_{OUT}	VOUT to GND			-0.3	28	V
V_{OVLO}	OVLO to GND			-0.3	7	V
$V_{/EN}$	$\overline{EN}$ to GND			-0.3	7	V
V_{BUS_DET}	BUS_DET to GND			-0.3	10	V
I_{SW1}	Maximum Continuous Current of switch IN-OUT				4.8	A
I_{SW2}	Maximum Peak Current of switch IN-OUT(10ms)				8	A
P_D	Power Dissipation at T_A= +25°C				1.4	W
T_{STG}	Storage Junction Temperature			-65	+150	°C
T_A	Operating Temperature Range			-40	+85	°C
T_{SOLD}	Soldering Temperature (reflow).				+260	°C
T_J	Max Junction Temperature				+150	°C
ESD	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	15.0		kV
			Contact Discharge	8.0		
		Human Body Model, JEDEC JS-001-2012	All Pins	>4.0		
		Charged Device Model, JESD22-C101	All Pins	>1.5		
Surge		IEC 61000-4-5, Surge Protection	VBUS	±100		V

Note1: Pulsed, 50ms maximum non-repetitive.

Electrical Characteristics

Unless otherwise noted, V_{IN}=2.5V to 28V, T_A=-40°C to 85°C, Typical values are at V_{IN}=5V, I_{IN}≤2A, C_{IN}=1μF and T_A=25°C.

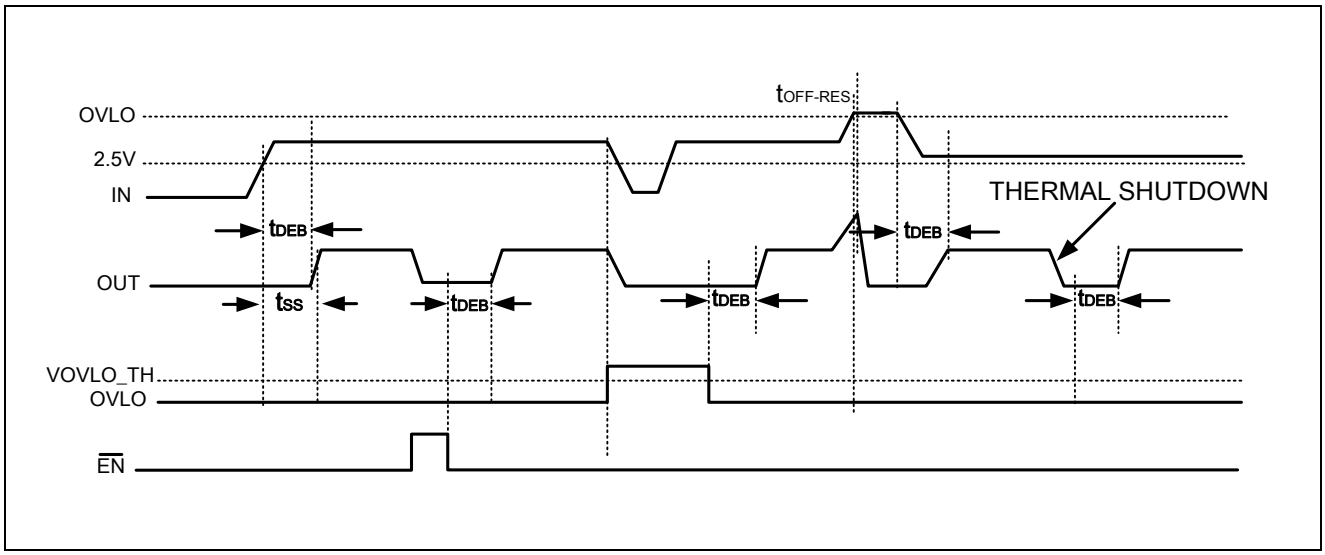
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
TVS Characteristics						
V_{BR}	Reverse Breakdown Voltage	I_T=10mA, T_A=25°C	29	32	36	V
I_{PP}	Peak Pulse Current(2)	t_p=8/20μs(+100V), T_A=25°C	25	32.5	44	A
V_C	Clamping Voltage(2)	I_{PP}=32.5A, t_p=8/20μs, T_A=25°C	22	35	45	V
I_{PP_NEG}	Reverse Peak Pulse Current(2)	t_p=8/20μs(-100V surge) , T_A=25°C	-40	-48.5	-55	A
V_{C_NEG}	Reverse Clamping Voltage(2)	I_{PP}=-48.5A, t_p=8/20μs, T_A=25°C	-1	-3	-6	V
V_F	Forward Voltage	I_F=10mA, T_A=25°C	0.2	0.6	0.9	V
Basic Operation						
V_{IN}	Input Voltage		2.5		28	V
I_{IN}	V_{IN} Quiescent Current	V_{IN}=5V, $V_{/EN}$=0V, OUT floating	110	150	220	μA
I_{IN_OVLO}	OVLO Supply Current	V_{IN}=12V, $V_{/EN}$=0V, OUT floating	150	190	250	μA
R_{ON}	On-Resistance of Switch IN-OUT	V_{IN}=5.0V, I_{OUT}=1A, T_A=25°C	25	35	53	mΩ
V_{OVLO}	Overvoltage Protect of V_{IN}	V_{IN} Rising	5.90	5.95	5.99	V
	Overvoltage Protect hysteresis of V_{IN}		0.05	0.15	0.30	V
	Adjustable OVLO Threshold Range		4		24	V
V_{OVLO_TH}	OVLO Set Threshold		1.18	1.2	1.22	V
V_{OVLO_SELECT}	External OVLO Select Threshold		0.2		0.3	V
V_{DET1}	Regulation Output of BUS_DET	V_{IN}=5V, $V_{/EN}$=0V, I_{DET}=1mA and C_{BUS_DET}=1μF	4.8			V
V_{DET2}	Regulation Output of BUS_DET	V_{IN}=9V, $V_{/EN}$=0V, I_{DET}=10mA and C_{BUS_DET}=1μF	6	6.7	7.5	V
V_{UVLO}	Undervoltage Protect of VIN	V_{IN} Rising	1.7	2.0	2.5	V
		V_{IN} Falling	1.5	1.8	2.3	V
I_{OVLO}	OVLO Input Leakage Current	V_{OVLO}=V_{OVLO_TH}	-100		100	nA
V_{IH}	$\overline{EN}$ Input Logic High Voltage	V_{IN}=2.5V to 28V	1.4			V

Electrical Characteristics (Continued)

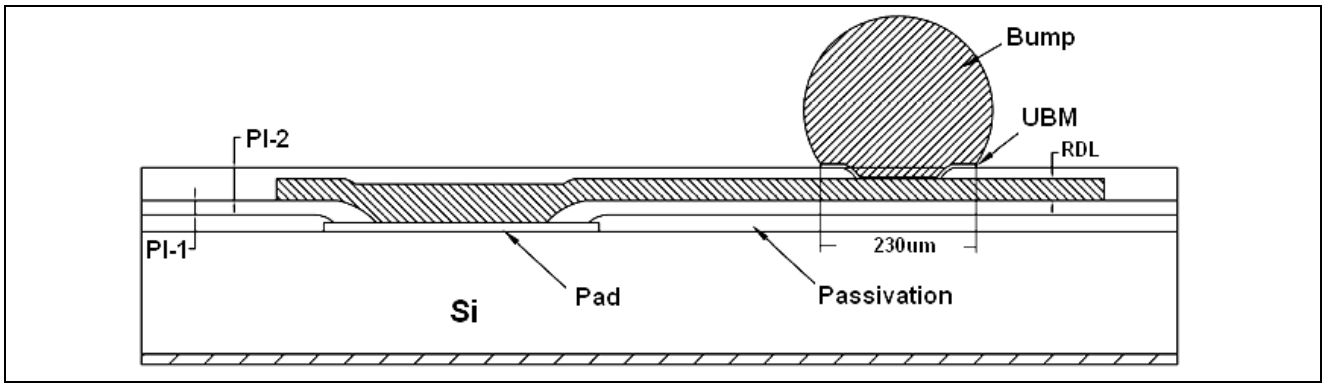
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IL}	$\overline{EN}$ Input Logic Low Voltage	V_{IN}=2.5V to 28V			0.3	V
T_{SHDN}	Thermal Shutdown(2)			150		°C
T_{SHDN_HYS}	Thermal-Shutdown Hysteresis(2)			20		°C
Dynamic Characteristics: see figure						
t_{DEB}	Debounce Time	Time from V_{UVLO}<V_{IN}< V_{OVLO} to V_{OUT}=10% of V_{IN}		21	32	ms
t_{SS}	Soft-Start time	Time from V_{UVLO}<V_{IN}< V_{OVLO} to V_{OUT}=90% of V_{IN}		23	35	ms
t_{OFF_RES}	Switch Turn-off Response Time(2)	R_L=100Ω, No C_L, V_{IN} > V_{OVLO} to V_{OUT} stop rising		50	80	ns

Note2: This parameter is guaranteed by design and characterization.

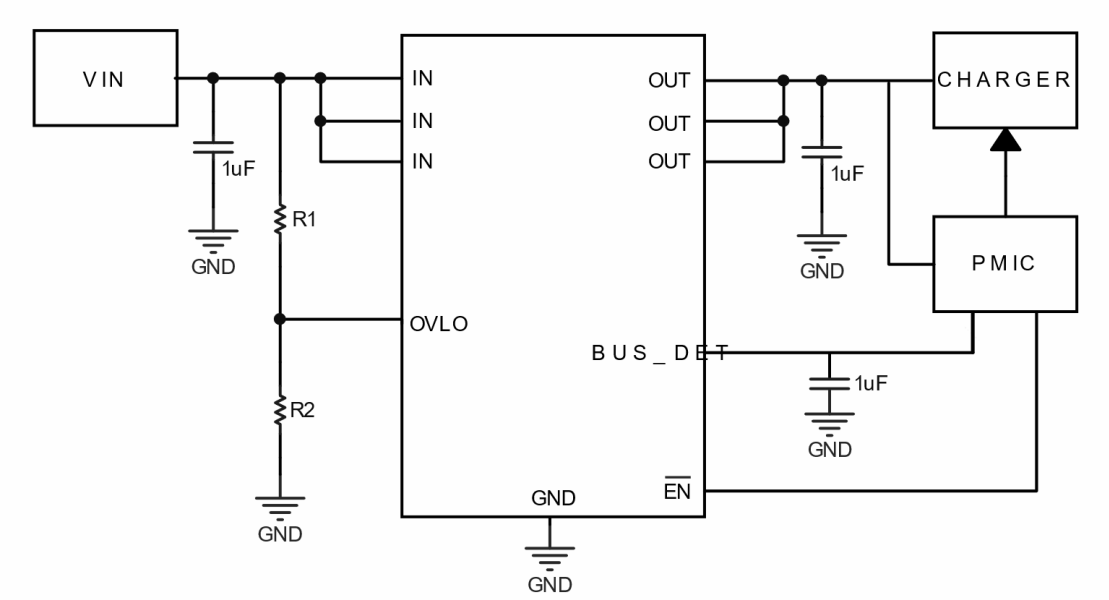
Timing Waveform



UBM Structure



Application Circuits

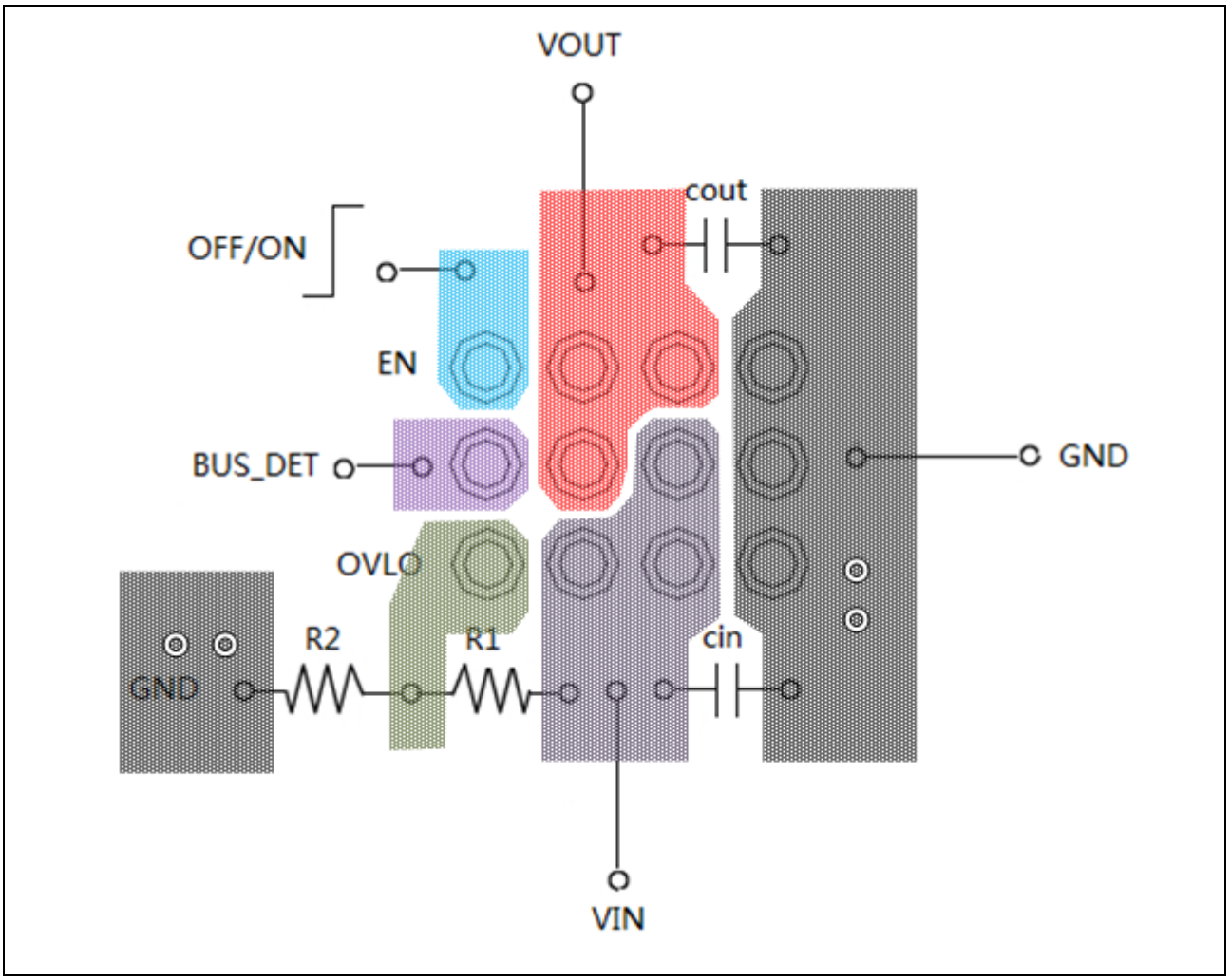


Note: R1 and R2 are only required for adjustable OVLO; otherwise connect OVLO to GND.

: This application circuit is for reference only.

Board Layout

ET9553L can be routed in a single layer PCB. PCB traces to IN, OUT, $\overline{EN}$, BUS_DET, OVLO and GND can be routed in the fashion shown in below picture.



1. If R1 and R2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.

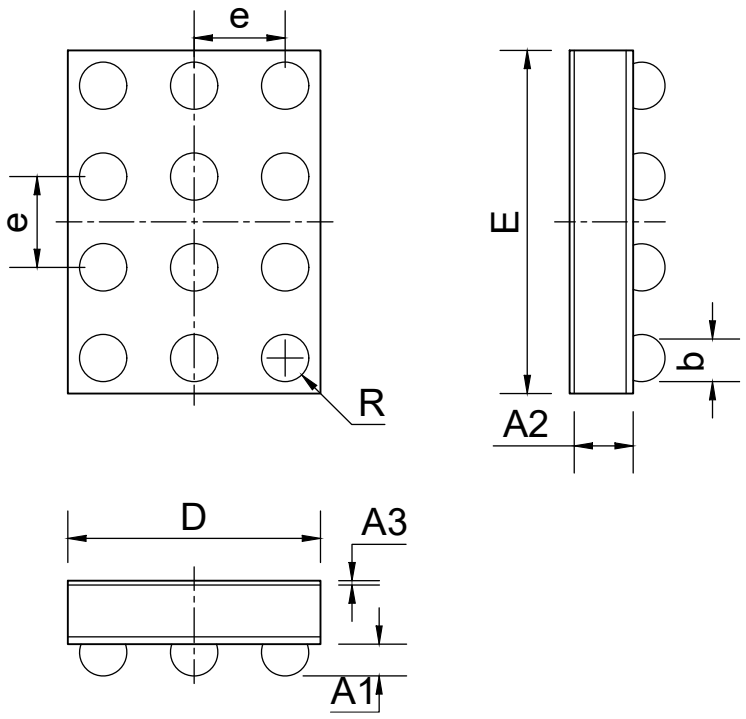
2. The decoupling capacitors per the recommended operating settings should be placed as close as possible to the ET9553L.

3. There should be a short path from the device ground pins to the system ground plane.This ensures best protection under ESD and surge transients.

4. If external TVS is used, IN pin routing passes through the TVS firstly, and then connect ET9553L.

Package Dimension

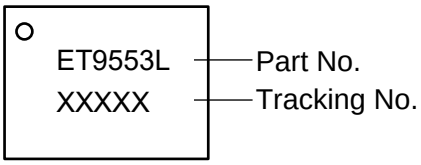
WLCSP12



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.18	0.20	0.22
A2	0.34	0.35	0.36
A3	0.018	0.025	0.032
b	0.24	0.27	0.30
D	1.13	1.18	1.23
E	1.53	1.58	1.63
e	0.40BSC		
R	0.24	0.27	0.30

Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0	2019-04-18	Preliminary Version	Wum	Wum	Liujy
1.0	2019-05-30	Original Version	Wum	Wum	Liujy
1.1	2019-06-10	Change I_{PP} max to 44A	Wum	Wum	Liujy
1.2	2020-04-01	Update package dimension	Wum	Wum	Liujy
1.3	2021-10-14	Add Marking	Wum	Wum	Liujy
1.4	2023-1-12	Update Typeset	Shibo	Wum	Liujy
1.5	2024-03-11	Update PCB Layout	Caojc	Wum	Liujy