USB Type-C Port Controller with USB-PD

General Description

The ET7303A is a USB Type-C and Power Delivery (PD) controller, which complies with USB Type-C™ 1.2 and Power Delivery (PD2.0) Specifications. The ET7303A supports Type-C Port Control interface (TCPCi).The ET7303A integrates a complete Type-C transceiver including the Type-C termination resistors, Rp and Rd, and enables the USB Type-C detection including attach and orientation.

The ET7303A integrates the physical layer of the USB BMC PD (Power Delivery) protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

Features

- PD-Compatible Dual-Role
- Support USB PD2.0 and Type-C™ Rev1.2
- CC Pin 28V Short-VBUS Circuit Protection
- VCONN Provider Path with Over-Voltage Protection and Programmable Over-Current Protection
- VCONN Path with Aided Discharge
- Current Capability Definition and Detection
- Cable Recognition and Alternate Modes Support
- Dead Battery and No Battery Support
- Low-Power Mode for Attach Detection
- BIST Mode Supported
- WLCSP9 Package
- MSL1 Level

Application

- Power Banks
- Tablets
- Notebooks
- Mobile Phones
- Monitors
- TVs

Pin Configuration

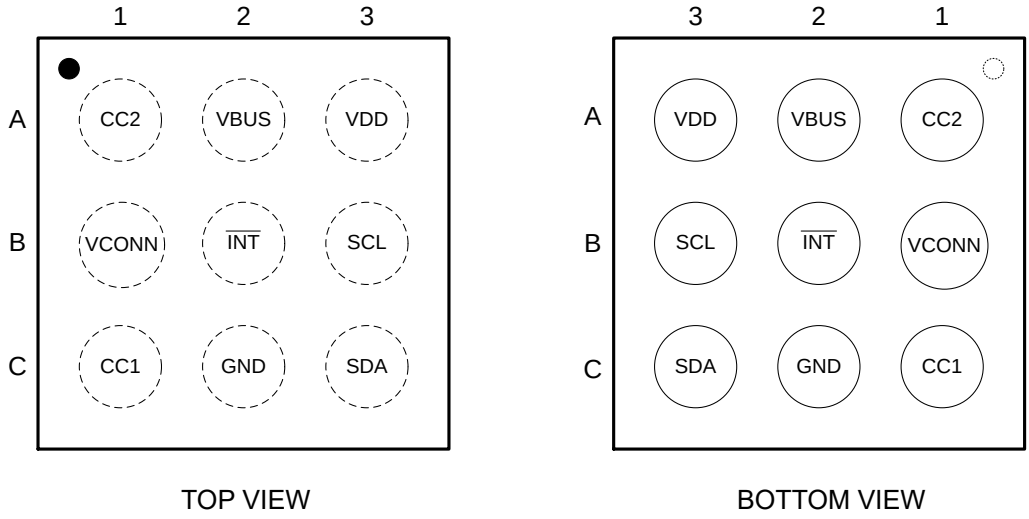


Figure 1. Pin Assignment

Pin Function

Pin No. WLCSP9	Pin Name	Description
A1	CC2	Type-C Connector Configuration Channel Pin2.
A2	VBUS	VBUS input pin for attach and detach detection.
A3	VDD	Positive Supply.
B1	VCONN	Regulated Power input For USB3.1 Full Featured Cables or Other Accessories.
B2	$\overline{INT}$	Interrupt Terminal to u-Processor Indicating Register Update. (Low Active Open-drain Output)
B3	SCL	I^2C communication clock signal.
C1	CC1	Type-C Connector Configuration Channel Pin1.
C2	GND	Ground (All ground must connected together in application).
C3	SDA	I^2C communication data signal.

Block Diagram

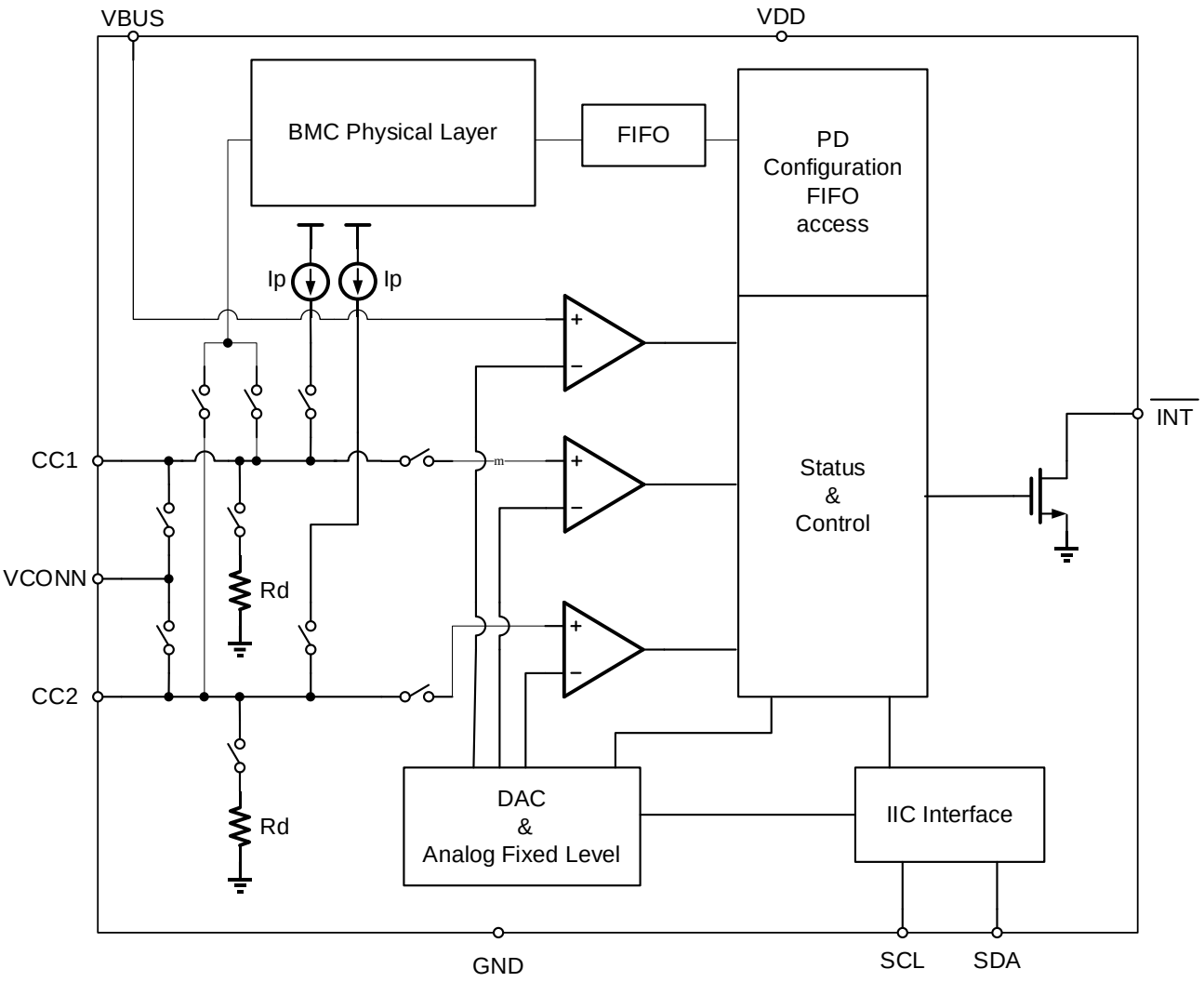


Figure2. Function Block

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min	Max	Unit
V_{DD} /V_{CONN}	VDD / VCONN Input Voltage	-0.3	6	V
V_{IO}	SCL / SDA / $\overline{INT}$ Input Voltage	-0.3	6	V
V_{CCX}	CC1 / CC2 Voltage	-0.3	28	V
V_{BUS}	VBUS to GND	-0.3	28	V
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
T_{LEAD}	Lead Temperature（Soldering，10sec）		+260	°C
P_D	Power Dissipation		1200	mW
θ_{JA}	Package Thermal Resistance (WLCSP9)		83.3	°C/W
ESD	HBM, JESD22-A114	±2000		V
	CDM, JESD22-A114	±1000		V
I_{LU}	Latch-up, JEDEC78	±200		mA

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation.
Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ET7303Adoes not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min	Max	Unit
V_{BUS}	VBUS to GND Supply Voltage	GND=0V	4.0	24	V
V_{DD}	VDD to GND Supply Voltage	GND=0V	3	5.5	V
V_{CONN}	VCONN to GND Supply Voltage	GND=0V	3.3	5.5	V
I_{VCONN}	VCONN Supply Current		200	600	mA
T_A	Operating Temperature, Free Air		-40	+85	°C

Electrical Characteristic

(T_A=-40 to +85°C,T_J=-40 to +150°C,V_{DD} = 3.3V,All typical values are at T_A=25°C unless otherwise specified.)

VBUS Related Parameters

Symbol		Parameter	Min	Typ	Max	Unit
V_{VBUS}		VBUS Detection Valid Voltage		4		V
V_{safe0V}		VBUS V_{safe0V}	-	--	0.8	V
$V_{measure}$	$V_{mearange}$	VBUS Measure Range(1)	5	--	20	V
	$V_{meastep}$	VBUS Measurement Resolution(1) (when VBUS Range 5 to10V)		0.5		V
		VBUS Measurement Resolution(1) (when VBUS Range 10 to 20V)		1		V

Note1: Guaranteed by characterization. Not production tested.

Type-C CC Switches

Symbol	Parameter	Min	Typ	Max	Unit
R_{SW_CCX}	RDSON for SWITCH1 and SWITCH2， VCONN to CC1 & CC2		0.8	1.5	Ω
I_{SW_CCX}	Over-Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range.(2)	450	600	750	mA
$t_{SoftStart\_3.3V}$	Time taken for the VCONN switch to turn on. V_{DD}=3.3V， V_{CONN}=3.3V	0.2	0.35	0.50	ms
$t_{SoftStart\_5V}$	Time taken for the VCONN switch to turn on. V_{DD}=3.3V， V_{CONN}=5V	0.3	0.45	0.60	ms
I_{TOL_CCX}	Tolerance of CC Current to VDD of 80uA, 180uA (1.5A) and 330 uA (3A)	-8		8	%
R_{DEVICE}	Device Pull-down Resistance (V_{DD}>3.0 V)	4.59	5.10	5.61	kΩ
V_{TH_DBL}	UFP Pull-Down Threshold Voltage in Dead Battery , Under I_{CC} = ICC_DFP80uA and ICC_DFP180uA	0.2		1.6	V
V_{TH_DBH}	UFP Pull-Down Threshold Voltage in Dead Battery, Under I_{CC} = ICC_DFP330uA	0.8		2.6	V

Note2： I_{SW_CCX} is progammable ,can be set to 200/300/400/500/600mA , and the default value is 600mA.

Current Consumption (V_{DD}=3.3V)

Symbol	Parameter	VDD Conditions	Min	Typ	Max	Unit
I_{UL}	Low-Power Mode	CC toggle at DRP mode when port is unconnected and waiting for connection	10	20	75	uA
I_{VCONN}	VCONN Power	VCONN5V supply on, VCONN5V Current when VCONN without supply to CC	6	15	30	uA
I_{SB}	Idle Mode Current	Cable attached (Full function on)		2.0		mA

Baseband PD

Symbol	Parameter	Min	Typ	Max	Unit
UI	Unit interval	3.03	3.35	3.7	us
Transmitter					
R_{Output}	TX Output Resistance	33	50	75	Ω
$p_{BitRate}$	Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate(3)			0.25	%
$t_{InterFrameGap}$	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble(3)	25			us
$t_{EndDriveBMC}$	Time to cease driving the line after the end of the last bit of the Frame(3)			23	us
$t_{HoldLowBMC}$	Time to Cease Driving the Line after the final High-to-Low Transition(3)	1			us
V_{swing}	Voltage Swing	1.05	1.12	1.2	V
$t_{StartDrive}$	Time before the start of the first bit of the preamble when the transmitter shall start driving the line(3)	-1		1	us
t_{RISE_TX}	Rise Time(3)	300			ns
t_{FALL_TX}	Fall Time(3)	300			ns
Receiver					
z_{BmcRx}	Receiver Input Impedance(3)	1			MΩ
$t_{TransWindow}$	Time Window for Detecting Non-Idle(3)	12		20	us

Note3: Guaranteed by characterization. Not production tested.

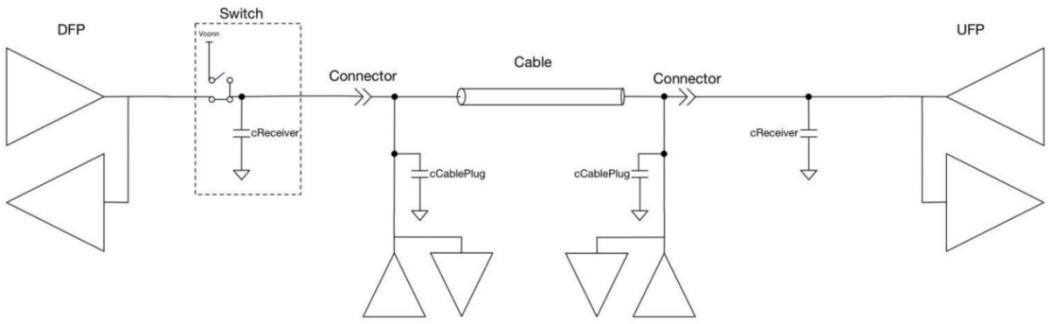


Figure 3. Transmitter Test Load

IO Specifications (V_{DD}=3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL_INTN}	INT_N Output Low Voltage (I_{OL}=4mA)			0.4	V
$I^2C\_V_{DD}$	I^2C Bus Supply Voltage	1.2		3.6	V
V_{ILI2C}	Low-Level Input Voltage			0.4	V
V_{IHI2C}	High-Level Input Voltage	0.9			V
I_{I2C}	SDA /SCL Pins Input Current (Input Voltage 0.1V_{DD} to 0.9V_{DD})	-10		10	uA
V_{OLSDA}	SDA Open-Drain Low-Level Output Voltage (I_{OL}=3mA)	0		0.4	V

I²C Specifications

Symbol	Parameter	Min	Max	Unit
f_{SCL}	I²C SCL Clock Frequency(4)	0	3400	kHz
$t_{HD;DAT}$	Data Hold Time(4)	30		ns
$t_{SU;DAT}$	Data Set-up Time(4)	70		ns
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter(4)		50	ns

Note4: Guaranteed by characterization. Not production tested.

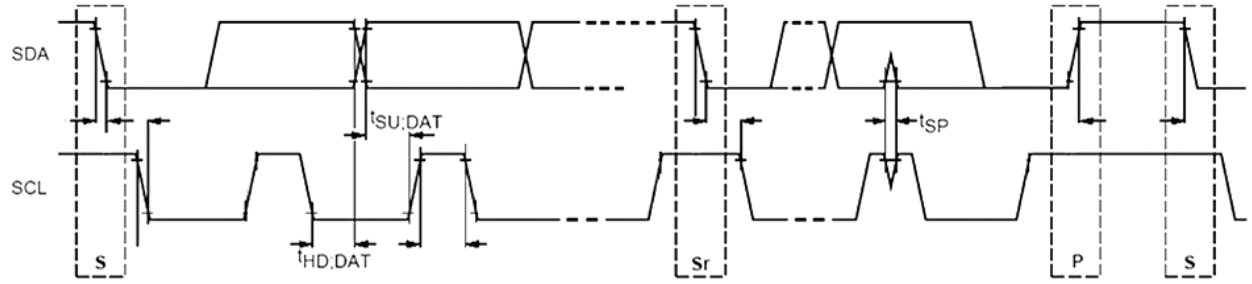


Figure 4. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Function Description

Configuration Channel Switch

The ET7303A integrates the control and detection functionality required to implement a USB Type-C host, device or dual-role port including: CC Pull-Down(RD),Pull-Up (Ip),VCONN Power Switch,USB BMC Power Delivery Physical Layer and CCx Threshold Comparators. Each CCx pin contains a flexible switch matrix that allows the host software to control what type of Type-C port is implemented. The switches are shown in Figure5.

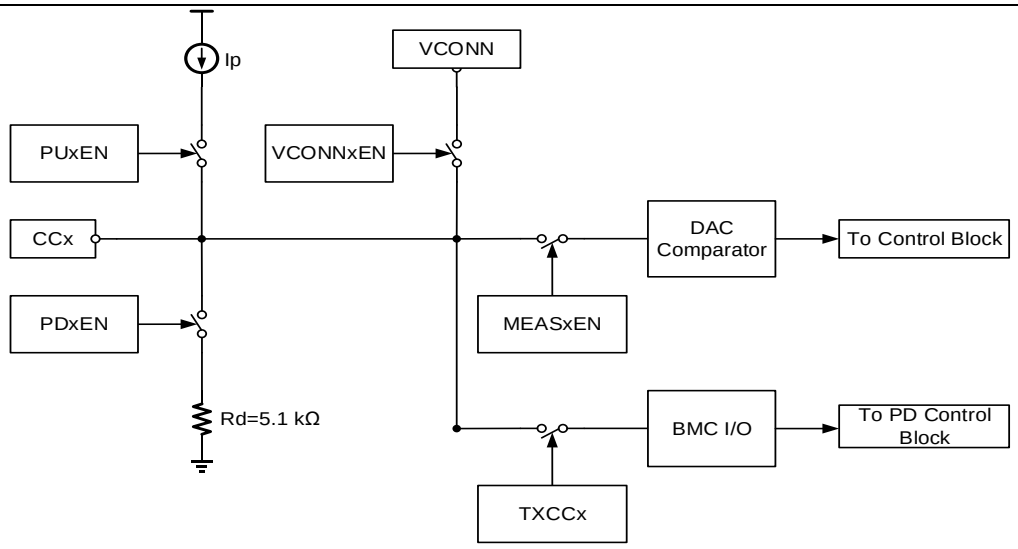


Figure 5. Configuration Channel Switch

Type-C Detection

The ET7303A implements multiple comparators that can be used by software to determine the state of the CC and VBUS pins. This status information provides the software all the information required to determine attach, detach and charging current capabilities based on the specific Type-C port to which the ET7303Ahas been configured.

The ET7303A has three fixed threshold comparators that match the USB Type-C specification for the three charging current levels that can be detected by a Type-C device. These comparators automatically cause a interrupt to occur when there is a change of state.
The ET7303A also has a fixed comparator that monitors if VBUS has reached a valid threshold or not. ET7303A can measure VBUS up to 20V which allows the software to confirm that changes to the VBUS line have occurred as expected based on various communication methods (Power Delivery (PD)) to change the charging level.

Detection through Autonomous Device DRP Toggle

The ET7303A has the capability to do autonomous DRP toggle. In autonomous toggle the ET7303A implements a fixed DRP toggle between presenting as a SRC and presenting as a SNK. Alternately, it can present as a SRC or SNK only and monitor CC1, CC2 and VBUS status.

Power Level Determination

The Type-C specification outlines the order of precedence for power level determination which covers power levels from basic USB2.0 levels to the highest levels of USB PD. The host software is expected to follow the USB Type-C specification for charging current priority based on feedback from the ET7303Adetection, and any USB Power Delivery communication.

Power Up, Initialization and Reset

When power is first applied through VDD, the ET7303A is reset and registers are initialized to the default values shown in the register map. ET7303A can be reset through software in the RESET register.
To properly configure the device in low power operation, place a 330pF cap on each CC pin and set the registers to default by programming the RESET register.

VBUS Monitoring

One of the features of USB PD is the ability to raise VBUS above the default vSafe5V level. The ability to monitor the VBUS voltage level is critical to determining when VBUS is at desired level as well as when VBUS is no longer present. The ET7303A implements measuring of VBUS and the results are stored in the VBUS Voltage register. The VBUS voltage measurement is enabled by setting the VBUS_MEASURE_EN bits in VBUS register.

VCONN

VCONN is required by active cables, e-mark, and VCONN powered accessories like Alternate Mode adapters. These types of devices or cables present Ra on one CC pin and Rd on the other CC pin. VCONN must be enabled when any of device or cable requiring VCONN is connected to a Type-C port and the ET7303A is operating as a DFP or DFP in DRP mode. Software can also enable the VCONN switch when the ET7303A is

a UFP during a VCONN_SWAP sequence. The ET7303A implements a VCONN switch which is controlled by software. The default state of this switch is open.

Once the VCONN switch is closed, the switch can be opened by any of the following conditions.

- Software clear in Power Control register.
- VCONN over current fault condition occurs resulting in ET7303A opening VCONN switch and setting the VCONN_OCP_FAULT_STATUS bit in Fault Status register.
- Hard Reset ordered set is received.
- Cable is removed (Rd no longer present) results in ET7303A opening VCONN switch and discharging VCONN to vSafe0V

The ET7303A discharges VCONN to vSafe0V by enabling Rd at designated CC pin anytime the VCONN switch transitions from closed to open state. Once at vSafe0V, the ET7303A disables the discharge circuit by removing Rd and then re-enable Rp (assuming it is still enabled in Role Control register).
Before closing the VCONN switch, the TCPM must make sure the voltage on VCONN pin is at a valid level. When opening the VCONN switch by clearing the ENABLE_VCONN bit, the TCPM software must make sure voltage on VCONN pin is at valid level until after VCONN switch is opened and then, if desired, can remove the voltage from the VCONN pin. Removing the voltage on VCONN pin before VCONN switch is opened will result in a false VCONN fault condition.

Interrupts

The ET7303A asserts the INT_N pin low anytime an unmasked event occurs. Upon assertion of the interrupt, the TCPM should read the Alert Registers to determine the reason for interrupt. Upon reading the Alert register, the TCPM should clear the interrupt by writing a 1’b1 to the appropriate field in the Alert register.
If the FAULT flag is set in the Alert register, the TCPM must first read the Fault Status register to determine reason for fault. Then clear the appropriate field in the Fault Status register by writing a 1’b1. Once all fields in Fault Status register are cleared, the TCPM can then clear the flag in the Alert Register by writing a 1’b1.
The ET7303A also has Vendor Defined Interrupt registers which is not part of the USB TCPC specification. These vendor defined interrupts are masked by default. Software can enable vendor interrupts by setting the appropriate bit in the Vendor Interrupts Mask Register and setting the VENDOR_IRQ_MASK field in the Alert Mask register.

BMC Power Delivery

The Type-C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol and is used for many different reasons with the Type-C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels
- Alternative Interfaces such as MHL, Display Port
- Vendor specific interfaces for use with custom docks or accessories
- Role swap for dual-role ports that want to switch who is the host or device
- Communication with USB3.1 full featured cables

  All Messages shall be composed of a Message Header and a variable length (including zero) data portion. A Message either originates in the Protocol Layer and is passed to the Physical Layer, or it is received by the Physical Layer and passed to the Protocol Layer. (Please see the Power Delivery Specification)

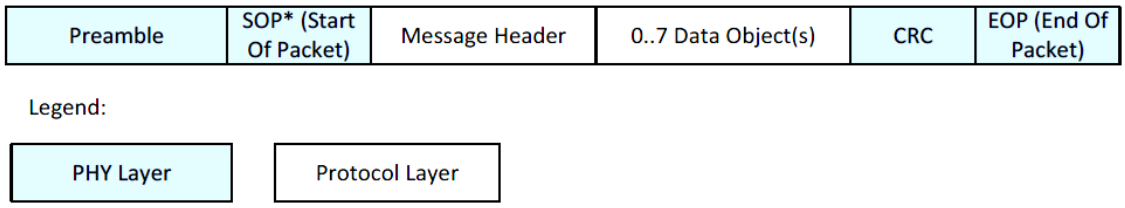


Figure 6. USB Power Delivery Packet Format including Message Payload

The ET7303A integrates a thin BMC PD client which includes the BMC physical layer and packet buffer which allows packets to be sent and received by the host software through I²C accesses. The ET7303A allows host software to implement all features of USB BMC PD through writes and reads of the buffer and control of the ET7303A physical interface, please refer to Figure7 and Figure8.

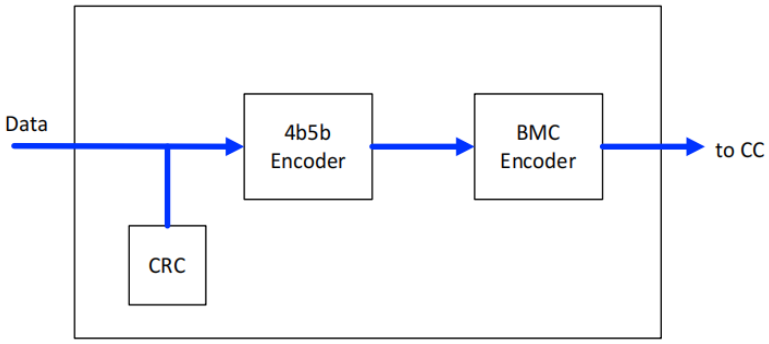


Figure 7. ET7303A BMC Transmitter Block Diagram

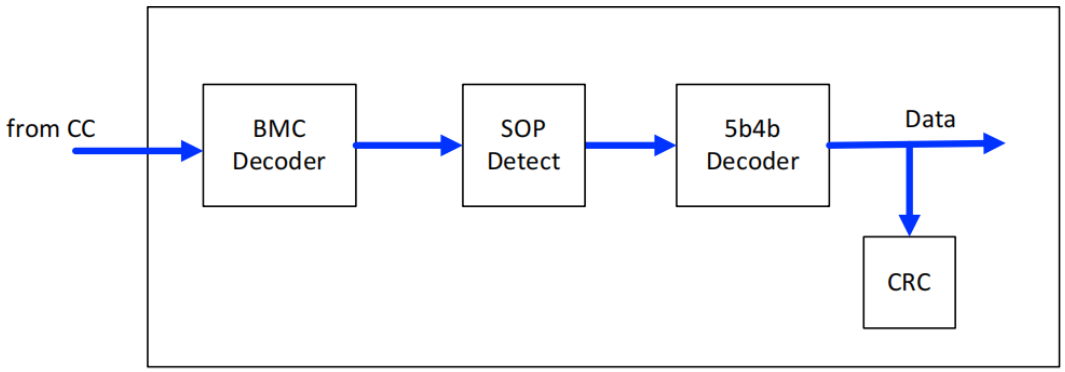


Figure 8. ET7303A BMC Receiver Block Diagram

Abbreviations :

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

Type-C Port Controller (TCPC) Interface

The Type-C Port Controller Interface (TCPCI) is the interface between a Type-C Port Manager and a Type-C Port Controller ,please refer to Figure9.

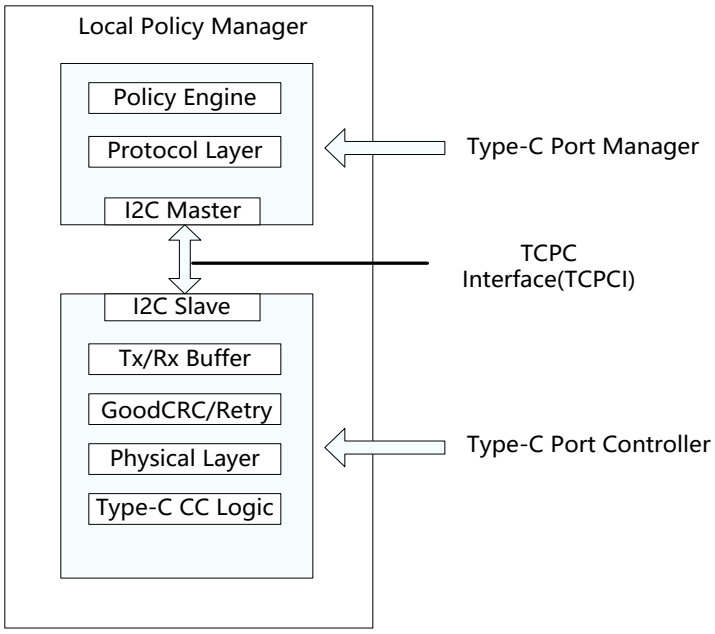


Figure 9. TCPC Interface

The Controller Interface uses the I²C Protocol:

The TCPM is the only master on this I²C bus.The TCPC is a slave device on this I²C bus.Each Type-C port has its own unique I²C slave address The TCPC shall have equal numbers of unique I²C slave addresses and supported Type-C ports The TCPC supports fast-mode bus speed. The TCPC has an open drain output, active low INT_N Pin. This pin is used to indicate change of state, where INT_N pin is asserted when any Alert Bits are set. The TCPCI supports an I/O nominal voltage range of 1.8V and 3.3V.The TCPC can auto-increment the I²C internal register address of the last byte transferred during a read independent of an ACK/NACK from the master.

I²C Interface

The ET7303A includes a full I²C slave controller. This block is designed for fast mode. Examples of an I²C write and read sequence are shown in Figure 10 and Figure 11 respectively.

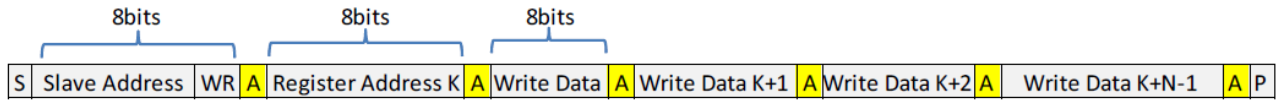


Figure 10. I²C Write Example

Note: Single Byte read is initiated by Master with P immediately following first data byte.

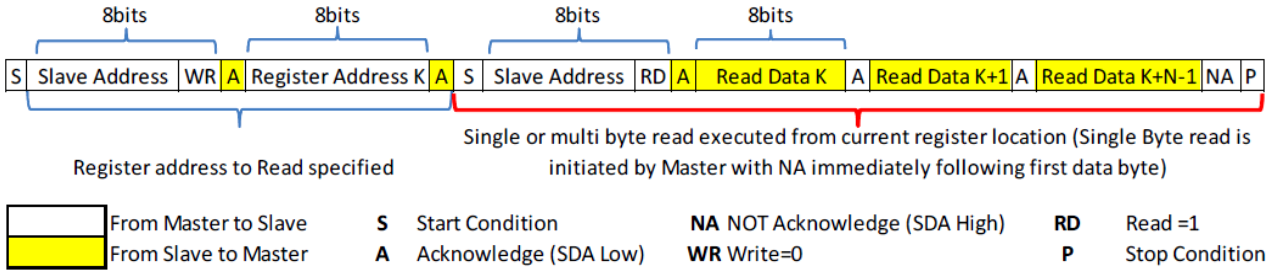


Figure 11. I²C Read Example

Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	1	0	0	1	1	1	0	R/W

Register Map :

Address	Register Name	Type	Reset Value
00h..01h	VENDOR_ID	R	CFh,6Dh
02h..03h	PRODUCT_ID	R	11h,17h
04h..05h	DEVICE_ID	R	71h,21h
06h..07h	USBTYPEC_REV	R	11h,00h
08h..09h	USBPD_REV_VER	R	11h,20h
0Ah..0Bh	PD_INTERFACE_REV	R	10h, 10h
0C..0Fh	Reserved		
10h..11h	ALERT	R/W	00h,00h
12h..13h	ALERT_MASK	R/W	FFh, 0Fh
14h	POWER_STATUS_MASK	R/W	FFh
15h	FAULT_STATUS_MASK	R/W	7Fh
16..17h	Reserved		
18h	CONFIG_STANDARD_OUTPUT	R/W	00h
19h	TCPC_CONTROL	R/W	00h
1Ah	ROLE_CONTROL	R/W	0Ah
1Bh	FAULT_CONTROL	R/W	00h
1Ch	POWER_CONTROL	R/W	00h
1Dh	CC_STATUS	R	00h
1Eh	POWER_ STATUS	R	08h

Register Map (Continued):

Address	Register Name	Type	Reset Value
1Fh	FAULT_STATUS	R/W	00h
20h..22h	Reserved	R	
23h	COMMAND	W	00h
24h..25h	DEVICE_CAPABILITIES_1	R	D8h, 02h
26h..27h	DEVICE_CAPABILITIES_2	R	35h,00h
28h	STANDARD_INPUT_CAPABILI TIES	R	00h
29h	STANDARD_OUTPUT_CAPABI LITIES	R	00h
2Ah..2Dh	Reserved	R	
2Eh	MESSAGE_HEADER_INFO	R/W	02h
2Fh	RECEIVE_DETECT	R/W	00h
30h	RECEIVE_BYTE_COUNT	R	00h
31h	RX_BUF_FRAME_TYPE	R	00h
32h	RX_BUF_HEADER_BYTE_0	R	00h
33h	RX_BUF_HEADER_BYTE_1	R	00h
34h	RX_BUF_OBJ1_BYTE_0	R	00h
35h	RX_BUF_OBJ1_BYTE_1	R	00h
36h	RX_BUF_OBJ1_BYTE_2	R	00h
37h	RX_BUF_OBJ1_BYTE_3	R	00h
38h	RX_BUF_OBJ2_BYTE_0	R	00h
…	RX_BUF_OBJn_BYTE_m	R	00h
4Fh	RX_BUF_OBJ7_BYTE_3	R	00h
50h	TRANSMIT	R/W	00h
51h	TRANSMIT_BYTE_COUNT	R/W	00h
52h	TX_BUF_HEADER_BYTE_0	R/W	00h
53h	TX_BUF_HEADER_BYTE_1	R/W	00h
54h	TX_BUF_OBJ1_BYTE_0	R/W	00h
…	TX_BUF_OBJn_BYTE_m	R/W	00h
6Fh	TX_BUF_OBJ7_BYTE_3	R/W	00h
90h	CONFIG1_LOWPWR	R/W	07h
93h	BMCIO_VCONNOCP	R/W	81h
97h	STATUS1	R	00h
98h	INT1	R/W	00h
99h	MASK1	R/W	00h
9Fh	WAKEUP	R/W	80h
A0h	RST	R/W	00h
A2h	TDRP	R/W	03h
A3h	TDRP_DUTY0	R/W	47h
A4h	TDRP_DUTY1	R/W	01h

Register detailed description, see below

Address = 0x00[reset =0xCF] --------Vendor ID Byte 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDOR_ID_BYTE_0	R	0xCF	Byte 0 of a 16-bit USB-IF defined ETEK vendor ID of 0x6DCF.

Address = 0x01 [reset = 0x6D] -------- Vendor ID Byte 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDOR_ID_BYTE_1	R	0x6D	Byte 1 of a 16-bit USB-IF defined ETEK vendor ID of 0x6DCF.

Address = 0x02 [reset = 0x11] -------- Product ID Byte 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODUCT_ID_BYTE_0	R	0x11	Byte 0 of ET7303A16-bit Product ID of 0x1711.

Address = 0x03 [reset = 0x17] -------- Product ID Byte 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODUCT_ID_BYTE_1	R	0x17	Byte 1 of ET7303A16-bit Product ID of 0x1711.

Address = 0x04 [reset = 0x71] -------- Device ID Byte 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Device_ID_BYTE_0	R	0x71	Byte 0 of a 16-bit Device ID.

Address = 0x05 [reset = 0x21] --------Device ID Byte 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Device_ID_BYTE_1	R	0x21	Byte 1 of a 16-bit Device ID.

Address = 0x06 [reset = 0x11] -------- USB Type-C Revision Byte 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USBTYPEC_REV_BYTE_0	R	0x11	Byte 0 of a 16-bit USB Type-C Revision. Revision 1.1. The ET7303A also supports USB Type-C™ Revision 1.2.

Address = 0x07 [reset = 0x00] -------- USB Type-C Revision Byte 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USBTYPEC_REV_BYTE_1	R	0x00	Byte 1 of a 16-bit USB Type-C Revision.

Address = 0x08 [reset = 0x11] -------- USB PD Revision Version Byte 0 Description

Bit	Field	Type	Reset	Description
7:0	USBPD_REV_VER_BYTE_0	R	0x11	Byte 0 of a 16-bit USB PD version. Version 1.1.

Address = 0x09 [reset = 0x00] -------- USB PD Revision Version Byte 1 Descriptions

Bit	Field	Type	Reset	Description
7:0	USBPD_REV_VER_BYTE_1	R	0x20	Byte 1 of a 16-bit USB PD Revision. Revision 2.0.

Address = 0x0A [reset = 0x10] -------- PD Interface Revision Byte 0 Descriptions

Bit	Field	Type	Reset	Description
7:0	PD_INTERFACE_REV_BYTE_0	R	0x10	Byte 0 of a 16-bit PD Interface (TCPC) Version. Version 1.0

Address = 0x0B [reset = 0x10] -------- PD Interface Revision Byte 1 Descriptions

Bit	Field	Type	Reset	Description
7:0	PD_INTERFACE_REV_BYTE_1	R	0x10	Byte 1 of a 16-bit PD Interface (TCPC) Revision. Revision 1.0

Address = 0x10 [reset = 0x00] -------- Alert Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_ALARM_HI	RC	0	VBUS Voltage Alarm Hi. 0b: Cleared 1b: A high-voltage alarm has occurred
6	TX_SOP_SUCCESS	RC	0	Transmit SOP* Message Successful 0b: Cleared 1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
5	TX_SOP_DISCARD	RC	0	Transmit SOP* Message Discarded 0b: Cleared 1b: Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers are empty.
4	TX_SOP_FAIL	RC	0	Transmit SOP* Message Failed 0b: Cleared 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
3	RX_HARD_RESET	RC	0	Received Hard Reset. 0b: Cleared. 1b: Received Hard Reset message
2	RX_SOP_STATUS	RC	0	Receive SOP* Message Status. Note RECEIVE_BYTE_COUNT being zero does not set this bit. 0b: Cleared. 1b: Receive buffer register changed.
1	PWR_STATUS	RC	0	Power Status 0b: Cleared. 1b: Power Status Changed
0	CC_STATUS	RC	0	CC Status. 0b:Cleare 1b: CC status changed

Address = 0x11 [reset = 0x00] -------- Alert Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0x0	Reserved
3	VBUS_SINK_DIS	RC	0	Not support
2	RRX_BUF_OVR	RC	0	Rx Buffer Overflow 0b: ET7303A Rx buffer is functioning properly 1b: ET7303A Rx buffer has overflowed
1	FAULT	RC	0	Fault 0b: No Fault 1b: A Fault has occurred. Read FAULT_STATUS register
0	VBUS_ALARM_LO	RC	0	Not support

Address = 0x12 [reset = 0xFF] --------Alert Mask Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_ALARM_HI_MASK	RW	1	Not support
6	TX_SOP_SUCCESS_MASK	RW	1	Transmit SOP* Message successful Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	TX_SOP_DISCARD_MASK	RW	1	Transmit SOP* Message discarded Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	TX_SOP_FAIL_MASK	RW	1	Transmit SOP* Message failed Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
3	RX_HARD_RESET_MASK	RW	1	Received Hard Reset Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	RX_SOP_STATUS_MASK	RW	1	Receive SOP* Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	PWR_STATUS_MASK	RW	1	Power Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	CC_STATUS_MASK	RW	1	CC Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked

Address = 0x13 [reset = 0x0F] --------Alert Mask Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0x0	Reserved
3	VBUS_SINK_DIS_MASK	RW	1	Not support
2	RX_BUF_OVR_MASK	RW	1	Rx Buffer Overflow Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	FAULT_MASK	RW	1	Fault Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	VBUS_ALARM_LO_MASK	RW	1	Not support

Address = 0x14 [reset = 0x7F] --------Power Status Mask Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Not support
6	TCPC_INIT_STATUS_MASK	RW	1	TCPC Initialization Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	SRC_HIGH_VBUS_STATUS_MAS K	RW	1	Not support
4	SRC_VBUS_STATUS_MASK	RW	1	Not support
3	VBUS_PRES_DET_STATUS_MAS K	RW	1	VBUS Present Detection Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	VBUS_PRES_INT_MASK	RW	1	VBUS Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	VCONN_PRES_INT_MASK	RW	1	VCONN Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	SINK_VBUS_STATUS_INT_MASK	RW	1	Not support

Address = 0x15 [reset = 0x7F] --------FAULT Status Mask Register Descriptions

Bit	Field	Type	Reset	Description
7	VCON_OV_MASK	RW	0	VCON_OV Status Mask 0b : Interrupt masked 1b : Interrupt unmasked
6	FORCE_VBUS_MASK	RW	1	Force Off VBUS Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	AUTO_DISC_FAIL_MASK	RW	1	Auto Discharge Failed Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	FORCE_DISC_FAIL_MASK	RW	1	Force Discharge Failed Mask 0b: Interrupt masked 1b: Interrupt unmasked
3	VBUS_OCP_FAIL_STATUS_ MASK	RW	1	Internal or External OCP ,VBUS Over Current Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked For ET7303A this field has no meaning.
2	VBUS_OVP_FAIL_STATUS_ MASK	RW	1	Internal or External OVP ,VBUS Over Voltage Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked For ET7303A this field has no meaning.
1	VCONN_OCP_FAULT_STATUS _MASK	RW	1	V(VCONN) Over Current Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	I2C_INT_ERR_STATUS_MASK	RW	1	I^2C Interface Error Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked

Address = 0x18[reset = 0x00] -------- Config Standard Output Descriptions

Bit	Field	Type	Reset	Description
7	HIGH_Z_OUTPUTS	R/W	0	Not support
6	DEBUG_ACC_CONNECTED#	R/W	0	Not support
5	AUDIO_ACC_CONNECTED#	R/W	0	Not support
4	ACTIVE_CABLE_CONNECTED	R/W	0	Not support
3:2	MUX_CTRL	R/W	0	Not support
1	CONNECTION_PRES	R/W	0	Not support
0	CONN_ORIENT	R/W	0	Not support

Address = 0x19 [reset = 0x00] --------TCPC Control Register Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	000	Reserved
3:2	I^2C_CLOCK_STRETCHING_CTL	R	00	Not support
1	BIST_TEST_MODE	RW	0	Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the ET7303A. The TCPM should clear this bit when a detach is detected. 0b: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1b: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
0	PLUG_ORIENTATION	RW	0	0b: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.

Address = 0x1A [reset = 0x0A] --------ROLE Control Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved.
6	DRP	RW	0	0b: No DRP, Bits B3..0 determine Rp/Rd/Ra or open settings 1b: DRP
5:4	RP_VALUE	RW	00	00b: Rp default current 01b: Rp 1.5A 10b: Rp 3A 11b: Reserved
3:2	CC2	RW	2’b10	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don’t care)
1:0	CC1	RW	2’b10	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don’t care)

Address = 0x1B [reset = 0x00] --------FAULT Control Register Descriptions

Bit	Field	Type	Reset	Description
7	DIS_VCON_OV	RW	0	0b : Fault detection circuit enabled 1b : Fault detection circuit disabled
6:5	Reserved	R	0	Reserved
4	FORCE_OFF_VBUS	RW	0	Not support
3	VBUS_DIS_FAULT_DETECT_TIME R	RW	0	Not support
2	VBUS_OCP_FAULT	RW	0	Not support
1	VBUS_OVP_FAULT	RW	0	Not support
0	VCONN_OC_FAULT	RW	0	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled

Address = 0x1C [reset = 0x00] --------Power Control Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6	VBUS_VOLTAGE_MONITOR	RW	0	Not support
5	DISABLE_VOLTAGE_ALARMS	RW	0	Not support
4	AUTO_DISCHARGE_DISCONNECT	RW	0	Not support
3	EN_BLEED_DISCHARGE	RW	0	Not support
2	FORCE_DISCHARGE	RW	0	Not support
1	VCONN_PWR_SUPPORTED	RW	0	0b: ET7303A delivers at least 1W on VCONN 1b: ET7303A delivers at least the power indicated in DEVICE_CAPABILITIES.VCONNPOWER Supported

0	ENABLE_VCONN	RW	0	0b: Disable VCONN Source 1b: Enable VCONN Source to CC indicated by PLUG_ORIENTATION in TCPC Control register.

Address = 0x1D [reset = 0x00] --------CC Status Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	0	Reserved
5	LOOKING4CONNECTION	R	0	0b: ET7303A is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found. 1b: ET7303A is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)
4	CONNECT_RESULT	R	0	0b: the ET7303A is presenting Rp 1b: the ET7303A is presenting Rd

3:2	CC2_STATE	R	00	If (ROLE_CONTROL.CC2=Rp) or (CONNECT_RESULT=0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				If (ROLE_CONTROL.CC2=Rd) or (CONNECT_RESULT=1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
				If ROLE_CONTROL.CC2=Ra, this field is set to 00b
				If ROLE_CONTROL.CC2=Open, this field is set to 00b
				This field always returns 00b if (Looking4Connection=1) or (POWER_CONTROL.ENABLE_VCONN=1 and TCPC_CONTROL.PLUG_ORIENTATION =0).
				Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

1:0	CC1_STATE	R	00	If (ROLE_CONTROL.CC1 = Rp) or (CONNECT_RESULT=0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				If (ROLE_CONTROL.CC1 = Rd) or (CONNECT_RESULT=1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp- 1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp- 3.0A
				If ROLE_CONTROL.CC1=Ra, this field is set to 00b
				If ROLE_CONTROL.CC1=Open, this field is set to 00b
				This field always returns 00b if (Looking4Connection=1) or (POWER_CONTROL.ENABLE_VCONN=1 and TCPC_CONTROL.PLUG_ORIENTATION =1).
				Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

Address = 0x1E [reset = 0x08] --------Power Status Register Descriptions

Bit	Field	Type	Reset	Description
7	DEBUG_ACC_CONNECTED	R	0	Not support
6	TCPC_INIT_STATUS	R	0	0b: The ET7303Ahas completed initialization and all registers are valid. 1b: The ET7303Ais still performing internal initialization and the only registers that are guaranteed to return the correct values are00h..0Fh. The ET7303A will never set this flag so software needs to be aware at power-up one reason for INT_N assertion is ET7303A has completed its initialization.
5	SOURCING_HIGH_VOLTAGE	R	0	Not support
4	SOURCING_VBUS	R	0	Not support
3	VBUS_PRES_DETECT_ENABLED	R	1	0b: VBUS Present Detection Disabled 1b: VBUS Present Detection Enabled (Default) Indicates if the ET7303A is monitoring for VBUS Present or if the circuit has been powered off
2	VBUS_PRESENT	R	0	0b: VBUS Disconnected 1b: VBUS Connected
1	VCONN_PRESENT	R	0	0b: VCONN is not present

				1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4 V
0	SINKING_VBUS	R	0	Not support

Address = 0x1F [reset = 0x00] --------Fault Status Register Descriptions

Bit	Field	Type	Reset	Description
7	VCON_OV	RC	0	0b : Not in an over-voltage protection state 1b : Over-voltage fault latched.
6	FORCEOFF_VBUS_STATUS	RC	0	Not support
5	AUTO_DIS_FAIL_STATUS	RC	0	Not support
4	FORCE_DIS_FAIL_STATUS	RC	0	Not support
3	VBUS_OCP_FAULT_STATUS	RC	0	Not support
2	VBUS_OVP_FAULT_STATUS	RC	0	Not support
1	VCONN_OCP_FAULT_STATUS	RC	0	The ET7303A will set this flag if a VCONN over current fault is detected. This flag will also get set if voltage on VCONN pin drops between VCONN present threshold, while the VCONN switch is still closed. 0b: No Fault detected 1b: Over current VCONN fault latched
0	I^2C_INT_ERROR_STATUS	RC	0	0b: No Error 1b: I^2C error has occurred. A TRANSMIT has been sent with an empty TRANSMIT_BUFFER.

Address = 0x23 [reset = 0x00] --------Command Register Descriptions

Bit	Field	Type	Reset	Description
7:0	COMMAND	RC	0	22h: disable VBUS_detect ; 33h: Enable VBUS_detect ; 88h: assert FAULTStatus. I^2C error; 99h: Enable_look4connection(DRP-toggling) when ROLE_CONTROL.DRP =1;

Address = 0x24 [reset = 0xD8] --------Device Capabilities 1 Byte 0 Descriptions

Bit	Field	Type	Reset	Description
7:5	ROLES_SUPPORTED	R	110	Roles Supported. 000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only. 010b: Sink only 011b: Sink with accessory support 100b: DRP only (Default for ET7303A) 101b: Adapter or Cable(Ra) only

				110b: Source, Sink, DRP, Adapter/Cable all supported (default) 111b: Not valid
4	SOP_DBG_SUPPORT	R	1	SOP’_DBG/SOP”_DBG Support 0b: All SOP* except SOP’_DBG/SOP”_DBG 1b: All SOP* messages are supported Configured in RECEIVE_DETECT and TRANSMIT
3	SRC_VCONN_SUPPORT	R	1	Source VCONN. 0b: ET7303A is not capable of switching VCONN 1b: ET7303A is capable of switching VCONN
2	SNK_VBUS_SUPPORT	R	0	Sink VBUS. 0b: ET7303A is not capable controlling the sink path to the system load 1b: ET7303A is capable of controlling the sink path to the system load
1	SRC_VBUS_HIGH_ SUPPORT	R	0	Source High Voltage VBUS. 0b: ET7303A is not capable of controlling the source high voltage path to VBUS 1b: ET7303A is capable of controlling the source high voltage path to VBUS
0	SRC_VBUS_SUPPORT	R	0	Source VBUS. 0b: ET7303A is not capable of controlling the source path to VBUS 1b: ET7303A is capable of controlling the source path to VBUS

Address = 0x25[reset = 0x02] -------Device Capabilities 1 Byte 1 Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6	VBUS_OCP_SUPPORT	R	0	VBUS OCP Reporting 0b: VBUS OCP is not reported by the ET7303A 1b: VBUS OCP is reported by the ET7303A
5	VBUS_OVP_SUPPORT	R	0	VBUS OVP Reporting 0b: VBUS OVP is not reported by the ET7303A 1b: VBUS OVP is reported by the ET7303A
4	BLEED_DISCHARGE_ SUPPORT	R	0	Bleed Discharge 0b: No Bleed Discharge implemented in ET7303A 1b: Bleed Discharge is implemented in the ET7303A
3	FORCE_DISCHARGE_ SUPPORT	R	0	Force Discharge. 0b: No Force Discharge implemented in ET7303A

				1b: Force Discharge is implemented in the ET7303A
2	VBUS_MEASURE_ALARM_ SUPPORT	R	0	VBUS Measurement and Alarm Capable 0b: No VBUS voltage measurement nor VBUS Alarms 1b: VBUS voltage measurement and VBUS Alarms
1:0	SRC_RP_SUPPORT	R	10b	Source Resistor Supported 00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3A, 1.5A, and default 11b: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register

Address = 0x26 [reset = 0x35] -------Device Capabilities 2 Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	SINK_DISCONNECT_DETECT_ SUPPORT	R	0	Sink Disconnect Detection 0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented
6	STOP_DISCHARGE_ THRESHOLD_SUPPORT	R	0	Stop Discharge Threshold 0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented
5:4	VBUS_VOLTAGE_ALARM_LSB	R	11	VBUS Voltage Alarm LSB. 00b: ET7303A has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01b: ET7303A has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by ET7303A. 10b: ET7303A has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by ET7303A. 11b: Not support this function.
3:1	VCONN_PWR_SUPPORT	R	010	VCONN Power Supported 000b: 1 W 001b: 1.5 W

				010b: 2 W 011b: 3 W 100b: 4 W 101b: 5 W 110b: 6 W 111b: External
0	VCONN_OC_FAULT_SUPPORT	R	1	VCONN OverCurrent Fault Capable. 0b: ET7303A is not capable of detecting a VCONN fault 1b: ET7303A is capable of detecting a VCONN fault

Address = 0x27 [reset = 0x00] -------Device Capabilities 2 Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	0x00	Reserved

Address = 0x28 [reset = 0x00] -------Standard Input Capabilities Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0	Reserved
2	EXT_VBUS_OVF_SUPPORT	R	0	VBUS External Over Voltage Fault 0b: Not present in ET7303A 1b: Present in ET7303A This field has no meaning for ET7303A
1	EXT_VBUS_OCF_SUPPORT	R	0	VBUS External Over Current Fault 0b: Not present in ET7303A 1b: Present in ET7303A This field has no meaning for ET7303A
0	EXT_FORCE_OFF_VBUS_SUPPO RT	R	0	Force Off VBUS (Source or Sink) 0b: Not present in ET7303A 1b: Present in ET7303A This field has no meaning for ET7303A

Address = 0x29 [reset = 0x00] -------Standard Output Capabilities Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6	DEBUG_ACCESSORY_OUT	R	0	Debug Accessory Indicator 0b: Not present in ET7303A 1b: Present in ET7303A
5	VBUS_PRESENT_OUT	R	0	VBUS Present Monitor 0b: Not present in ET7303A 1b: Present in ET7303A
4	AUDIO_ACCESSORY_OUT	R	0	Audio Adapter Accessory Indicator 0b: Not present in ET7303A 1b: Present in ET7303A

3	ACTIVE_CABLE_OUT	R	0	Active Cable Indicator 0b: Not present in ET7303A 1b: Present in ET7303A
2	MUX_OUT	R	0	MUX Configuration Control 0b: Not present in ET7303A 1b: Present in ET7303A
1	CONNECTION_OUT	R	0	Connection Present 0b: Not present in ET7303A 1b: Present in ET7303A
0	CONNECTOR_ORIENT_OUT	R	0	Connector Orientation 0b: Not present in ET7303A 1b: Present in ET7303A

Address = 0x2E [reset = 0x02] -------Message Header Info Register Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	RW	000	Shall be set to zero by sender and ignored by receiver
4	CABLE_PLUG	RW	0	0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
3	DATA_ROLE	RW	0	0b: UFP 1b: DFP
2:1	USBPD_SPECREV	RW	01	00b: Revision 1.0 01b: Revision 2.0 10b: Revision 3.0 11b: Reserved
0	POWER_ROLE	RW	0	0b: Sink 1b: Source

Address = 0x2F [reset = 0x00] -------Receiver Detect Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Shall be set to zero by sender and ignored by receiver
6	EN_CABLE_RESET	RW	0	0b: ET7303A does not detect Cable Reset signaling 1b: ET7303A detects Cable Reset signaling
5	EN_HARD_RESET	RW	0	0b: ET7303A does not detect Hard Reset signaling 1b: ET7303A detects Hard Reset signaling
4	EN_SOP_DBGPP	RW	0	0b: ET7303A does not detect SOP_DBG'' message 1b: ET7303A detects SOP_DBG'' message
3	EN_SOP_DBGP	RW	0	0b: ET7303A does not detect SOP_DBG' message 1b: ET7303A detects SOP_DBG' message
2	EN_SOPPP_MESSAGE	RW	0	0b: ET7303A does not detect SOP'' message 1b: ET7303A detects SOP'' message

1	EN_SOPP_MESSAGE	RW	0	0b: ET7303A does not detect SOP' message 1b: ET7303A detects SOP' message
0	EN_SOP_MESSAGE	RW	0	0b: ET7303A does not detect SOP message 1b: ET7303A detects SOP message

Address = 0x30 [reset = 0x00] -------Receive Byte Count Register Descriptions

Bit	Field	Type	Reset	Description
7:0	RECEIVE_BYTE_COUNT	R	0x00	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register. This is the number of bytes in the RX_BUFFER_DATA_OBJECTS plus three (for the RX_BUF_FRAME_TYPE and RX_BUF_HEADER).

Address = 0x31 [reset = 0x00] -------Receive Buffer Frame Type Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	00000	Shall be set to zero by sender and ignored by receiver
2:0	RX_SOP_MESSAGE	R	000	000b: Received SOP 001b: Received SOP' 010b: Received SOP' ' 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved.

Address = 0x32 [reset = 0x00] -------Receive Buffer Header Byte 0 Descriptions

Bit	Field	Type	Reset	Description
7:0	RX_BUF_HDR_BYTE_0	R	0x00	Byte 0 (bits 7:0) of USB PD message header.

Address = 0x33 [reset = 0x00] -------Receive Buffer Header Byte 1 Descriptions

Bit	Field	Type	Reset	Description
7:0	RX_BUF_HDR_BYTE_1	R	0x00	Byte 1 (bits 15:8) of USB PD message header.

Address = 0x34~4F [reset = 0x00] -------Receive Buffer Data Object 1 Through 7 Descriptions

Bit	Field	Type	Reset	Description
7	RX_BUFF_OBJy_BYTE_x	R	0x00	RX Byte x.

Address = 0x50 [reset = 0x00] -------Transmit Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	RW	00	Shall be set to zero by sender and ignored by receiver
5:4	RETRY_COUNTER	RW	00	00b: No message retry is required 01b: Automatically retry message transmission once

				10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
3	Reserved	RW	0	
2:0	TX_SOP_MESSAGE	RW	000	000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP" 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2

Address = 0x51 [reset = 0x00] -------Transmit Byte Count Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BYTE_COUNT	RWU	0x00	The number of bytes the TCPM will write. This is the number of bytes in the TX_BUFFER_DATA_OBJECTS plus two (for the TX_BUF_HEADER)

Address = 0x52 [reset = 0x00] -------Transmit Buffer Header Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BUF_HDR_BYTE_0	RW	0x00	Byte 0 (bits 7:0) of USB PD message header.

Address = 0x53 [reset = 0x00] -------Transmit Buffer Header Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BUF_HDR_BYTE_1	RW	0x00	Byte 1 (bits 15:8) of USB PD message header.

Address = 0x54~6F [reset = 0x00] -------Transmit Buffer Data Object 1 Through 7 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BUFF_OBJx_BYTE_x	R	0	TX Byte Data object 1 through 7.

Address = 0x90 [reset = 0x07] -------CONFIG_LOWPWR Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	00	Reserved
5	VCONN DISCHARGE_EN	RW	0	VCONN OVP occurs and discharge path turn-on 0b : No discharge (default) 1b : Discharge
4	BMCIO_LPRPRD	RW	0	Set role in Low power mode: 0b : Low power mode RD (default) 1b : Low power mode RP
3	BMCIO_LPEN	RW	0	Low power mode enable

				0b : Standby mode (default) 1b : Low power
2	BMCIO_BG_EN	RW	1	BMCIO BandGap enable 0b : BandGap off ， CC pin function disable 1b : BandGap on (default)，CC pin function enable
1	VBUS_DETEN	RW	1	VBUS detection enable 0b : Measure off; 1b : Operation (default)
0	BMCIO_OSC_EN	RW	1	24M oscillator for BMC communication 0b : Disable 24M oscillator 1b : Enable 24M oscillator (default) Tips: 24M oscillator will be enabled automatically when INT occur.

Address = 0x93 [reset = 0x81] ------ BMCIO_VCONNOCP Register Descriptions

Bit	Field	Type	Reset	Description
7:5	BMCIO_VCONNOCP[2:0]	RW	100	VCONN over-current control selection 000b : Current level = 200mA 001b : Current level = 300mA 010b : Current level = 400mA 011b : Current level = 500mA 100b : Current level = 600mA(default) 101 to 111b : Reserved If VCONN OCP trigger, the switch turn off timing under 60us.
4:1	Reserved	R	0000	Reserved
0	Reserved	RW	1	Reserved

Address = 0x97 [reset = 0x00] -------STATUS1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	00000	Reserved
1	VBUS_safe0v	R	0	0b : VBUS over 0.5v(default) 1b : VBUS under 0.5v
0	Reserved	R	0	Reserved

Address = 0x98 [reset = 0x00] -------INT1 Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	00	Reserved
5	INT_RA_DETACH	RW	0	0b : Cleared (default) 1b : Ra detach
4:2	Reserved	RW	000	Reserved
1	INT_VBUS_safe0v	RW	0	0b :VBUS without under 0.5V(default);

				1b :VBUS under 0.5V
0	INT_WAKEUP	RW	0	0b : Cleared (default) ; 1b :LowPower mode exited

Address = 0x99 [reset = 0x00] -------MASK1 Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	00	Reserved
5	M_RA_DETACH	RW	0	0b : Interrupt masked (default) 1b : Interrupt unmasked
4:2	Reserved	R	000	Reserved
1	M_VBUS_safe0v	RW	0	0b : Interrupt masked (default) 1b : Interrupt unmasked
0	M_WAKEUP	RW	0	0b : Interrupt masked (default) 1b : Interrupt unmasked

Address = 0x9F [reset = 0x80] -------Wakeup Register Descriptions

Bit	Field	Type	Reset	Description
7	WAKEUP_SEL	RW	1	0b : Wakeup function disable 1b : Wakeup function enable (default)
6:4	Reserved	R	000	Reserved
3:0	Reserved	R	0000	Reserved

Address = 0xA0 [reset = 0x00] -------RST Register Descriptions

Bit	Field	Type	Reset	Description
7:1	Reserved	R	0	Reserved
0	SOFT_RST	RW	0	0b: do nothing; 1b: software reset.

Address = 0xA2 [reset = 0x03] -------T_{DRP} Register Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0000	Reserved
3:0	T_{DRP}	RW	0011	The period of DRP toggle consists with Source and Sink. Period = 51.2 + TDRP * 6.4 (ms) 0000 : 51.2ms ; 0001 : 57.6ms 0010 : 64ms ; 0011 : 70.4ms (default) … 1111 : 147.2ms

Address = 0xA3 [reset = 0x47] -------T_{DRP}_duty0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	D_SRC[7:0]	RW	47h	The percent of time that a DRP will, advertise Source during tDRP. Setting with 0xA4[1:0] , DUTY = (D_SRC[9:0] + 1) /1024 00'0000'0000 : 1/1024; 00'0000'0001 : 2/1024 … 01'0100'0110 : 327/1024; 01'0100'0111 : 328/1024 (default) … 11'1111'1110 : 1023/1024; 11'1111'1111 : 1024/1024;

Address = 0xA4 [reset = 0x01] -------T_{DRP}_duty1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	000000	Reserved
1:0	D_SRC[9:8]	RW	01	See 0xA3[7:0]

Typical Application

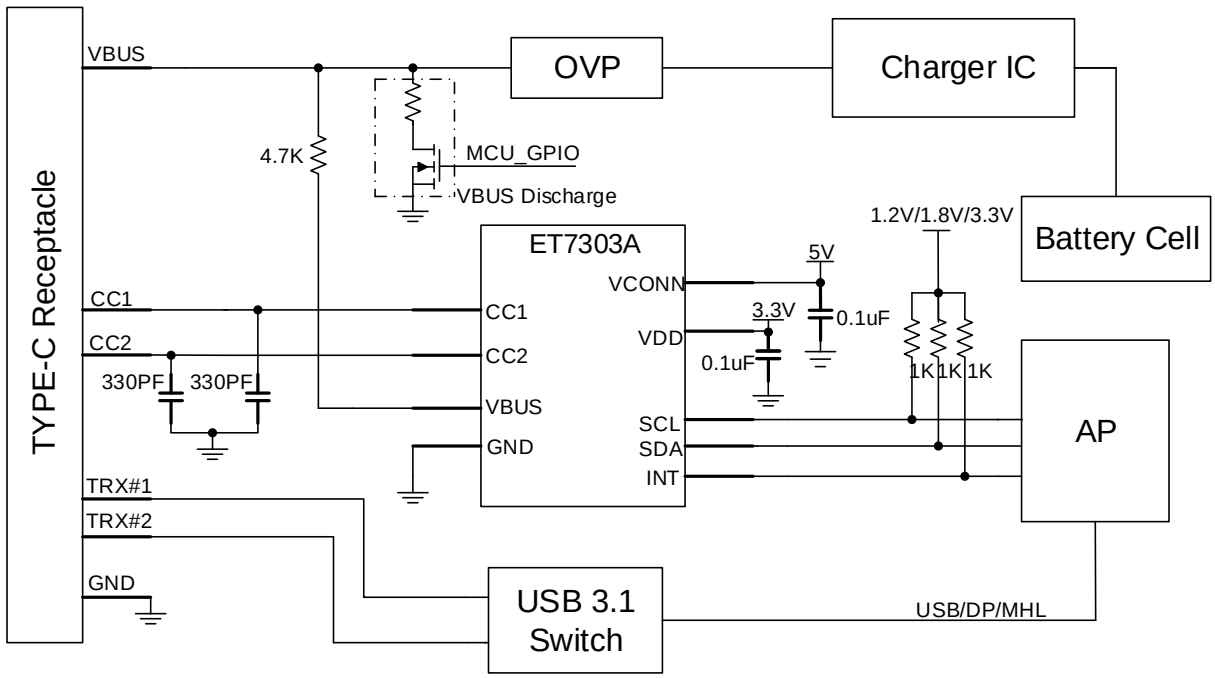


Figure 12. Typical Applications(*)

Notes* :

1. A pullup_resistor(value =1kohm) should be set on SCL/SDA/INT Port.

2. CC1/CC2 capacitance(C1/C2=330pF) is required.

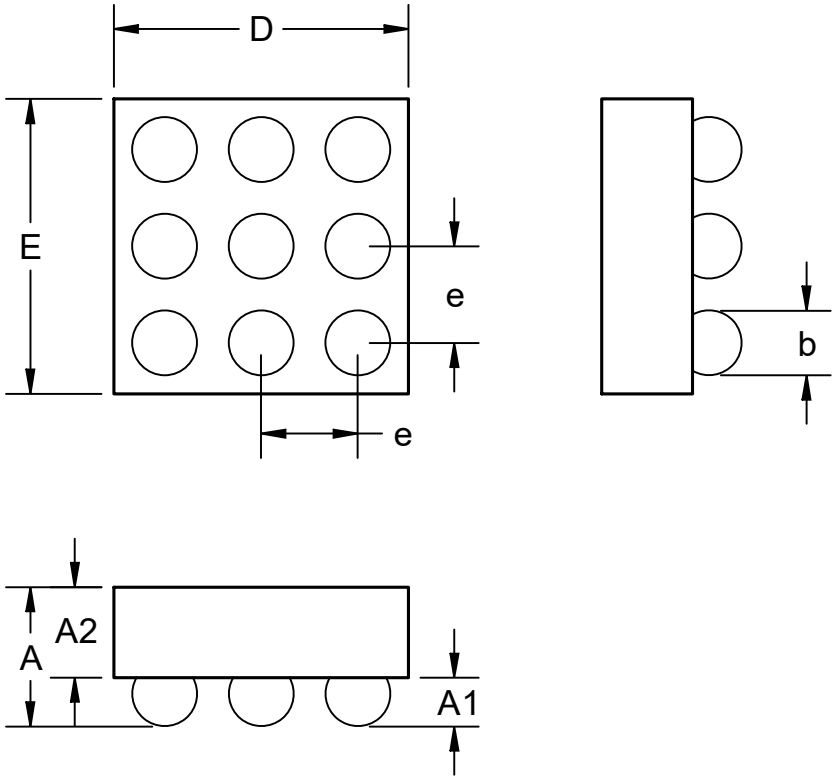
3. VBUS should be series in a 4.7kohm resistor, better for surge.

4. It is suggested to add a discharge-curcuit for VBUS.

5. If VCONN is not used, connect to GND via 1Kohm resistor.

Package Dimension

WLCSP9 Package

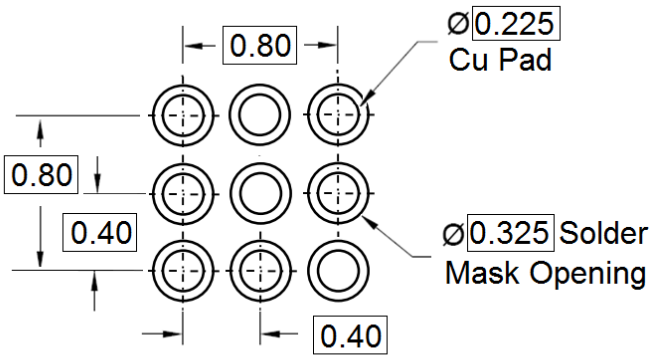


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

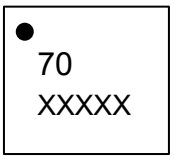
SYMBOL	MIN	NOM	MAX
A	0.502	0.550	0.598
A1	0.180	0.200	0.220
A2	0.300	0.325	0.350
b	0.235	0.260	0.285
D	1.250	1.280	1.310
E	1.280	1.310	1.340
e	0.400BSC		

Recommend Land Pattern



Recommended Land Pattern Unit (mm)

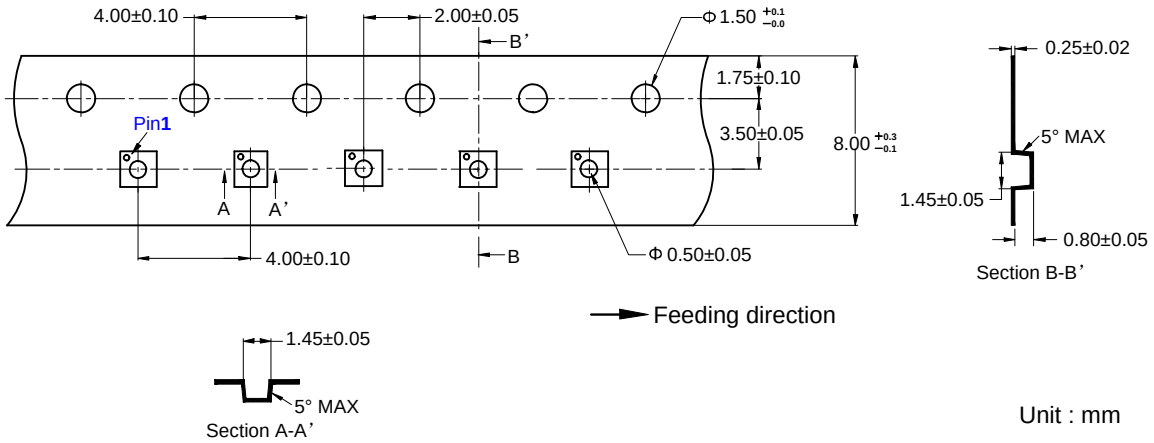
Marking Information



70 - Part Number

XXXXX - Tracking Number

Tape Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2021-06-25	First Version	Chenz	Chenz	Zhujl
1.1	2021-11-03	Add CDM Spec	Chenz	Chenz	Zhujl
1.2	2022-08-10	Update Typeset	Tianqh	Chenz	Zhujl
1.3	2022-12-13	Add tape information	Tianqh	Chenz	Zhujl
1.4	2023-10-23	Update marking	Shibo	Chenz	Liujy