Programmable USB Type-C Controller with Power Delivery PHY

General Description

The ET7301 is a programmable USB Type-Control IC. It supports the USB Type-C connector application with Configuration Channel (CC) control logic detection and indication functions. This products support a flexible hardware solution to configure DFP/UFP/DRP connection. It can connect to a controller through I^2C-bus interface. ET7301 performs USB Type-C detection including attach, detach and orientation. It setup VBUS threshold detection automatically as well as the various charging current levels. ET7301 provide the software flexibility for multiple platform support.

The ET7301 integrates the physical layer of the USB BMC PD (Power Delivery) protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

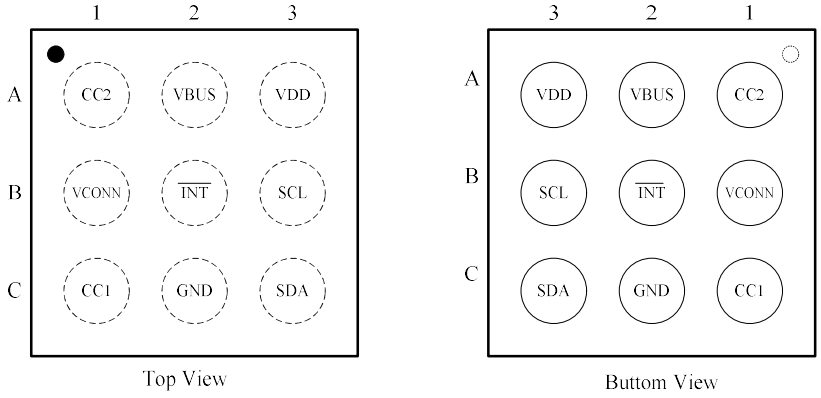
Features

- Dual-Role Functionality with Autonomous DRP Toggle
- Software configurable either as a dedicated host, dedicated device, or dual role. Dedicated devices can operate both on a Type-C receptacle or a Type-C plug with a fixed CC and VCONN channel
- Full Type-C Specification 1.1 support. Configuration Channel (CC)
  - Role Detection and Configuration :DFP/UFP/DRP
  - Type-C USB Port Detection of Attach and Orientation
  - Type-C Current Mode
  - Audio Adapter Accessory Mode
  - Debug Accessory Mode
  - Active Cable Detection
- USB Power Delivery(PD) Specification2.0, Version 1.1 Support
  - Automatic GoodCRC Packet Response
  - Automatic retries of sending a packet if a GoodCRC is not received
  - Automatic soft reset packet sent with retries if needed
  - Automatic Hard Reset Ordered Set Sent
- Dead Battery Support (SNK Mode Support when No Power Applied)
- High Speed I^2C Interface
- Supply Voltage:2.8V to 5.5V
- Low Standby Supply Current: I_{DD} =25uA (Typical)
- Package:WLCSP-9 (ET7301),QFN14(ET7301Y)

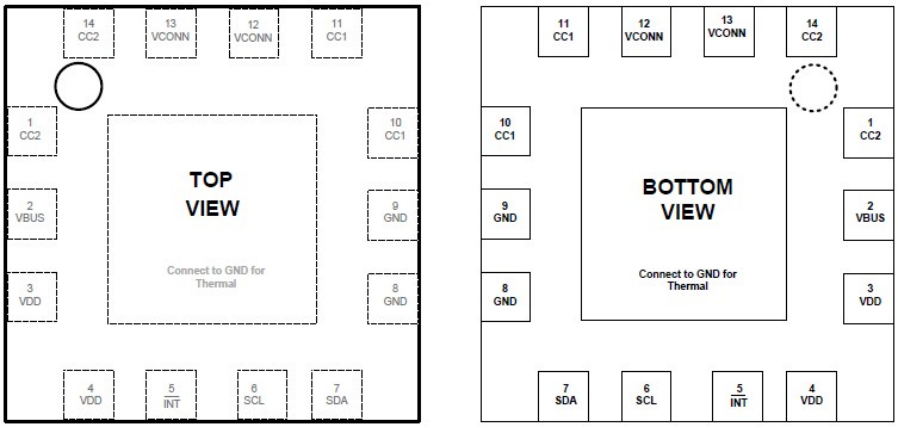
Application

- Host, Device, Dual Role Port Applications
- Smartphones, Tablets and Notebooks
- USB Peripherals

Pin Configuration



CSP9



QFN14

Figure 1. Pin Assignment

Pin Function

QFN14 Pin No.	CSP9 Pin No.	Name	Description
1，14	A1	CC2	Type-C Connector Configuration Channel Pin2
2	A2	VBUS	USB VBUS Detect Terminal .Expected to be an OVP protect input
3，4	A3	VDD	Positive Supply
13	B1	VCONN	Regulated Power input For USB3.1 Full Featured Cables Or Other Accessories
5	B2	$\overline{INT}$	Interrupt Terminal to u-Processor Indicating Register Update (Low Active Open-drain Output)
6	B3	SCL	I^2C communication clock signal
10，11	C1	CC1	Type-C Connector Configuration Channel Pin1
8，9	C2	GND	Ground (All ground must connected together in application)
7	C3	SDA	I^2C communication data signal

Block Diagram

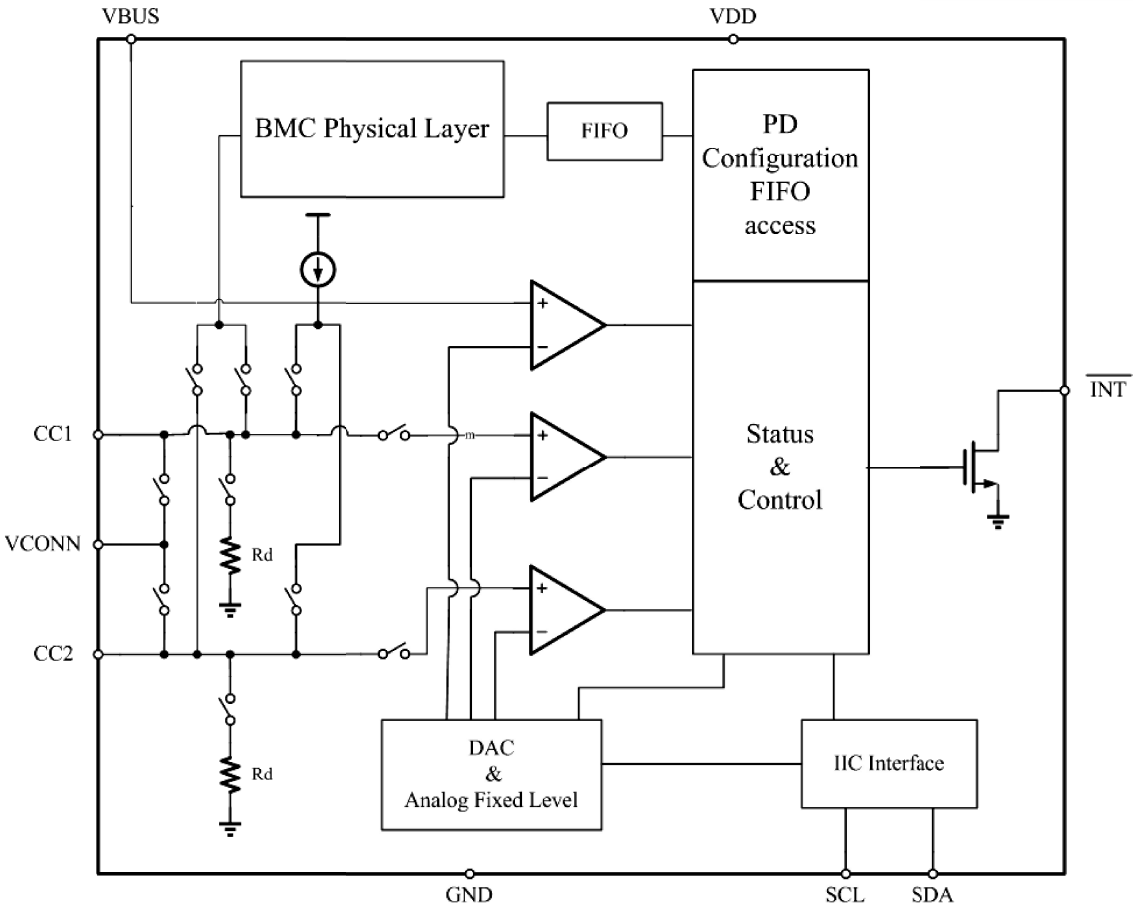


Figure 2. Function Block

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min	Max	Unit
V_{BUS} to GND	VBUS Voltage	-0.3	28	V
V_{DD} to GND	Supply Voltage	-0.3	6	V
V_{IN}	Input Voltage	-0.3	6	V
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
P_D	Power Dissipation		400	mW
ESD/Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
	Charged Device Model,JESD22-C101		1	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ET7301 does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min	Max	Unit
V_{BUS}To GND	VBUS Voltage	GND=0V	4.0	28	V
V_{DD}To GND	Power Supply Voltage	GND=0V	2.8	5.5	V
V_{CONN} To GND	VCONN Supply Voltage	GND=0V	2.7	5.5	V
Ivconn	VCONN Supply Current			560	mA
I_{OH}/I_{OL}	Output Sink/Source Current	V_{BAT}=4.2V		200	mA
T_A	Operating Temperature, Free Air		-40	+85	°C

Electrical Characteristic

(T_A=-40 to +85°C, T_J=-40 to +125°C, All typical values are at T_A=25°C unless otherwise specified.)

Type-C CC Switches

Symbol	Parameter		Min	Typ	Max	Unit
R_{SW_CCX}	R_{DSON} for SW1_CC1 and SW1_CC2	VCONN to CC1 & CC2		0.4	1.2	Ω
I_{SW_CCX}	Over-Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range. OCPreg=0Fh		600	800	1000	mA
$t_{SoftStart}$	Time taken for the VCONN switch to turn on.		0.8	1.5	2.2	ms
I_{TOL_CCX}	Tolerance of CC Current to VDD of 80uA (default), 180uA (1.5A) and 320 uA (3A)		-8		8	%
R_{DEVICE}	Device Pull-down Resistance (VDD>3.0 V)		4.59	5.10	5.61	kΩ
	Device Pull-down Resistance (VDD=0V. CCx=2.2V)		4.08	5.10	6.20	kΩ
z_{OPEN}	CC Resistance for Disabled State		126			kΩ
$V_{WAKElow}$	Wake threshold for CC pin DFP or UFP LOW value. Assumes bandgap and wake circuit turned on ie PWR[0]=1			0.25		V
$V_{WAKEhigh}$	Wake threshold for CC pin DFP or UFP HIGH value. Assumes bandgap and wake circuit turned on ie PWR[0]=1			1.45		V
V_{BC_LVL}	CC Pin Thresholds. Assumes PWR=4'h7	BC=2'b00	0.15	0.20	0.25	V
		BC=2'b01	0.61	0.66	0.70	V
		BC=2'b10	1.16	1.23	1.31	V
V_{BC_LVLhys}	Hysteresis on the Ra and Rd Comparators			20		mV
$V_{MDACstep}$	Measure block MDAC step size for each code in MDAC[5:0] register. MEAS_VBUS=0			42		mV
	Measure block MDAC step size for each code in MDAC[5:0] register for VBUS measurement. MEAS_VBUS=1			420		mV
$V_{VBUSthr}$	VBUS threshold at which I_VBUSOK interrupt is triggered. Assumes measure block on ie; PWR[2]=1			4.0		V

t_{TOG1}	When TOGGLE=1, time at which internal versions of PU_EN1=PU_EN2=0 and PWDN1=PDWN2=1 selected to present externally as a SNK in the DRP toggle		30	45	60	ms
t_{TOG2}	When TOGGLE=1, time at which internal versions of PU_EN1=1 or PU_EN2=1 and PWDN1=PDWN2=0 selected to present externally as a SRC in the DRP toggle		20	30	40	ms
t_{DIS}	Disable time after a full toggle (t_{TOG1}+t_{TOG2}) cycle so as to save power	TOG_SAVE_PWR2:1=00		0		ms
		TOG_SAVE_PWR2:1=01		40		ms
		TOG_SAVE_PWR2:1=10		80		ms
		TOG_SAVE_PWR2:1=11		160		ms
T_{shut}	Temp. for Vconn Switch Off			145		℃
T_{hys}	Temp. Hysteresis for Vconn Switch Turn On			10		℃

Current Consumption

Symbol	Parameter	V_{DD}	Conditions	Min	Typ	Max	Unit
$I_{disable}$	Disabled Current	3.0 to 5.5 V	Nothing Attached, No I^2C Transactions. PWR[3:0]=0h		0.4	5	uA
I_{stdby}	Standby Current	3.0 to 5.5 V	Nothing attached, no I^2C traffic, PWR[3:0]=1h,WAKE_EN=0.TOGGLE= 1 TOG_SAVE_PWR[2:1]=01h		25	40	uA
$I_{pd\_stdby\_meas}$	BMC PD Standby Current	3.0 to 5.5 V	Device Attached, BMC PD Active But Not Sending or Receiving data. PWR[3:0]=7h		40		uA

Baseband PD

Symbol	Parameter	Min	Typ	Max	Unit
UI	Unit interval	3.03	3.35	3.7	us
Transmitter					
R_{Output}	TX Output Resistance	21	50	79	Ω
$t_{EndDriveBMC}$	Time to cease driving the line after the end of the last bit of the Frame			23	us
$t_{HoldLowBMC}$	Time to Cease Driving the Line after the final High-to-Low Transition	1			us
V_{OH}	Logic High Voltage	1.05		1.2	V
V_{OL}	Logic Low Voltage	0		75	mV
$t_{StartDrive}$	Time before the start of the first bit of the preamble when the transmitter shall start driving the line	-1		1	us
t_{RISE_TX}	Rise Time	300			ns
t_{FALL_TX}	Fall Time	300			ns
Receiver					
$C_{Receiver}$	Receiver Capacitance when Driver isn't Turned On		50		pF

z_{BmcRx}	Receiver Input Impedance	1			MΩ
$V_{SDACstep}$	BMC Receiver SDAC step size for each code in SDAC[5:0]register		17		mV
$V_{SDAChys}$	BMC Receiver SDAC hysteresis for each code over the SDAC range (SDAC_HYS=01)		85		mV
$t_{RxFilter}$	Rx Bandwidth Limiting Filter(2)	100			ns
$n_{TransitionCount}$	Transitions count in time window of 12 µs Min. and 20 µs Max.	3			edges
$t_{ACTIVITY}$	Time from the last BMC edge(1) to when ACTIVITY bit goes LOWin the STATUS register(2)	5		9	us

Notes:
1、The last BMC edge includes edge when BMC bus is not driven and thus voltage is the result of pull ups/pull downs to if/when it trips the SDAC receiver threshold to cause another BMC edge.
2、Guaranteed by characterization. Not production tested

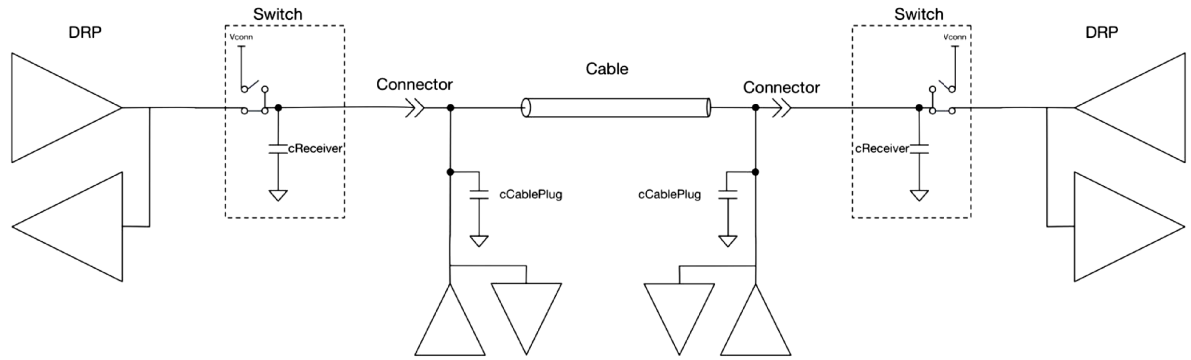


Figure 3. Transmitter Test Load

USB PD Specific Parameters

Symbol	Parameter	Min	Typ	Max	Unit
$t_{HardReset}$	If a Soft Reset message fails, a Hard Reset is sent after $t_{HardReset}$ of CRCReceive Timer expiring			5	ms
$t_{HardResetFinish}$	If the ET7301 cannot send a Hard Reset within $t_{HardResetFinish}$ time because of a busy line, then a I_HARDFAIL interrupt is triggered			5	ms
$t_{Receive}$	This is the value for which the CRCReceiveTimer expires. The CRCReceiveTimer is started upon the last bit of the EOP of the transmitted packet	0.9		1.1	ms
t_{Retry}	Once the CRCReceiveTimer expires, a retry packet has to be sent out within t_{Retry} time. This time is hard to separate externally from $t_{Receive}$ since they both happen sequentially with no visible difference in the CC output			75	us
$t_{SoftReset}$	If a GoodCRC packet is not received within $t_{Receive}$ for N_RETRIES then a Soft Reset packet is sent within $t_{SoftReset}$ time.			5	ms
$t_{Transmit}$	From receiving a packet, we have to send a GoodCRC in response within $t_{Transmit}$ time. It is measured from the last bit of the EOP ofthe received packet to the first bit sent of the preamble of the GoodCRC packet			195	us

IO Specifications (VDD=3.0V to 5.5V)(3)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL_INTN}	INT_N Output Low Voltage (I_{OL}=4mA)			0.4	V
T_{INT_Mask}	Time from global interrupt mask bit cleared to INT_N goes LOW	50			us
V_{ILI2C}	Low-Level Input Voltage			0.51	V
V_{IHI2C}	High-Level Input Voltage	1.32			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	0.09			V
I_{I2C}	Input Current of SDA and SCL Pins (Input Voltage 0.26V to 2V)	-10		10	uA
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH (Input Voltage 1.8V)	-10		10	uA
V_{OLSDA}	SDA Open-Drain Low-Level Output Voltage (I_{OL}=3mA)	0		0.3	V
I_{OLSDA}	SDA Open-Drain Low-Level Output Current(V_{OLSDA}=0.4V)	20			mA
C_I	Capacitance for Each I/O Pin		5		pF

Note: 3、The external I^2C pull-up voltage must be between 1.71V and VDD.

I^2C Specifications Fast Mode I^2C Specification (Fast Mode)

Symbol	Parameter	Min	Max	Unit
f_{SCL}	I^2C SCL Clock Frequency	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.26		us
t_{LOW}	Low Period of I^2C SCL Clock	0.5		us
t_{HIGH}	High Period of I^2C SCL Clock	0.26		us
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.26		us
$t_{HD;DAT}$	Data Hold Time	0		us
$t_{SU;DAT}$	Data Set-up Time(1)	50		ns
tr	Rise Time of I^2C_SDA and I^2C_SCL Signals(2)		120	ns
tf	Fall Time of I^2C_SDA and I^2C_SCL Signals(2)	6	120	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.26		us
t_{BUF}	Bus-Free Time between STOP and START Conditions	0.5		us
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns
C_b	Capacitive Load for each Bus Line		550	pF

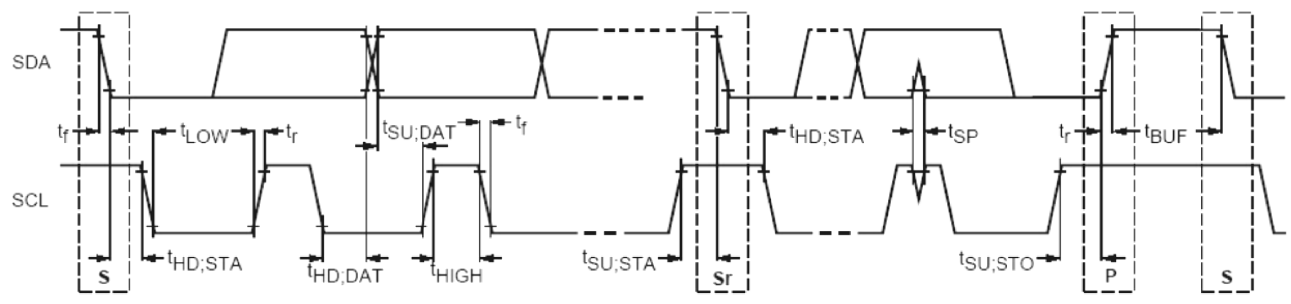


Figure 4. Definition of Timing for Full-Speed Mode Devices on the I^2C Bus

Function Description

Configuration Channel Switch

The ET7301 integrates the control and detection functionality required to implement a USB Type-C host, device or dual-role port including: CC Pull-Down(RD)，Pull-Up (Ip)，VCONN Power Switch，USB BMC Power Delivery Physical Layer and CCx Threshold Comparators. Each CCx pin contains a flexible switch matrix that allows the host software to control what type of Type-C port is implemented. The switches are shown in Figure 5.

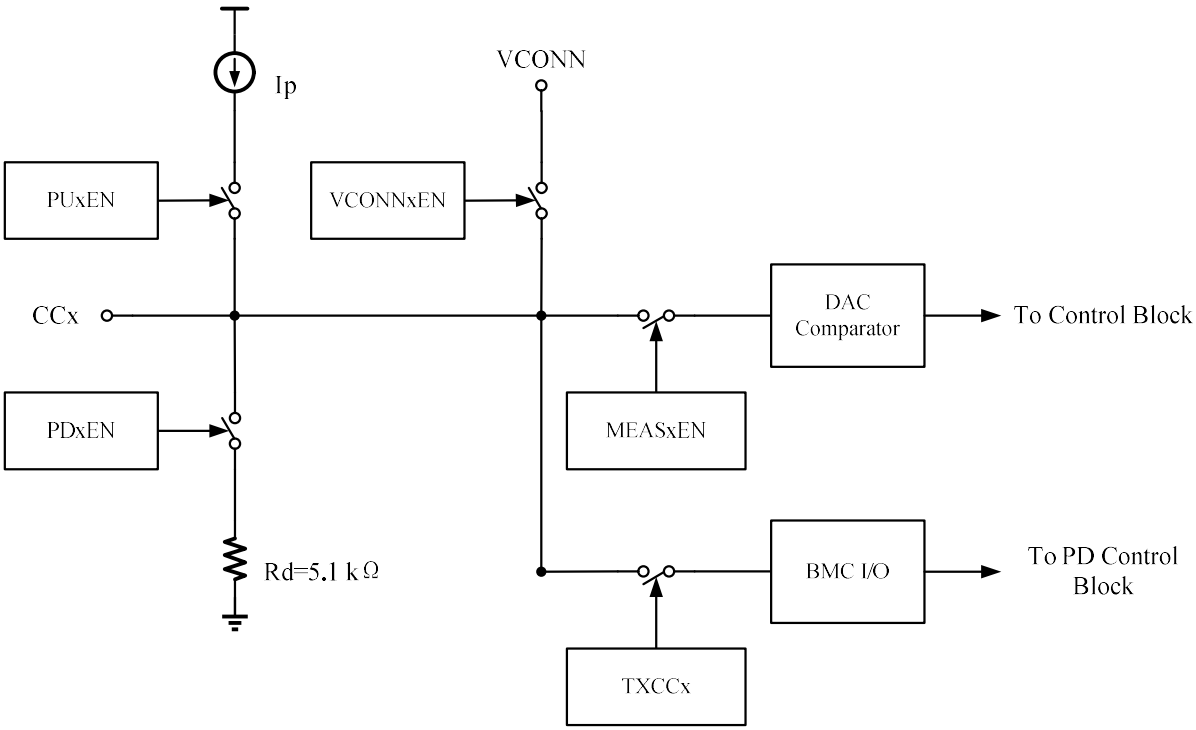


Figure 5. Configuration Channel Switch

Type-C Detection

The ET7301 implements multiple comparators and a programmable DAC that can be used by software to determine the state of the CC and VBUS pins. This status information provides the software all the information required to determine attach, detach and charging current capabilities based on the specific Type-C port to which the ET7301 has been configured.

The ET7301 has three fixed threshold comparators that match the USB Type-C specification for the threecharging current levels that can be detected by a Type-C device. These comparators automatically cause a BC_LVL interrupt to occur when there is a change of state. In addition to the fixed threshold comparators, the host software can use the 6-bit DAC to determine the state of the CC lines more accurately.

The ET7301 also has a fixed comparator that monitors if VBUS has reached a valid threshold or not. The DAC can be used to measure VBUS up to 26.88V which allows the software to confirm that changes to the VBUS line have occurred as expected based on various communication methods to change the charging level.

Detection through Autonomous Device Toggle

The ET7301 has the capability to do autonomous DRP toggle. In autonomous toggle the ET7301 internally controls the PDWN1, PDWN2, PU_EN1 and PU_EN2, MEAS_CC1 and MEAS_CC2 and implements a fixed

DRP toggle between presenting as a SRC and presenting as a SNK. Alternately, it can present as a SRC or SNK only and poll CC1 and CC2 continuously.

Autonomous Device Toggle register setup through I^2C.

Registers/Bits	Value
TOGGLE	1
HOST_CUR0	1
HOST_CUR1	0
MEAS_VBUS	0
VCONN_CC1	0
VCONN_CC2	0
Mask Register	0xFE
Maska Register	0xBF
Maskb Register(Except I_TOGDONE and I_BC_LVL Interrupt)	0x01
PWR[3:0]	0x07

Toggle Functionality

When TOGGLE bit (Control2 register) is set the ET7301 implements a fixed DRP toggle between presenting as a SRC and as a SNK. It can also be configured to present as a SRC only or SNK only and poll CC1 and CC2 continuously. This operation is turned on with TOGGLE=1 and the processor should initially. Write HOST_CUR1=0, HOST_CUR0=1(for default current) ,VCONN_CC1=VCONN_CC2=0, Mask Register=0xFE, Maska register=0xBF, and Maskb register=0x01, and PWR=0x07. It returns I_TOGDONE and TOGSS1/2. The processor should also read the interrupt register to clear them prior to setting the TOGGLE bit.

Manual Device Toggle

The ET7301 has the capability to do manual DRP toggle. In manual toggle the ET7301 is configurable by the processor software by I^2C and setting TOGGLE=0.

Initial Attach Detection

The ET7301 implements the Type-C Disabled state which removes all termination from the CC pins. In this state, the ET7301 monitors the CC pins for any activity which indicates that either a host or a device is attempting to attach. When the ET7301 detects this activity, it interrupts the host software through the WAKE interrupt. The host software can then enable the desired termination based on the required port type and validate the attach per the Type-C specification.

Manual Device Detection and Configuration (UFP)

A Type-C device must monitor VBUS to determine if it is attached or detached. The ET7301 provides this information through the VBUSOK interrupt. After the Type-C device knows that a Type-C host has been attached, it needs to determine what type of termination is applied to each CC pin. The software determines if an Ra or Rd termination is present based on the BC_LVL and COMP interrupt and status bits.

Additionally, for Rd terminations, the software can further determine what charging current is allowed by the Type-C host by reading the BC_LVL status bits. This is summarized in Table 1.

Table 1. Device Interrupt Summary

Status Type	Interrupt Status				Meaning
	BC_LVL[1 :0]	COMP	COMP Setting	VBUSOK	
CC Detection	2'b00	NA	NA	1	vRA
	2'b01	NA	NA	1	vRd-Connect and vRd-USB
	2'b10	NA	NA	1	vRd-Connect and vRd-1.5
	2'b11	0	6'b11_0100 (2.05 V)	1	vRd-Connect and vRd-3.0
Attach	NA	NA	NA	1	Host Attached, VBUS Valid
Detach	NA	NA	NA	0	Host Detached, VBUS Invalid

The high level software flow diagram for a Type-C device (UFP) is shown in Figure 6.

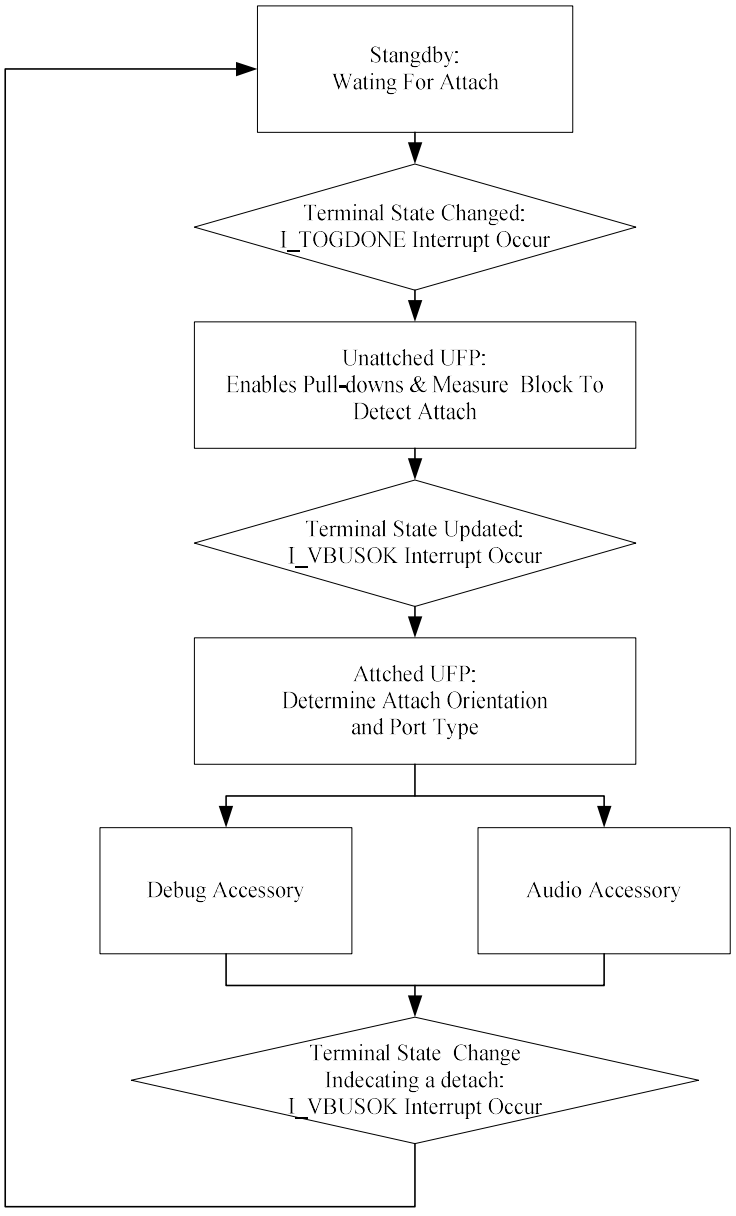


Figure 6.UFP Software Flow

Manual Host Detection and Configuration (DFP)

When the ET7301 is configured as a Type-C host, the software can use the status of the comparators and DAC to determine when a Type-C device has been attached or detached and what termination type has been attached to each CC pin.

The ET7301 allows the host software to change the charging current capabilities of the port through the HOST_CUR control bits. If the HOST_CUR bits are changed prior to attach, the ET7301 will automatically indicate the programmed current capability when a device is attached. If the current capabilities are changed after a device is attached, the ET7301 will immediately change the CC line to the programmed capability.

The Type-C specification outlines different attach and detach thresholds for a Type-C host that are based on how much current is supplied to each CC pin. Based on the programmed HOST_CUR setting, the software adjusts the DAC comparator threshold to match the Type-C specification requirements. The BC_LVL comparators can also be used as part of the Ra detection flow. This is summarized in Table 2.

Table 2. Host Interrupt Summary

Termination	HOST_CUR[1:0]	Interrupt Status			Attach/Detach
		BC_LVL[1:0]	COMP	COMP Setting	
Ra	2'b01	2'b00	NA	NA	NA
	2'b10	2'b01	0	6'b00_1000 (0.4 V)	
	2'b11	2'b10	0	6'b01_0010 (0.8 V)	
Rd	2'b01,2'b10	NA	0	6'b10_0100 (1.6 V)	Attach
		NA	1	6'b10_0100 (1.6 V)	Detach
	2'b11	NA	0	6'b11_1101 (2.6 V)	Attach
		NA	1	6'b11_1101 (2.6 V)	Detach

The high level software flow diagram for a Type-C Host (DFP) is shown below in Figure 7.

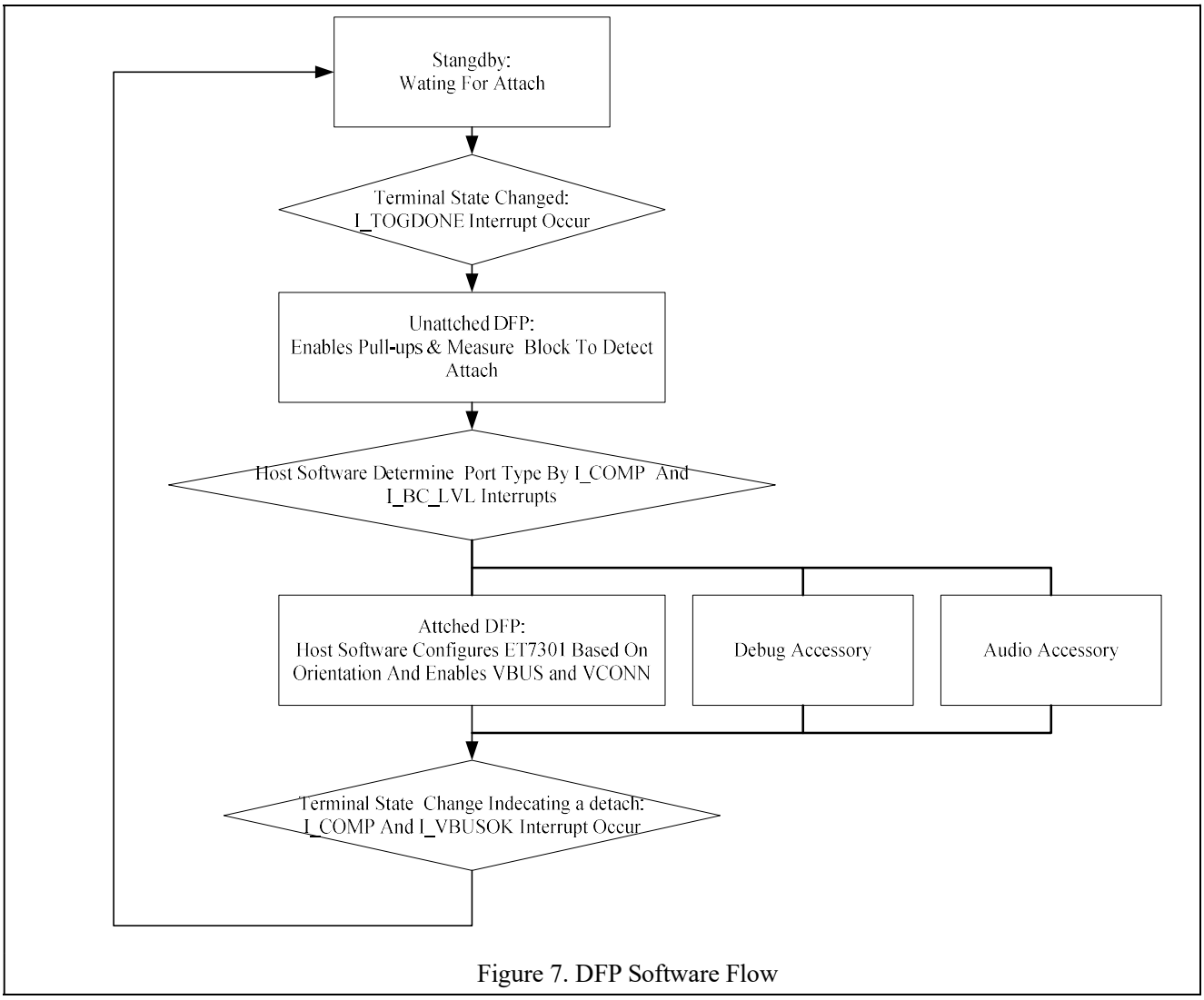


Figure 7. DFP Software Flow

Manual Dual-Role Detection and Configuration (DRP)

The Type-C specification allows ports to be both a device or a host depending on what type of port has attached. This functionality is similar to USB OTG ports with the current USB connectors and is called a dual-role port. The ET7301 can be used to implement a dual-role port. A Type-C dual role port toggles between presenting as a Type-C device and a Type-C host. The host software controls the toggle time and configuration of the ET7301 in each state as shown in Figure 8.

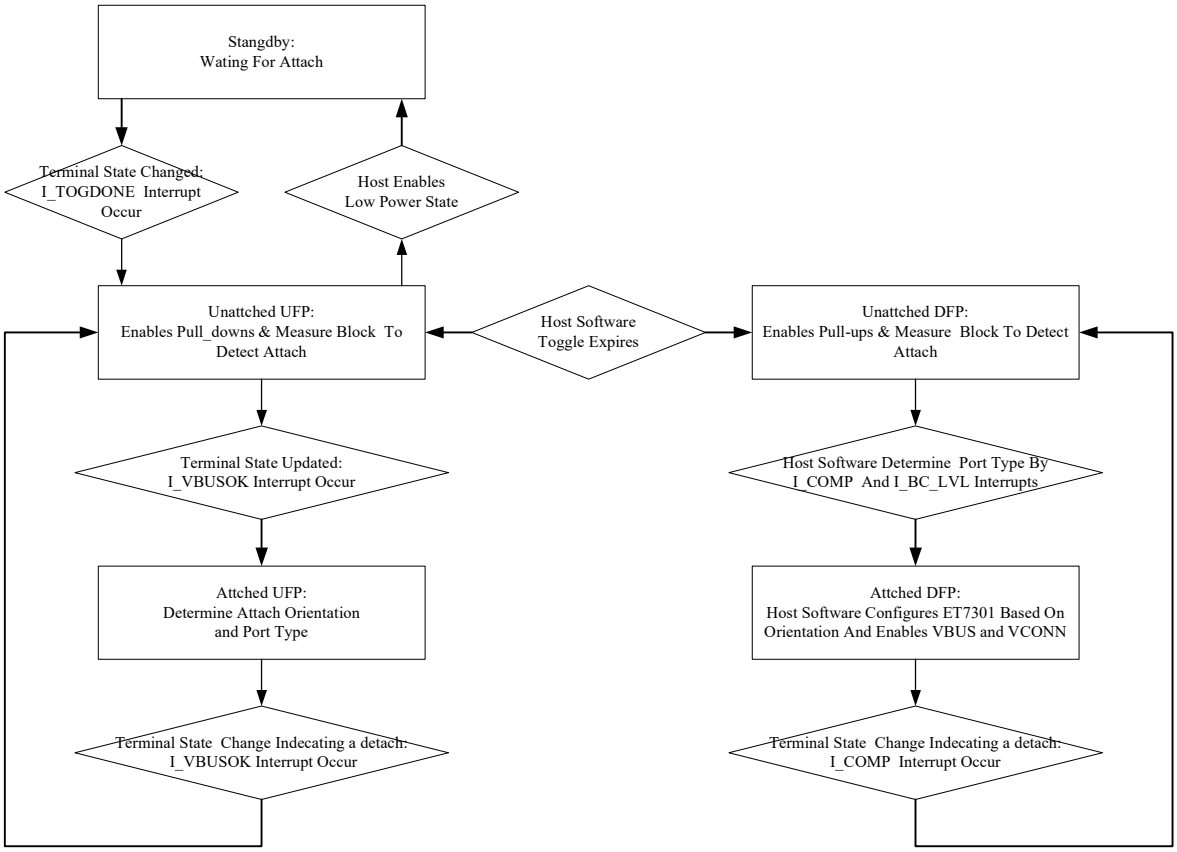


Figure 8. DRP Software Flow

Power Level Determination

The Type-C specification outlines the order of precedence for power level determination which covers power levels from basic USB2.0 levels to the highest levels of USB PD. The host software is expected to follow the USB Type-C specification for charging current priority based on feedback from the ET7301 detection, external BC1.2 detection and any USB Power Delivery communication.

The ET7301 does not integrate BC1.2 charger detection which is assumed available in the USB transceiver or USB charger in the system.

Power Up, Initialization and Reset

When power is first applied through VDD, the ET7301 is reset and registers are initialized to the default values shown in the register map. ET7301 can be reset through software by programming the SW_RES bit in the RESET register.

To properly configure the device in low power operation, place a 0.2uF cap on each CC pin and set the registers to default by programming the SW_RES bit.

BMC Power Delivery

The Type-C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol and is used for many different reasons with the Type-C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels

- Alternative Interfaces such as MHL, Display Port
- Vendor specific interfaces for use with custom docks or accessories
- Role swap for dual-role ports that want to switch who is the host or device
- Communication with USB3.1 full featured cables

All Messages shall be composed of a Message Header and a variable length (including zero) data portion. A Message either originates in the Protocol Layer and is passed to the Physical Layer, or it is received by the Physical Layer and is passed to the Protocol Layer.(Please see the Power Delivery Specification)

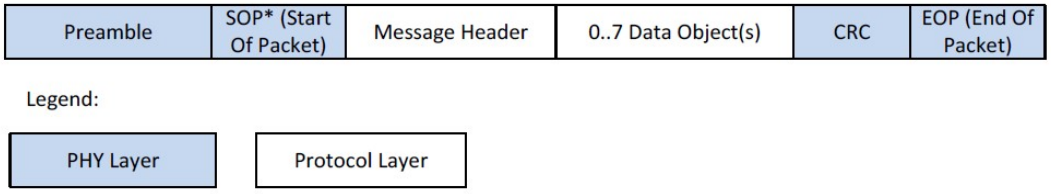


Figure 9.USB Power Delivery Packet Format including Message Payload

The ET7301 integrates a thin BMC PD client which includes the BMC physical layer and packet FIFOs (48 bytes for transmit and 80 bytes for receive) which allows packets to be sent and received by the host software through I^2C accesses. The ET7301 allows host software to implement all features of USB BMC PD through writes and reads of the FIFO and control of the ET7301 physical interface.

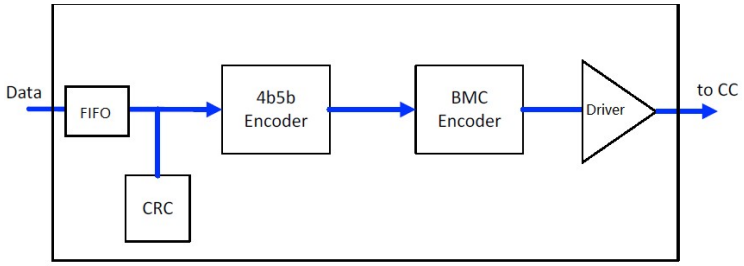


Figure 10. ET7301 BMC Transmitter Block Diagram

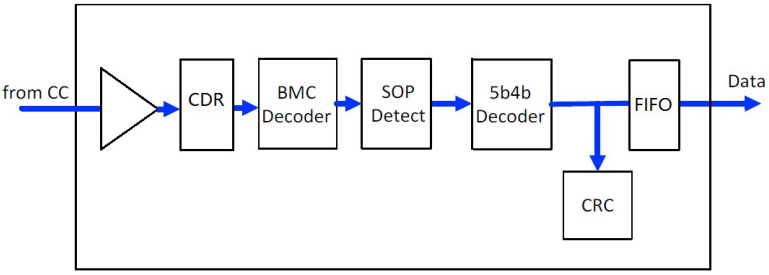


Figure 11. ET7301 BMC Receiver Block Diagram

The ET7301 uses tokens to control the transmission of BMC PD packets. These tokens are written to the transmit FIFO and control how the packet is transmitted on the CC pin. The tokens are designed to be flexible and support all aspects of the USB PD specification. The ET7301 additionally enables control of the BMC transmitter through tokens. The transmitter can be enabled or disabled by specific token writes which allow faster packet processing by burst writing the FIFO with all the information required to transmit a packet.

The ET7301 receiver stores the received data and the received CRC in the receive FIFO when a valid packet is received on the CC pin. The BMC receiver automatically enables the internal oscillator , when activity is sensed on the CC pin , and load the FIFO when a packet is received. The I_ACTIVITY and I_CRC_CHK interrupts alert the host software that a valid packet was received.

PD Automatic Sending Retries

If GoodCRC packet is not received and AUTO_RETRY is set, then a retry of the same message that was in the TxFIFO written by the processor is executed within t_{Retry} and that is repeated for N_RETRY times.

PD Send Soft Reset

If the correct GoodCRC packet is still not received for all retries then I_RETRYFAIL interrupt is triggered and if AUTO_SOFT_RESET is set, then a Soft Reset packet is created (MessageID is set to 0 and the processor upon servicing I_RETRYFAIL would set the true MessageID Counter to 0. If this Soft Reset is sent successfully where a GoodCRC control packet is received with a MessageID=0 then I_TXSENT interrupt occurs. If no power applied to VDD, then the SRC can recognize the ET7301 as a SNK.

PD Automatic Receive GoodCRC

The power delivery packets require a GoodCRC acknowledge packet to be sent for each received packet where the calculated CRC is the correct value. This calculation is done by the ET7301 and triggers the I_CRC_CHK interrupt if the CRC is good. If the AUTO_CRC (Switches1 register bit) is set and AUTO_PRE=0, then the ET7301 will automatically send the GoodCRC control packet in response to alleviate the local processor from responding quickly to the received packet. If GoodCRC is required for anything beyond SOP, then enable SOP*.

PD Send

The ET7301 implements part of the PD protocol layer for sending packets in an autonomous fashion. If not, this Soft Reset packet is retried N_RETRIES times (MessageID is always 0 for all retries) if a GoodCRC acknowledge packet is not received with CRCReceive Timer expiring ($t_{Receive}$ of 1.1 ms max). If all retries fail, then I_SOFTFAIL interrupt is triggered.

PD Send Hard Reset

If all retries of the soft reset packet fail and if AUTO_HARD_RESET is set, then a hard reset ordered set is sent by loading up the TxFIFO with RESET1, RESET1, RESET1, RESET2 and sending a hard reset. Note only one hard reset is sent since the typical retry mechanism doesn't apply. The processor's policy engine firmware is responsible for retrying the hard reset is it doesn't receive the required response.

Software Model

Port software interacts with the port chip in two primary ways:

- I^2C Registers
- 8 bit data tokens sent to or received from the FIFO register.
- All reserved bits written in the TxFIFO should be 0 and all reserved bit read from the RxFIFO should be ignored.

Transmit Data Tokens

Transmit data tokens provide in-sequence transmit control and data for the transmit logic. Note that the token codes, and their equivalent USB PD K-Code are not the same. Tokens are read one at a time when they reach the end of the TX FIFO. I.e., the specified token action is performed before the next token is read from the TX FIFO.

The tokens are defined as follows:

Code	Name	Bytes	Description
101xxxx1 (0xA1)	TXON	1	Alternative method for starting the transmitter with the TX-START bit. This is not a token written to the TxFIFO but a command much like TX_START but it is more convenient to write it while writing to the TxFIFO in one contiguous write operation. It is preferred that the TxFIFO is first written with data and then TXON or TX_START is executed. It is expected that A1h will be written for TXON not any other bits where x is non-zero such as B1h, BFh, etc
0x12	SOP1	1	When reaching the end of the FIFO causes a Sync-1 symbol to be transmitted.
0x13	SOP2	1	When reaching the end of the FIFO causes a Sync-2 symbol to be transmitted.
0x1B	SOP3	1	When reaching the end of the FIFO causes a Sync-3 symbol to be transmitted.
0x15	RESET1	1	When reaching the end of the FIFO causes a RST-1 symbol to be transmitted.
0x16	RESET2	1	When reaching the end of the FIFO causes a RST-2 symbol to be transmitted.
0x80	PACKSYM	1+N	This data token must be immediately followed by a sequence of N packed data bytes. This token is defined by the 3 MSB‟s being set to 3’b100. The 5 LSB’s are the number of packed bytes being sent. Note: N cannot be less than 2 since the minimum control packet has a header that is 2 bytes and N cannot be greater than 30 since the maximum data packet has 30 bytes (2 byte header +7 data objects each having 4 bytes) Packed data bytes have two 4 bit data fields. The 4 LSB‟s are sent first, after 4b5b conversion etc in the chip.
0xFF	JAM_CRC	1	Causes the CRC, calculated by the hardware, to be inserted into the transmit stream when this token reaches the end of the TX FIFO.
0x14	EOP	1	Causes an EOP symbol to be sent when this token reaches the end of the TX FIFO.
0xFE	TXOFF	1	Turn off the transmit driver. Typically the next symbol after EOP

Receive Data Tokens

Receive data tokens provide in-sequence receive control and data for the receive logic. The RxFIFO can absorb as many packets as the number of bytes in the RxFIFO (80 bytes). The tokens are defined as follows:

Code	Name	Bytes	Description
111b_bbbb	SOP	1	First byte of a received packet to indicate that the packet is an SOP packet (“b” is undefined and can be any bit)
110b_bbbb	SOP1	1	First byte of a received packet to indicate that the packet is an SOP’ packet and occurs only if ENSOP1=1 (“b” is undefined and can be any bit)
101b_bbbb	SOP2	1	First byte of a received packet to indicate that the packet is an SOP” packet and occurs only if ENSOP2=1 (“b” is undefined and can be any bit)
100b_bbbb	SOP1DB	1	First byte of a received packet to indicate that the packet is an SOP’_DEBUG

			packet and occurs only if ENSOP1DB=1 (“b” is undefined and can be any bit)
011b_bbbb	SOP2DB	1	First byte of a received packet to indicate that the packet is an SOP”_DEBUG packet and occurs only if ENSOP2DB=1 (“b” is undefined and can be any bit)
010b_bbbb 001b_bbbb 000b_bbbb	Do Not Use	1	These can be used in future versions of this device and should not be relied on to be any special value. (“b” is undefined and can be any bit)

I²C Interface

The ET7301 includes a full I²C slave controller. The I²C slave fully complies with the I²C specificationVersion 6 requirements. This block is designed for fast mode. Examples of an I²C write and read sequence are shown in Figure 12 and Figure 13 respectively.

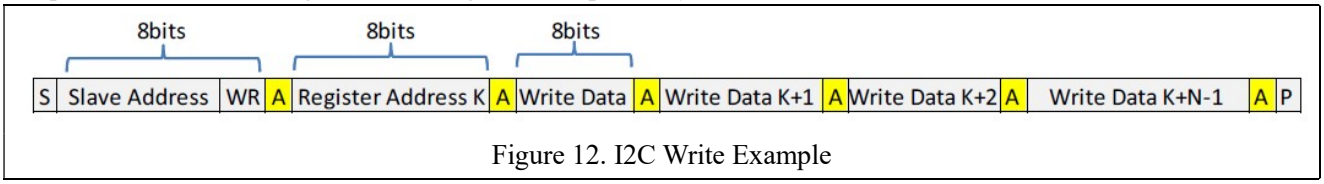


Figure 12. I2C Write Example

Note: Single Byte read is initiated by Master with P immediately following first data byte.

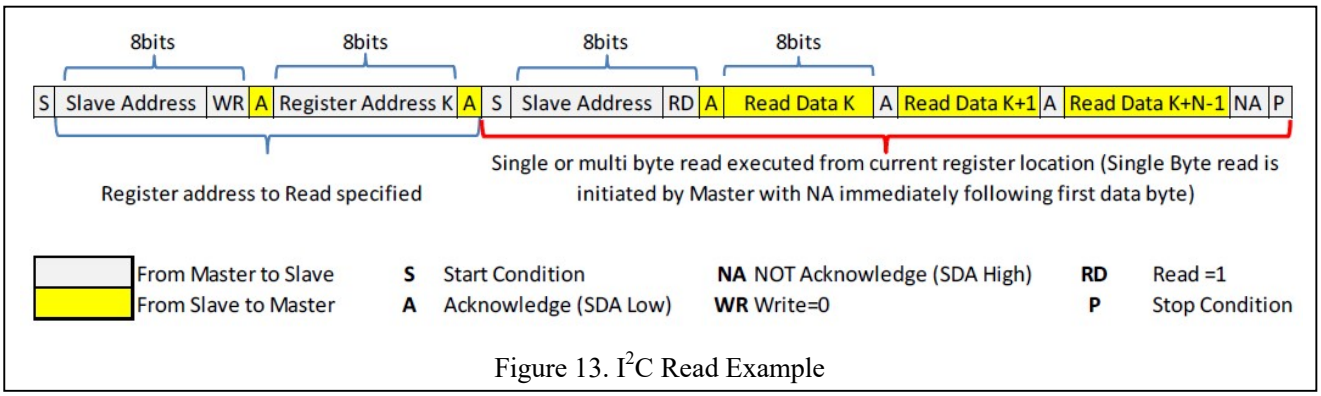


Figure 13. I²C Read Example

Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

Table 3. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	0	1	0	R/W

Register Definitions

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Device ID	R	8x	Version ID[3:0]				Revision ID[3:0]			
0x02	Switches0	R/W	03	PU_EN2	PU_EN1	VCONN_CC2	VCONN_QC1	MEAS_CC2	MEAS_CC1	PDWN2	PDWN1
0x03	Switches1	R/W	20	POWERROLE	SPECRREV1	SPECREV0	DATAROLE		AUTO_CRC	TXCC2	TXCC1
0x04	Measure	R/W	31		MEAS_VBUS	MDAC5	MDAC4	MDAC3	MDAC2	MDAC1	MDACO
0x05	Slice	R/W	60	SDAC_HYS1	SDAC_HYS2	SDAC5	SDAC4	SDAC3	SDAC2	SDAC1	SDAC0
0x06	Control0	R/W/C	24		TX_FLUSH	I NT_MASK		HOST_CUR1	HOST_CURO	AUTO_PRE	TX_START
0x07	Control1	R/W/C	00		ENSOP2DB	ENSOP1DB	BIST_MODE2		RX_FLUSH	ENSOP2	ENSOP1
0x08	Control2	R/W	02	TOPG_SAVE_ PWR2	TOPG_SAVE_ PWR2	TOG_RD_ONLY		WAKE_EN	MODE[1:0]		TOGGLE
0x09	Control3	R/W	06		SEND HARD RESET		AUTO HARD RESET	AUTO SOFT RESET	N_RETRIES[1:0]		AUTO_RETRY
0x0A	Mask1	R/W	00	M_VBUSOK	M_ACTIVITY	M_COMP_CHNG	M_CRC_CHK	M_ALERT	M_WAKE	M_COLLISION	M_BC_LVL
0x0B	Power	R/W	01					PWR3	PWR2	PWR1	PWR0
0x0C	Reset	W/C	00							PD_RESET	SW_RES
0x0D	OCPreg	R/W	0F					OCP_RANGE	OCP_CUR2	OCP_CUR1	OCP_CUR0
0x0E	Maska	R/W	00	M_OCP_TEMP	M_TOGDONE	M_SOFTFAIL	M_RETRYFAIL	M_HARDSENT	M_TXSENT	M_SOFTRST	M_HARDRST
0x0F	Maskb	R/W	00								M_GCRCSENT
0x3C	Status 0a	R	00			SOFTFAIL	RETRYFAIL	POWER3	POWER2	SOFTRST	HARDRST
0x3D	Status 1a	R	00			TOGSS3	TOGSS2	TOGSS1	RXSOP2DB	RXSOP1DB	RXSOP
0x3E	Interrupta	R/C	00	I_OCP_TEMP	I_TOGDONE	I_SOFTFAIL	I_RETRYFAIL	I_HARDSENT	I_TXSENT	I_SOFTRST	I_HARDRST
0x3F	Interrupt	R/C	00								I_GCRCSENT
0x40	Status0	R	00	VBUSOK	ACTIVITY	COMP	CRC_CHK	ALERT	WAKE	BC_LVL1	BC_LVL0
0x41	Status1	R	28	RXSOP2	RXSOP1	RX_EMPTY	RX_FULL	TX_EMPTY	TX_FULL	OVRTEMP	OCP
0x42	Interrupt	R/C	00	I_VBUSOK	I_ ACTIVITY	I_COMP_CHNG	I_ CRC_CHK	I_ ALERT	I_WAKE	I_COLLISION	I_BC_LVL
0x43	FIFOs	R/W(11)	00	Write to TX FIFO or read from RX FIFO repeatedly without address auto increment							

Type C Bits	USB PD Bits	General Bits

Notes:

1. Do not use registers that are blank.
2. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers.
3. .FIFO register is serially read/written without auto address increment.

Address: 01h**-- Device ID**

Reset Value: 0x1000_00XX

Type: Read

Bit	Name	Description
7:4	Version ID	Device version ID
3:0	Revision ID	Revision History of each version

Address: 02h**-- Switches0**

Reset Value: 0x0000_0011

Type: Read/write

Bit	Name	Description
7	PU_EN2	1: Enable host pull up current to CC2 pin based on Control0 register HOST_CUR[1 :0] setting
6	PU_EN1	1: Enable host pull up current to CC1 pin based on Control0 register HOST_CUR[1 :0] setting
5	VCONN _CC2	1: Enable the VCONN pin to CC2 pin switch
4	VCONN - CC1	1: Enable the VCONN pin to CC1 pin switch
3	MEAS_CC2	1: Connect the measure block to CC2 pin to monitor or measure the voltage on CC2 pin. Note, PWR=0x07 for proper operation
2	MEAS_CC1	1: Connect the measure block to CC1 pin to monitor or measure the voltage on CC1 pin. Note, PWR=0x07 for proper operation
1	PDWN2	1: Enable Device pull down on CC2 pin
0	PDWN1	1: Enable Device pull down on CC1 pin

Address: 03h**—Switches1**

Reset Value: 0x0010_0000

Type: Read/write

Bit	Name	Description
7	POWERROLE	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Power Role bit in the message header if an SOP packet is received 1: Source if SOP 0: Sink if SOP
6:5	SPECREV[1:0]	Bit used for constructing the GoodCRC acknowledge packet. These bits correspond to the Specification Revision bits in the message header 00: Revision 1.0 01: Revision 2.0 10, 11: Do Not Use

4	DATAROLE	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Data Role bit in the message header. For SOP: 1: SRC 0: SNK
3	Reserved	Do Not Use
2	AUTO_CRC	1: Starts the transmitter automatically when a message with a goodCRC is received and automatically sends a GoodCRC acknowledge packet back to the relevant SOP* 0: Feature disabled
1	TXCC2	1: Enable BMC transmit driver on CC2 pin
0	TXCC1	1: Enable BMC transmit driver on CC1 pin

Address: 04h--**Measure**

Reset Value: 0x0011_0001

Type: Read/Write

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved</td><td>Do Not Use</td></tr>
<tr><td>6</td><td>MEAS_VBUS</td><td>1: Measure VBUS with the MDAC/comparator. This requires MEAS_CCx bits in Switches0 register to be 0
0: MDAC/comparator measurement is controlled by MEAS_CCx bits</td></tr>
<tr><td>5:0</td><td>MDAC[5:0]</td><td>Measure Block DAC data input. The step size is $v_{MDACstepCC}$ which is dependent on Meas_VBUS register setting. Examples are shown below. Valid values from 00_0000 to 11_1111 for MEAS_VBUS=1
<table>
<tr><th>MDAC[5:0]</th><th>MEAS_VBUS=0</th><th>MEAS_VBUS=1</th><th>Unit</th></tr>
<tr><td>00_0000</td><td>0.042</td><td>0.420</td><td>V</td></tr>
<tr><td>00_0001</td><td>0.084</td><td>0.840</td><td>V</td></tr>
<tr><td>11_0000</td><td>2.058</td><td>20.58</td><td>V</td></tr>
<tr><td>11_0011</td><td>2.184</td><td>21.84</td><td>V</td></tr>
<tr><td>11_1110</td><td>2.646</td><td>26.46</td><td>V</td></tr>
<tr><td>11 1111</td><td>>2.688</td><td>26.88</td><td>V</td></tr>
</table></td></tr>
</table>

Address: 05h--**Slice**

Reset Value: 0x0110_0000

Type: Read/Write

Bit	Name	Description
7:6	SDAC_HYS[1:0]	Adds hysteresis where there are now two thresholds, the lower threshold which is always the value programmed by SDAC[5:0] and the higher threshold that is: 11: 255 mV hysteresis: higher threshold = (SDAC value + 20hex) 10 :170 mV hysteresis: higher threshold = (SDAC value + 0Ahex) 01 :85 mV hysteresis: higher threshold = (SDAC value + 05hex) 00 : No hysteresis: higher threshold = SDAC value
5:0	SDAC[5:0]	BMC Slicer DAC data input. Allows for a programmable threshold so as to meet the BMC receive mask under all noise conditions

Address: 06h**--Control0**
Reset Value: 0x0010_0100
Type: (See Column Below)

Bit	Name	R/W/C	Description
7	Reserved	N/A	Do Not Use
6	TX_FLUSH	W/C	1: Self clearing bit to flush the content of the transmit FIFO
5	INT_MASK	R/W	1: Mask all interrupts 0: Interrupts to host are enabled
4	Reserved	N/A	Do Not Use
3:2	HOST_CUR[1 :0]	R/W	Controls the host pull-up current enabled by PU_EN[2:1] bits in the Switches0 register: 00: Current disabled 01: 80 uA - Default USB power 10: 180 uA - Medium Current Mode: 1.5A 11: 330 uA - High Current Mode: 3A
1	AUTO_PRE	R/W	1: Starts the transmitter automatically when a message with a goodCRC is received. This allows the software to take as much as300 µS to respond after the I_CRC_CHK interrupt is received. Before starting the transmitter, an internal timer waits for approximately 170 µS before executing the transmit start and preamble 0: Feature disabled
0	TX_START	W/C	1: Start transmitter using the data in the transmit FIFO. Preamble is started first. During the preamble period the transmit data can start to be written to the transmit FIFO. Self clearing

Address: 07h**—Control1**
Reset Value: 0x0000_0000
Type: (See Column Below)

Bit	Name	R/W/C	Description
7	Reserved	N/A	Do Not Use
6	ENSOP2DB	R/W	1: Enable SOP”_DEBUG (SOP double prime debug) packets 0: Ignore SOP”_DEBUG (SOP double prime debug) packets
5	ENSOP1DB	R/W	1: Enable SOP’_DEBUG (SOP prime debug) packets 0: Ignore SOP’_DEBUG (SOP prime debug) packets
4	BIST_MODE2	R/W	1: Sent BIST Mode 01s pattern for testing
3	Reserved	N/A	Do Not Use
2	RX_FLLUSH	R/C	1: Self clearing bit to flush the content of the receive FIFO.
1	ENSOP2	R/W	1: Enable SOP”(SOP double prime) packets 0: Ignore SOP”(SOP double prime) packets
0	ENSOP1	R/W	1: Enable SOP’(SOP prime) packets 0: Ignore SOP’(SOP prime) packets

Address: 08h—**Control2**
Reset Value: Ox0000_0010
Type: (See Column Below)

Bit	Name	R/W/C	Description
7:6	TOG_SAVE_PWR2 TOG_SAVE_PWR1	R/W	00: Don't go into the DISABLE state after one cycle of toggle 01: Wait between toggle cycles for t_{DIS} time of 40 ms 10: Wait between toggle cycles for t_{DIS} time of 80 ms 11: Wait between toggle cycles for t_{DIS} time of 160 ms
5	TOG_RD_ONLY	R/W	1: When TOGGLE=1 only Rd values will cause the TOGGLE state machine to stop toggling and trigger the I_TOGGLE interrupt 0: When TOGGLE=1, Rd and Ra values will cause the TOGGLE state machine to stop toggling
4	Reserved	N/A	Do Not Use
3	WAKE_EN	R/W	1: Enable Wake Detection functionality if the power state is correct 0: Disable Wake Detection functionality
2:1	MODE	R/W	11: Enable SRC polling functionality if TOGGLE=1 10: Enable SNK polling functionality if TOGGLE=1 01: Enable DRP polling functionality if TOGGLE=1 00: Do Not Use
0	TOGGLE	R/W	1: Enable DRP, SNK or SRC Toggle autonomous functionality 0: Disable DRP, SNK and SRC Toggle functionality

Address: 09h—**Control3**
Reset Value: Ox0000_0110
Type: (See Column Below)

Bit	Name	R/W/C	Description
7	Reserved	N/A	Do Not Use
6	SEND_HARD_RESET	W/C	1: Send a hard reset packet (highest priority) 0: Don't send a soft reset packet
5	Reserved	N/A	Do Not Use
4	AUTO_HARDRESET	R/W	1: Enable automatic hard reset packet if soft reset fail 0: Disable automatic hard reset packet if soft reset fail
3	AUTO_SOFTRESET	R/W	1: Enable automatic soft reset packet if retries fail 0: Disable automatic soft reset packet if retries fail
2:1	N_RETRIES[1:0]	R/W	11: Three retries of packet (four total packets sent) 10: Two retries of packet (three total packets sent) 01: One retry of packet (two total packets sent) 00: No retries (similar to disabling auto retry)
0	AUTO_RETRY	R/W	1: Enable automatic packet retries if GoodCRC is not received 0: Disable automatic packet retries if GoodCRC is not received

Address: 0Ah--**Mask0**

Reset Value: 0x0000_0000

Type: Read/Write

Bit	Name	Description
7	M_VBUSOK	1: Mask I_VBUSOK interrupt bit 0: Do not mask
6	M_ACTIVITY	1: Mask interrupt for a transition in CC bus activity 0: Do not mask
5	M_COMP _CHNG	1: Mask I_COMP_CHNG interrupt for change is the value of COMP, the measure comparator 0: Do not mask
4	M_CRC_CHK	1: Mask interrupt from CRC_CHK bit 0: Do not mask
3	M_ALERT	1: Mask the I_ALERT interrupt bit 0: Do not mask
2	M_WAKE	1: Mask I_WAKE interrupt bit 0: Do not mask
1	M_COLLISION	1: Mask the I_COLLISION interrupt bit 0: Do not mask
0	M_BC_LVL	1: Mask I_BC_LVL interrupt bit 0: Do not mask

Address: 0Bh--**Power**

Reset Value: 0x0000_0001

Type: Read/write

Bit	Name	Description
7:4	Reserved	Do Not Use
3:0	PWR[3:0]	Power enables: PWR[0]: Bandgap and wake circuit PWR[1]: Receiver powered and current references for Measure block PWR[2]: Measure block powered PWR[3]: Enable internal oscillator, for PD PHY It is expected that PWR=4'h1 is used for low power WAKE detection. PWR=4'h7 is used for all other detection

Address: 0Ch--**Reset**

Reset Value: 0x0000_0000

Type: Write/Clear

Bit	Name	R/W/C	Description
7:2	Reserved	N/A	Do Not Use
1	PD_RESET	W/C	1: Reset just the PD logic for both the PD transmitter and receiver
0	SW_RES	W/C	1: Reset the ET7301 including the I^2C registers to their default values

Address: 0Dh--**OCPreg**

Reset Value: 0x0000_1111

Type: Read/write

Bit	Name	Description
7:4	Reserved	Do Not Use
3	OCP_RANGE	1: OCP range between 100 mA-800 mA (max_range=800 mA) 0: OCP range between 10 mA-80 mA (max_range=80 mA)
2:0	OCP_CUR[2:0]	111: max_range (see bit definition above for OCP_RANGE) 110: 7*max_range/8 101: 6*max_range/8 100: 5*max_range/8 011: 4*max_range/8 010: 3*max_range/8 001: 2*max_range/8 000: 1*max_range/8

Address: 0Eh--**Maska**

Reset Value: 0x0000_0000

Type: Read/Write

Bit	Name	Description
7	M_OCP_TEMP	1: Mask the I_OCP_TEMP interrupt
6	M_TOGDONE	1: Mask the I_TOGDONE interrupt
5	M_SOFTFAIL	1: Mask the I_SOFTFAIL interrupt
4	M_RETRYFAIL	1: Mask the I_RETRYFAIL interrupt
3	M_HARDSENT	1: Mask the I_HARDSENT interrupt
2	M_TXSENT	1: Mask the I_TXSENT interrupt
1	M_SOFTRST	1: Mask the I_SOFTRST interrupt
0	M_HARDRST	1: Mask the I_HARDRST interrupt

Address: 0Fh--**Maskb**

Reset Value: 0x0000_0000

Type: Read/Write

Bit	Name	Description
7:1	Reserved	Do Not Use
0	M_GCRCSENT	1: Mask the I_GCRCSENT interrupt

Address: 3Ch—**Status0a**

Reset Value: 0x0000_0000

Type: Read

Bit	Name	Description
7:6	Reserved	Do Not Use
5	SOFTFAIL	1: All soft reset packets with retries have failed to get a GoodCRC acknowledge. This status is cleared when a START_TX, TXON or SEND_HARD_RESET is executed
4	RETRYFAIL	1: All packet retries have failed to get a GoodCRC acknowledge. This status is cleared when a START_TX,TXON or SEND_HARD_RESET is executed
3:2	POWER3 POWER2	Internal power state when logic internals needs to control the power state. POWER3 corresponds to PWR3 bit andPOWER2 corresponds to PWR2 bit. The power state is the higher of both PWR[3:0] and {POWER3, POWER2, PWR[1:0]} so that if one is 03 and the other is F then the internal power state is F
1	SOFTRST	1: One of the packets received was a soft reset packet
0	HARDRST	1: Hard Reset PD ordered set has been received

Address: 3Dh—**Status1a**

Reset Value: 0x0000_0000

Type: Read

Bit	Name	Description
7:6	Reserved	Do Not Use
5:3	TOGSS3 TOGSS2 TOGSS1	000: Toggle logic running (processor has previously written TOGGLE=1) 001: Toggle functionality has settled to SRC on CC1(STOP_SRC1 state) 010: Toggle functionality has settled to SRC on CC2(STOP_SRC2 state) 101: Toggle functionality has settled to SNK on CC1(STOP_SNK1 state) 110: Toggle functionality has settled to SNK on CC2(STOP_SNK2 state) 111: Toggle functionality has detected Audio Accessory with VRA on both CC1 and CC2 (settles to STOP_SRC1 state) Otherwise: Not defined (do not interpret)
2	RXSOP2DB	1: Indicates the last packet placed in the RxFIFO is type SOP”_DEBUG (SOP double prime debug)
1	RXSOP1DB	1: Indicates the last packet placed in the RxFIFO is type SOP’_DEBUG (SOP prime debug)
0	RXSOP	1: Indicates the last packet placed in the RxFIFO is type SOP

Address: 3Eh—**Interrupta**
Reset Value: 0x0000_0000
Type: Read/Clear

Bit	Name	Description
7	I_OCP_TEMP	1: Interrupt from either a OCP event on one of the VCONN switches or an over-temperature event
6	I_TOGDONE	1: Interrupt indicating the TOGGLE functionality was terminated because a device was detected
5	I_SOFTFAIL	1: Interrupt from automatic soft reset packets with retries have failed
4	I_RETRYFAIL	1: Interrupt from automatic packet retries have failed
3	I_HARDSENT	1: Interrupt from successfully sending a hard reset ordered set
2	I_TXSENT	1: Interrupt to alert that we sent a packet that was acknowledged with a GoodCRC response packet
1	I_SOFTRST	1: Received a soft reset packet
0	I_HARDRST	1: Received a hard reset ordered set

Address: 3Fh—**Interruptb**
Reset Value: 0x0000_0000
Type: Read/Write

Bit	Name	Description
7:1	Reserved	Do Not Use
0	I_GCRCSENT	1: Sent a GoodCRC acknowledge packet in response to an incoming packet that has the correct CRC value

Address: 40h--**Status0**
Reset Value: 0x0000_0000
Type: Read

Bit	Name	Description
7	VBUSOK	1: VBUS is higher than $V_{VBUSthr}$ threshold 0: VBUS is lower than $V_{VBUSthr}$ threshold
6	ACTIVITY	1: Transitions are detected on the active CC* line. This bit goes high after a minimum of 3 CC transitions, and remains high for $t_{ACTIVITY}$ after last transition on CC 0: inactive
5	COMP	1: Measured CC*input is higher than reference level driven from the MDAC 0: Measured CC*input is lower than reference level driven from the MDAC
4	CRC_CHK	1: Indicates the last received packet had the correct CRC. This bit remains set until the SOP of the next packet 0: Packet received for an enabled SOP* and CRC for the enabled packet received was incorrect
3	ALERT	1: Alert software an error condition has occurred. An alert is caused by: TX_FULL: the transmit FIFO is full

		RX_FULL: the receive FIFO is full
2	WAKE	1: Voltage on CCx indicated that either a device, host or dual-role port is attempting to attach
1:0	BC_LVL[1:0]	Current voltage status of the measured CC pin interpreted as host current levels as follows: 00: < 200 mV (VRA) 01: >200 mV, <660 mV (VRd-USB) 10: >660 mV, <1.23 V (VRd-1.5) 11 :>1.23 V (VRd-3.0*) Note the software must measure these at an appropriate time, while there is no signaling activity on the selected CC line. BC_LVL is only defined when Measure block is on which is when register bits PWR[2]=1 and either MEAS_CC1=1 orMEAS_CC2=1

Address: 41h--**Status1**

Reset Value: 0x0010_1000

Type: Read

Bit	Name	Description
7	RXSOP2	1: Indicates the last packet placed in the RxFIFO is type SOP”(SOP double prime)
6	RXSOP1	1: Indicates the last packet placed in the RxFIFO is type SOP’(SOP prime)
5	RX_EMPTY	1: The receive FIFO is empty
4	RX_FULL	1: The receive FIFO is full
3	TX_EMPTY	1: The transmit FIFO is empty
2	TX_FULL	1: The transmit FIFO is full
1	OVRTEMP	1: Temperature of the device is too high
0	OCP	1: Indicates an over-current or short condition has occurred on the VCONN switch

Address: 42h--**Interrupt**

Reset Value: 0x0000_0000

Type: Read/Clear

Bit	Name	Description
7	I_VBUSOK	1: Interrupt occurs when VBUS transitions through 4.5V. This bit typically is used to recognize port partner during startup
6	I_ACTIVITY	1: A change in the value of ACTIVITY of the CC bus has occurred
5	I_COMP	1: A change in the value of COMP has occurred. Indicates selected CC line has tripped a threshold programmed into the MDAC
4	I_CRC_CHK	1: The value of CRC_CHK newly valid. I.e. The validity of the incoming packet has been checked
3	I_ALERT	1: Alert software an error condition has occurred. An alert is caused by: TX_FULL: the transmit FIFO is full RX_FULL: the receive FIFO is full
2	I_WAKE	1: Voltage on CC indicated a device attempting to attach .Software must then

		Power up the clock and receiver blocks
1:0	I_CLOLLISION	1: When a transmit was attempted, activity was detected on the active CC line Transmit is not done. The packet is received normally
0	I_BC_LVL	1: A change in host requested current level has occurred

Address: 43h--**FIFOs**
Reset Value: 0x0000_0000
Type: Read or Write

Bit	Name	Description
7:0	TX/RX Token	Writing to this register writes a byte into the transmit FIFO. Reading from this register reads from the receive FIFO. Each byte is a coded token. Or a token followed by a fixed number of packed data byte

Typical Application

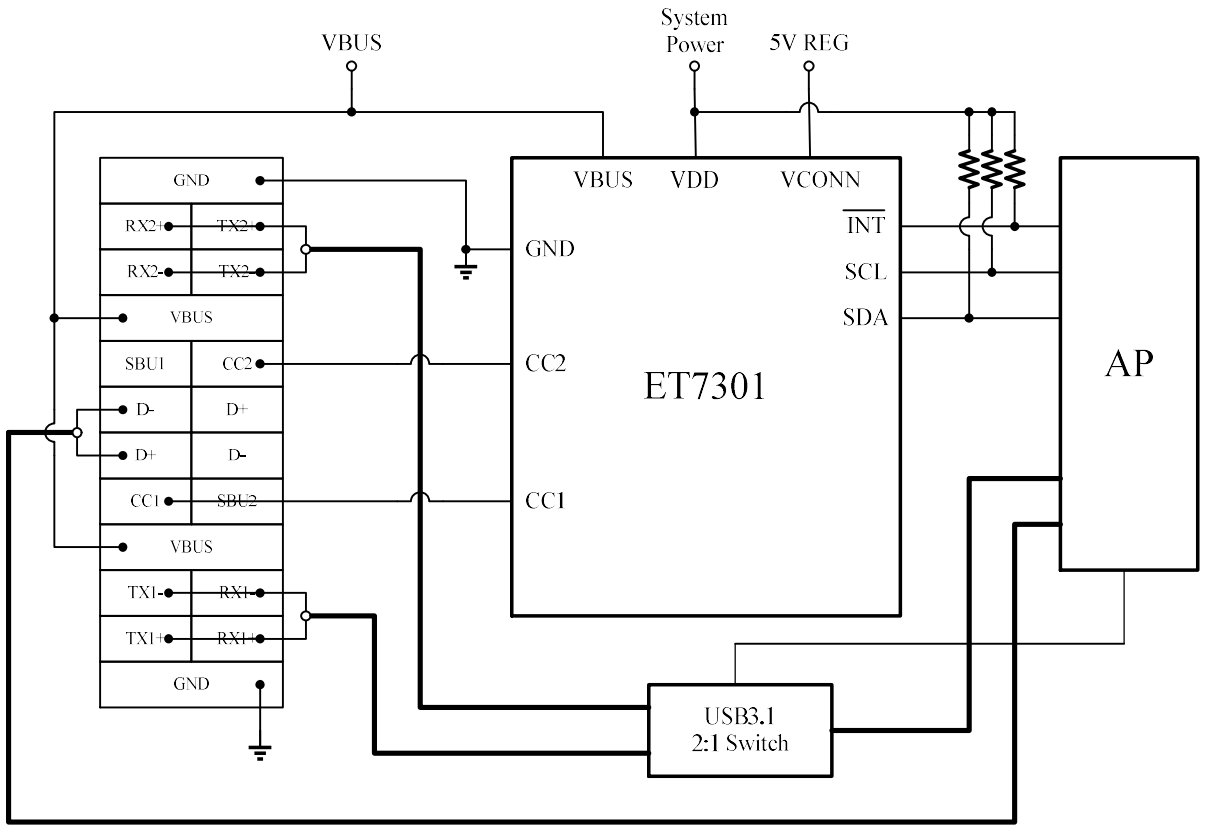
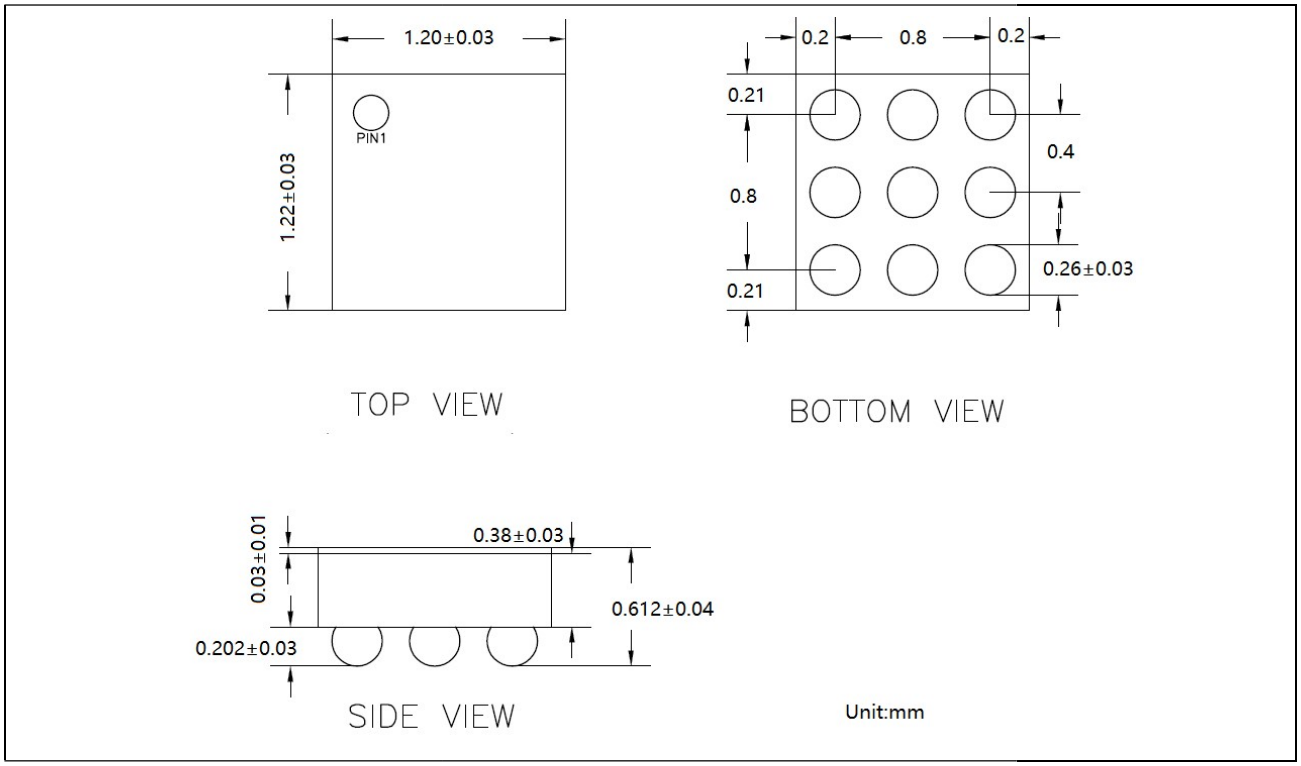


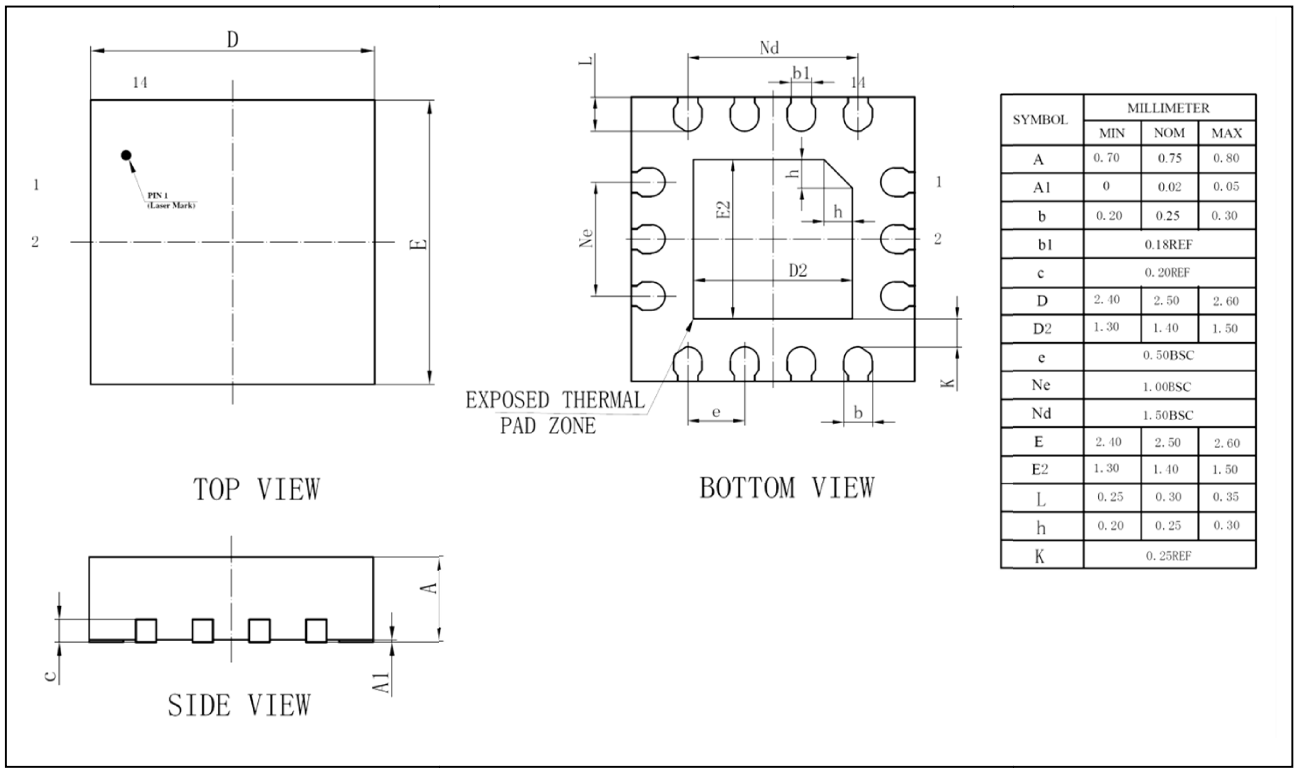
Figure 14

Package Dimension

WLCSP9（1.22mm*1.20mm）



QFN14(2.5*2.5)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.20REF		
D	2.40	2.50	2.60
D2	1.30	1.40	1.50
e	0.50BSC		
Ne	1.00BSC		
Nd	1.50BSC		
E	2.40	2.50	2.60
E2	1.30	1.40	1.50
L	0.25	0.30	0.35
h	0.20	0.25	0.30
K	0.25REF		

Revision History and Checking Table

No.	Version	Date	Revision Item	Request	Function and characteristic checking	Package dimension checking	Typos checking
1	1.0	2016-08-15	Original Version	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li	Zhu Jun Li
2	1.1	2017-06-09	Add QFN14 Package	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li	Zhu Jun Li