I²C Controlled 3 A Single-Cell Battery Charger With USB Charger Detection for High Input Voltage and Narrow Voltage DC (NVDC) Power Path Management

General Description

The ET95601CX device is a highly-integrated 3 A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I²C serial interface with charging and system settings makes the device a truly flexible solution.

Features

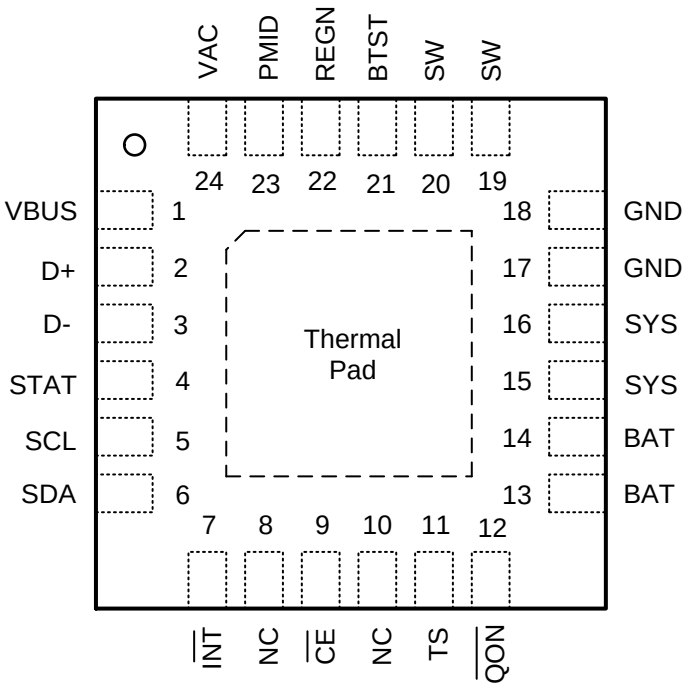
- High-Efficiency, 1.5 MHz, Synchronous Switch Mode Buck Charger
  - 92% Charge Efficiency at 2 A from 5 V Input
  - Optimized for USB Voltage Input (5 V)
  - Selectable Low Power Pulse Frequency Modulation (PFM) Mode for Light Load Operations
- Supports USB On-The-Go (OTG)
  - Boost Converter With Up to 1.2 A Output
  - 92% Boost Efficiency at 1 A Output
  - Accurate Constant Current (CC) Limit
  - Soft-Start Up To 500 µF Capacitive Load
  - Output Short Circuit Protection
  - Selectable Low Power PFM Mode for Light Load Operations
- Single Input to Support USB Input and High Voltage Adapters
  - Support 3.9 V to 13.5 V Input Voltage Range With 22 V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100 mA to 3.2 A With 100 mA Resolution) to Support USB 2.0, USB 3.0 Standards and High Voltage Adapters (IINDPM)
  - VINDPM Threshold Automatically Tracks Battery Voltage
  - Auto Detect USB SDP, DCP and Non-Standard Adapters
- High Battery Discharge Efficiency With 19.5 mΩ Battery Discharge MOSFET
- Narrow VDC (NVDC) Power Path Management
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake Up

- Flexible Autonomous and I²C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 22 μA Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% at 1.5 A Charge Current Regulation
  - ±10% at 0.9 A Input Current Regulation
- Package: QFN24(4 mm × 4 mm x 0.75 mm)

Applications

- Smart Phones
- Portable Internet Devices and Accessory

Pin Configuration



Top View

Pin Functions

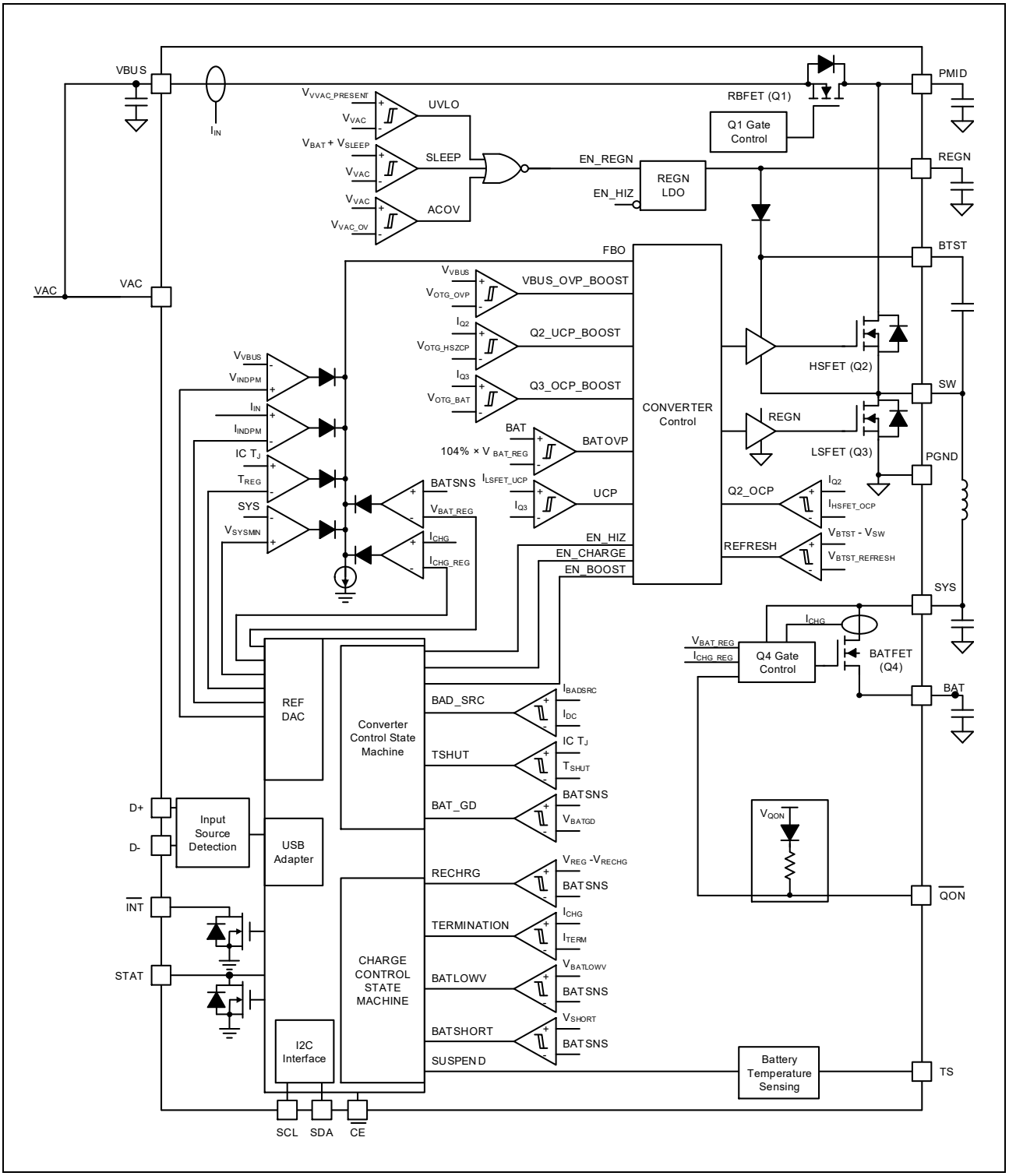
Pin		TYPE[1]	DESCRIPTION
NAME	NO.		
BAT	13	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10 µF close to the BAT pin.
	14		
BTST	21	P	PWM high side driver positive supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect the 0.047 µF bootstrap capacitor from SW to BTST.
$\overline{CE}$	9	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
GND	17	—	Ground pins.
	18		
$\overline{INT}$	7	DO	Open-drain interrupt Output. Connect the INT to a logic rail through 10 kΩ resistor. The INT pin sends an active low, 256 µs pulse to host to report charger device status and fault.
NC	8	—	No Connect. Keep the pins float.
	10		
D-	3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adapters.
PMID	23	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
D+	2	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adapters
QON	12	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ duration turns on BATFET to exit shipping mode. When VBUS is not plugge D- in, a logic low of t_{QON_RST} (minimum 14 s) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (minimum 524 ms) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic.
REGN	22	P	LSFET driver and internal supply output. Internally, REGN is connected to the anode of the boost-strap diode.Connect a 4.7 µF (10 V rating) ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
SCL	5	DI	I^2C interface clock. Connect SCL to the logic rail through a 10 kΩ resistor.
SDA	6	DIO	I^2C interface data. Connect SDA to the logic rail through a 10 kΩ resistor.

Pin Functions (Continued)

Pin		TYPE[1]	DESCRIPTION
NAME	NO.		
STAT	4	DO	Open-drain charge status output. Connect the STAT pin to a logic rail via 10 kΩ resistor. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): 1 Hz, 50% duty cycle Pulses This pin can be disabled via STAT_DIS register bit.
SW	19	P	Switching node output. Connected to output inductor. Connect the 0.047 μF bootstrap capacitor from SW to BTST.
	20		
SYS	15	P	Converter output connection point. The internal current sensing network is connected between SYS and BAT. Connect a 20 μF capacitor close to the SYS pin.
	16		
TS	11	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. When TS pin is not used, connect a 10 kΩ resistor from REGN to TS and connect a 10 kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
VAC	24	AI	Charge input voltage sense. This pin must be connected to VBUS pin.
VBUS	1	P	Charger input. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS to GND close to device.
Thermal Pad	—	P	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

Note1: AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

Block Diagram



Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(2)]

Symbol	Parameter	Min	Max	Unit
Voltage Range (with respect to GND)	VAC, VBUS (converter not switching)[(3)]	-0.3	22	V
Voltage Range (with respect to GND)	BTST, PMID (converter not switching)[(3)]	-0.3	22	V
Voltage Range (with respect to GND)	SW	-2	16	V
Voltage Range (with respect to GND)	BTST to SW	-0.3	7	V
Voltage Range (with respect to GND)	D+, D-	-0.3	7	V
Voltage Range (with respect to GND)	REGN, TS, $\overline{CE}$, BAT, SYS (converter not switching)	-0.3	7	V
Output Sink Current	STAT		6	mA
Voltage Range (with respect to GND)	SDA, SCL, INT, QON, STAT	-0.3	7	V
Voltage Range (with respect to GND)	PGND to GND (QFN package only)	-0.3	0.3	V
Output Sink Current	INT		6	mA
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

Note2: Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

Note3: VBUS is specified up to 22 V for a maximum of one hour at room temperature.

ESD Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[4]	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[5]	± 250	

Note4: JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

Note5: JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{BUS}	Input voltage	3.9		13.5[6]	V
I_{in}	Input current (VBUS)			3.25	A
I_{SWOP}	Output current (SW)			3.25	A
V_{BATOP}	Battery voltage			4.624	V
I_{BATOP}	Fast charging current			3.0	A
I_{BATOP}	Discharging current (continuous)			6	A
T_A	Operating ambient temperature	-40		85	°C

Note6: The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

Thermal information

Symbol	Thermal Metric	ET95601CX RTW (QFN) 24 Pins	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	36	°C/W
$R_{\theta JC(top)}$	Junction to case (top) thermal resistance	23	°C/W

Electrical Characteristics

V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, T_J = -40 °C to 125 °C and T_J = 25 °C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.5 V, V_{BUS} < $V_{AC\text{-}UVLOZ}$, leakage between BAT and VBUS, T_J < 85 °C			5	µA
I_{BAT}	Battery discharge current (BAT) in buck mode	V_{BAT} = 4.5 V, HIZ Mode or No VBUS, I²C disabled, BATFET Disabled. T_J < 85 °C		22	44	µA
I_{BAT}	Battery discharge current (BAT, SW, SYS)	V_{BAT} = 4.5 V, HIZ Mode or No VBUS, I²C Disabled, BATFET Enabled. T_J < 85 °C		35	70	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, High-Z Mode, No battery		37	74	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, High-Z Mode, No battery		43	86	µA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, V_{VBUS} > V_{VBAT}, converter not switching		1.5	3	mA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{VBAT}, converter switching, V_{BAT} = 3.8 V, I_{SYS} = 0 A		3		mA
I_{BOOST}	Battery Discharge Current in boost mode	V_{BAT} = 4.2 V, boost mode, I_{VBUS} =0 A, converter switching		3		mA
VBUS, VAC AND BAT PIN POWER-UP						
V_{BUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13.5	V
V_{VAC_UVLOZ}	V_{BUS} for active I²C, no battery Sense VAC pin voltage	V_{VAC} rising	3.7			V
$V_{VAC\_UVLOZ\_HYS}$	I²C active hysteresis	VAC falling from above V_{VAC_UVLOZ}		300		mV
V_{SLEEP}	Sleep mode falling threshold	(V_{VAC} - V_{VBAT}), V_{BUSMIN_FALL} ≤ V_{BAT} ≤ V_{REG}, VAC falling	10	65	200	mV
V_{SLEEPZ}	Sleep mode rising threshold	(V_{VAC}–V_{VBAT}), V_{BUSMIN_FALL} ≤ V_{BAT} ≤ V_{REG}, V_{AC} rising		250		mV

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{VAC\_OV\_RISE}$	VAC 6.5 V Overvoltage rising threshold	VAC rising; OVP (REG06[7:6]) = '01'	6.1	6.4	6.7	V
$V_{VAC\_OV\_RISE}$	VAC 10.5 V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) ='10'	10.3	10.9	11.5	V
$V_{VAC\_OV\_RISE}$	VAC 14 V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) ='11'	13.5	14.2	14.9	V
$V_{VAC\_OV\_HYS}$	VAC 6.5 V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) ='01'		250		mV
$V_{VAC\_OV\_HYS}$	VAC 10.5 V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) ='10'		150		mV
$V_{VAC\_OV\_HYS}$	VAC 14 V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) ='11'		100		mV
V_{BAT_UVLOZ}	BAT for active I^2C, no adapter	V_{BAT} rising		2.4		V
$V_{BAT\_DPL\_FALL}$	Battery Depletion Threshold	V_{BAT} falling	2.2	2.4	2.6	V
$V_{BAT\_DPL\_RISE}$	Battery Depletion Threshold	V_{BAT} rising	2.4	2.6	2.8	V
V_{BUSMIN_FALL}	Bad adapter detection falling threshold	V_{BUS} falling		3.8		V
I_{BADSRC}	Bad adapter detection current source	Sink current from VBUS to GND		30		mA
POWER-PATH						
V_{SYS_MIN}	System regulation voltage	V_{VBAT} < SYS_MIN[2:0] = 101, BATFET Disabled (REG07[5] = 1)	3.5	3.65		V
V_{SYS}	System Regulation Voltage	I_{SYS} = 0 A, V_{VBAT} > V_{SYSMIN}, V_{VBAT} = 4.400 V, BATFET disabled (REG07[5] = 1)		V_{BAT} + 75mV		V
V_{SYS_MAX}	Maximum DC system voltage output	I_{SYS} = 0 A, Q4 off, V_{VBAT}=4.400 V,		4.475		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40 °C≤ T_A ≤ 125 °C		45		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and SW - Q2	V_{REGN} = 5 V , -40 °C ≤ T_A ≤ 125 °C		50		mΩ

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and GND - Q3	V_{REGN} = 5 V , -40 °C ≤ T_A ≤ 125 °C		80		mΩ
V_{FWD}	BATFET forward voltage in Supplement mode			40		mV
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2 V, T_J = 25 °C		19		mΩ
BATTERY CHARGER						
V_{BATREG_RANGE}	Charge voltage program range		3.856		4.624	V
V_{BATREG_STEP}	Charge voltage step			16		mV
V_{BATREG_ACC}	Charge voltage setting accuracy	V_{BAT} = 4.208 V or V_{BAT} = 4.352 V, –40 ≤ TJ ≤ 85°C	-0.5		0.5	%
$I_{CHG\_REG\_RANGE}$	Charge current regulation range		0		2875	mA
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 540 mA, VBUS=5 V, V_{VBAT} = 3.8 V	486		594	mA
I_{CHG_REG}	Charge current regulation accuracy	I_{CHG} = 1.955 A, VBUS=5V, V_{VBAT} = 3.8 V	1.857		2.052	mA
$V_{BATLOWV\_FALL}$	Battery LOWV falling threshold	I_{CHG} = 240 mA	2.6	2.8	2.9	V
$V_{BATLOWV\_RISE}$	Battery LOWV rising threshold	Pre-charge to fast charge	2.8	3.0	3.1	V
I_{PRECHG}	Precharge current regulation	I_{PRECHG} [3:0] = '0011' = 208 mA	166	208	250	mA
I_{TERM_ACC}	Termination current regulation accuracy	I_{CHG} > 780 mA, I_{TERM} [3:0] = '0010' = 180 mA, V_{VBAT} = 4.208 V	-25		25	%
V_{SHORT}	Battery short voltage	V_{VBAT} falling	1.9	2	2.1	V
V_{SHORTZ}	Battery short voltage	V_{VBAT} rising	2.1	2.2	2.3	V
I_{SHORT}	Battery short current	V_{VBAT} < V_{SHORTZ}	80	100	120	mA
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 0		100		mV
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 1		200		mV

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{SYSLOAD}$	System discharge load current	V_{SYS} = 4.2 V		30		mA
INPUT VOLTAGE AND CURRENT REGULATION						
V_{INDPM_ACC}	Input voltage regulation accuracy		-3		3	%
$V_{DPM\_VBAT\_ACC}$	Input voltage regulation accuracy tracking V_{BAT}		-3		3	%
I_{INDPM}	USB input current regulation limit	V_{VBUS} =5 V, current pulled from SW, I_{INDPM} (REG[4:0]=00100)= 500 mA, -40 ≤ T_J ≤ 85 °C	440		500	mA
		V_{VBUS} =5 V, current pulled from SW, I_{INDPM}(REG[4:0]=01000)= 900 mA, -40 ≤ T_J ≤ 85 °C	688		932	mA
		V_{VBUS}=5 V, current pulled from SW, I_{INDPM} (REG[4:0]=01110)= 1.5 A, -40 ≤ T_J ≤ 85 °C	1.3		1.5	A
I_{IN_START}	Input current limit during system start-up sequence			200		mA
BAT PIN OVERVOLTAGE PROTECTION						
V_{BATOVP_RISE}	Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104		%
V_{BATOVP_FALL}	Battery overvoltage threshold	V_{BAT} falling, as percentage of V_{BAT_REG}		102		%
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1]=1)=120 °C		120		°C
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1]=0)=100 °C		100		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		160		°C
T_{SHUT_HYST}	Thermal Shutdown Hysteresis			30		°C

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
JEITA Thermistor Comparator (BUCK MODE)						
VT1	T1 (0 °C) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to V_{REGN}		72.5%		
VT1	Falling	As Percentage to V_{REGN}		71.7%		
VT2	T2 (10 °C) threshold, Charge back to I_{CHG}/5 below this temperature	As percentage of V_{REGN}		67.3%		
VT2	Falling	As Percentage to V_{REGN}		66.6%		
VT3	T3 (45 °C) threshold, charge back to I_{CHG} and V_{REG}-0.2V above this temperature.	Charger suspends charge. As Percentage to V_{REGN}		44.4%		
VT3	Falling	As Percentage to V_{REGN}		43.9%		
VT5	T5 (60 °C) threshold, charge suspended above this temperature.	As Percentage to V_{REGN}		34.1%		
VT5	Falling	As Percentage to V_{REGN}		34.7%		
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)						
V_{BCOLD}	Cold Temperature Threshold, Voltage Rising Threshold	As Percentage to V_{REGN} (Approx. -20 °C w/ 103AT), T_J = -20 °C - 125 °C		79.3%		
V_{BCOLD}	Falling	T_J = -20 °C - 125 °C		78.5%		
V_{BHOT}	Hot Temperature Threshold, Voltage falling Threshold	As Percentage to V_{REGN} (Approx. 65 °C w/ 103AT), T_J = -20 °C - 125 °C		31.2%		
V_{BHOT}	Rising	T_J = -20 °C - 125 °C		31.8%		
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{BATFET_OCP}[(7)]	System over load threshold			7.0		A

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BOOST MODE OPERATION						
$V_{OTG\_REG\_ACC}$	Boost mode regulation voltage accuracy	V_{VBAT} = 3.8 V, $I_{(PMID)}$ = 0 A, BOOSTV[1:0] = '10' = 5.126 V	-3		3	%
$V_{BATLOWV\_OTG}$	Battery voltage exiting boost mode	V_{VBAT} falling, MIN_VBAT_SEL (REG01[0]) = 0	2.7	2.8	2.9	V
		V_{VBAT} rising, MIN_VBAT_SEL (REG01[0]) = 0	2.9	3.0	3.1	V
		V_{VBAT} falling, MIN_VBAT_SEL (REG01[0]) = 1	2.4	2.5	2.6	V
		V_{VBAT} rising, MIN_VBAT_SEL (REG01[0]) = 1	2.7	2.8	2.9	V
I_{OTG_OCP}	Boost mode RBFET over-current protection	BOOST_LIM =1.2A, (REG02[7] = 1)		1.2		A
I_{OTG_OCP}	Boost mode RBFET over-current protection	BOOST_LIM = 0.5 A (REG02[7] = 0)		0.5		A
V_{OTG_OVP}	OTG overvoltage threshold	Rising threshold		6.0		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 9 V, I_{REGN} = 40 mA		5.0		V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5 V, I_{REGN} = 20 mA		4.7		V
LOGIC I/O PIN CHARACTERISTICS (CE, INT, STAT)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
I_{BIAS}	High-level leakage current	Pull up rail 1.8 V			1	μA
V_{OL}	Low-level output voltage				0.4	V
I²C Interface (SCL, SDA)						
V_{IH}	Input high threshold level	Pull up rail 1.8 V	1.3			V
V_{IL}	Input t low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current 5 mA			0.4	V

Note7:Specified by design. Not production tested.

Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBUS/BAT POWER UP						
t_{BADSRC}	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination			24		ms
$t_{SYSOVLD\_DGL}$	System over-current deglitch time to turn off Q4			256		μs
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		μs
t_{SAFETY}	Typical Charge Safety Timer Range	CHG_TIMER = 1		10		hr
QON TIMING						
$t_{SHIPMODE}$	$\overline{QON}$ low time to turn on BATFET and exit ship mode	-10°C ≤ T_J ≤ 60°C		2.1		s
$t_{QON\_RST\_2}$	$\overline{QON}$ low time to reset BATFET	-10°C ≤ T_J ≤ 60°C		14.7		s
t_{BATFET_RST}	BATFET off time during full system reset	-10°C ≤ T_J ≤ 60°C		524		ms
t_{SM_DLY}	Enter ship mode delay	-10°C ≤ T_J ≤ 60°C		12.6		s
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[4]=1	REGN LDO disabled		40		s
f_{SCL}	SCL clock frequency				400	kHz

Detailed Description

Overview

The ET95601CX device is a highly integrated 3.0 A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

Feature Description

Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (Supplement Mode). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET\_OCP}$), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in BATFET Enable (Exit Shipping Mode) is applied to re-enable BATFET.

Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. Input Source Type Detection is based on D+/ D- lines to set default input current limit (IINDPM) register or input source type.
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- V_{VAC} above $V_{VAC\_PRESENT}$
- V_{VAC} above V_{BAT} + V_{SLEEPZ} in buck mode or VBUS below V_{BAT} + V_{SLEEP} in boost mode
- After 220 ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VBUS voltage below V_{VAC_OV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the $\overline{INT}$ pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the device runs input source detection through D+/D- lines. The ET95601CX follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/ DCP) and non-standard adapter through USB D+/D- lines.

After input source type detection is completed, an INT pulse is asserted to the host. in addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. PG_STAT bit is set
3. VBUS_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

D+/D- Detection Sets Input Current Limit in ET95601CX

The ET95601CX contains a D+/D- based input source detection to set the input current limit at VBUS plug-in. The D+/D- detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detection. The USB BC1.2 is capable to identify Standard Downstream Port (SDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the non-standard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D- pins. If an adapter is detected as DCP, the input current limit is set at 2.4 A. If an adapter is detected as unknown, the input current limit is set at 0.5 A.

When DCP is detected, the device start adjustable high voltage adapter handshake including QC2.0, etc. The handshake connects combinations of voltage source(s) and/or current sink on D+/D- to signal input source to raise output voltage from 5V to 9V(HVDCP_EN=1, EN_12V=0) / 12V(HVDCP_EN=1, EN_12V=1). The

adjustable high voltage adapter handshake can be disabled by clearing HVDCP_EN and EN_12V bits .

Table1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D + THRESHOLD	D - THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D-} within V_{1P2_VTH}	2
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P7_VTH}	1
Divider 4	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P7_VTH}	2.4

Table2. Input Current Limit Setting from D+/D- Detection

D+/ D- DETECTION	INPUT CURRENT LIMIT (IINLIM)
USB SDP (USB500)	500 mA
USB DCP	2.4 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Divider 2	2 A
Unknown 5 V Adapter	500mA

Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V - 5.4 V) for USB.

The device supports dynamic VINDPM settings which tracks the battery voltage. the actual input voltage limit will be VBAT + VDPM_BAT_TRACK offset.

Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value set by IINDPM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled.

Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overload the input source. The algorithm automatically identify maximum input current limit of power source without entering VINDPM to avoid input source overload.

This feature is disabled by default (ICO_EN=0) and can be enabled by setting ICO_EN bit to 1. After DCP

input source is detected based on the procedures previously described (Input Source Type Detection). The algorithm runs automatically when ICO_EN bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected.

The actual input current limit used by the Dynamic Power Management is reported in IDPM_LIM register while Input Current Optimizer is enabled (ICO_EN = 1) or set by IINDPM register when the algorithm is disabled (ICO_EN = 0).

Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA output requirement. The maximum output current is up to 1.2 A. The boost operation can be enabled if the conditions are valid:

1. BAT above V_{OTG_BAT}
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG_CONFIG bit = 1)
4. Voltage at TS (thermistor) pin is within acceptable range (V_{BHOT} < V_{TS} < V_{BCOLD})
5. After 30 ms delay from boost mode enable

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is 5.126 V and the output current can reach up to 1.2 A, selected through I^2C (BOOST_LIM bit). The boost output is maintained when BAT is above V_{OTG_BAT} threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot.

Host Mode and Standalone Power Management

Host Mode and Default Mode in ET95601CX

The ET95601CX is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 10 hours fast charging safety timer. At the end of the 10 hours, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a 1 to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, BATFET_DLY, and BATFET_DIS bits.

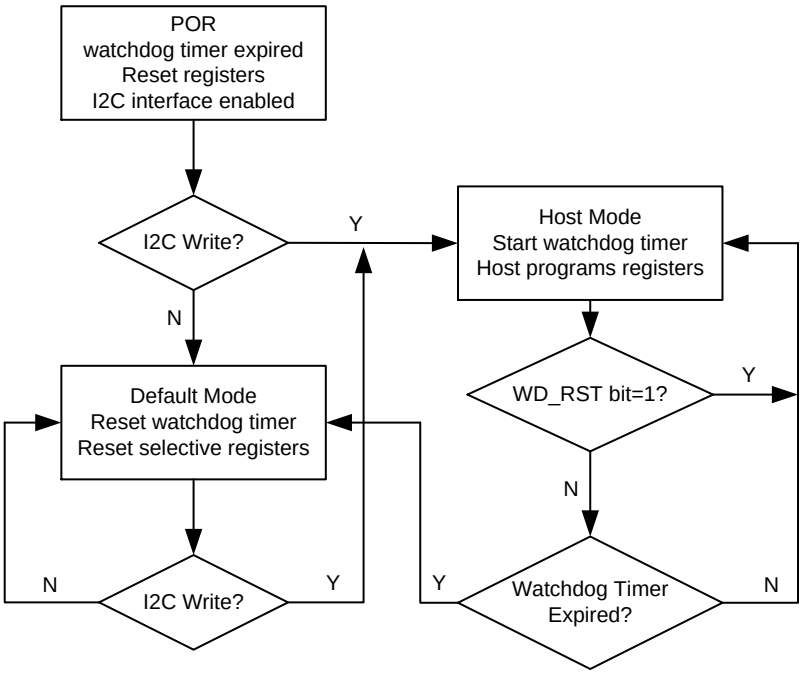


Figure1. Watchdog Timer Flow Chart

Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0 A charge current for high capacity tablet battery. The 19.5 mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table3. Charging Parameter Default Setting

DEFAULT MODE	ET95601CX
Charging voltage	4.208 V
Charging current	1.955 A
Pre-charge current	156 mA
Termination current	180 mA
Temperature profile	JEITA
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG_CONFIG bit = 1 and I_{CHG} register is not 0 mA and $\overline{CE}$ is low)
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit =1. in addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

Table4. Charging Current Setting

V_{BAT}	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< 2.2 V	I_{SHORT}	100 mA	01
2.2 V to 3 V	I_{PRECHG}	156 mA	01
> 3 V	I_{CHG}	1.955 A	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

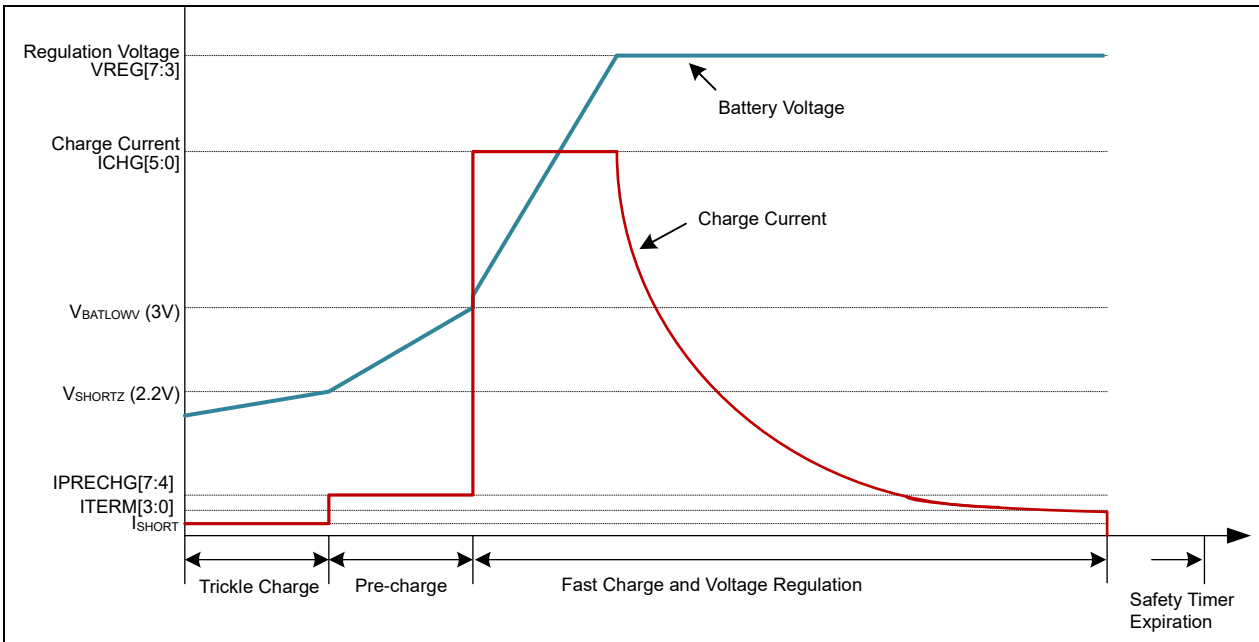


Figure2. Battery Charging Profile

Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

Resistance Compensation (IRCOMP)

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to delivery maximum power to battery.

The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register (VCLAMP) and the minimum resistance compensation (BATCOMP).

$$V_{REG\_ACTUAL} = V_{REG} + \min(I_{CHRG\_ACTUAL} \times BATCOMP, V_{CLAMP})$$

Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1 - T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1 - T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3 - T5), JEITA recommends charge voltage less than 4.1 V.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3 - T5) can be V_{REG} or V_{REG}-0.2V (configured by JEITA_VSET). The current setting at cool temperature (T1 - T2) can be further reduced to 20% of fast charge current (JEITA_ISET).

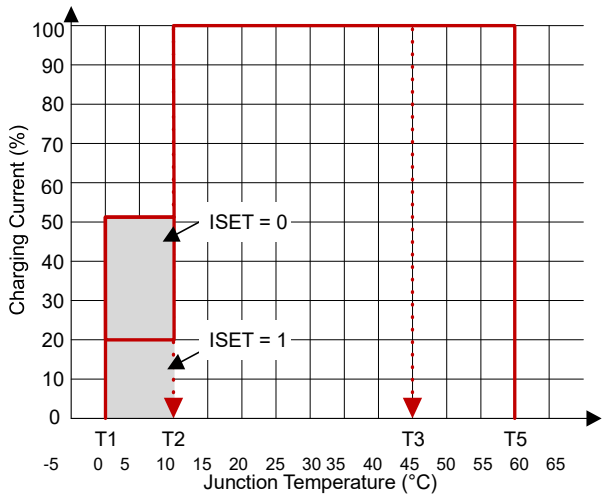


Figure3. JEITA Profile: Charging Current

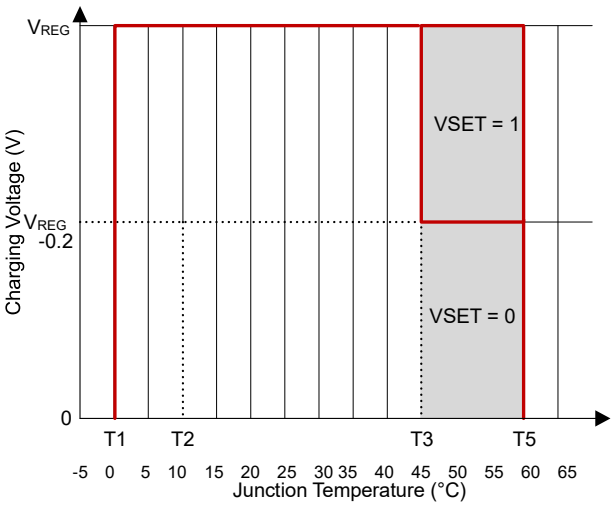


Figure4. JEITA Profile: Charging Voltage

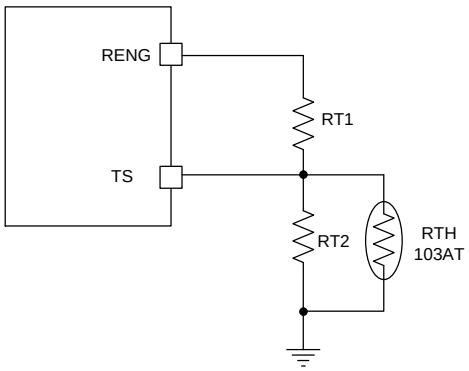


Figure5. TS Resistor Network

Equation 1 through Equation 2 describe updates to the resistor bias network.

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{V_{REGN}}{VT1} - 1}{\frac{1}{RT1} + \frac{1}{RTH_{COLD}}} \quad (2)$$

Select 0 °C to 60 °C range for Li-ion or Li-polymer battery:

- RTH_{COLD} = 27.28 kΩ
- RTH_{HOT} = 3.02 kΩ
- RT1 = 5.275 kΩ
- RT2 = 28.365 kΩ

Boost Mode Thermistor Monitor during Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. In additional, VBUS_STAT bits are set to 000 and NTC_FAULT is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC_FAULT is cleared.

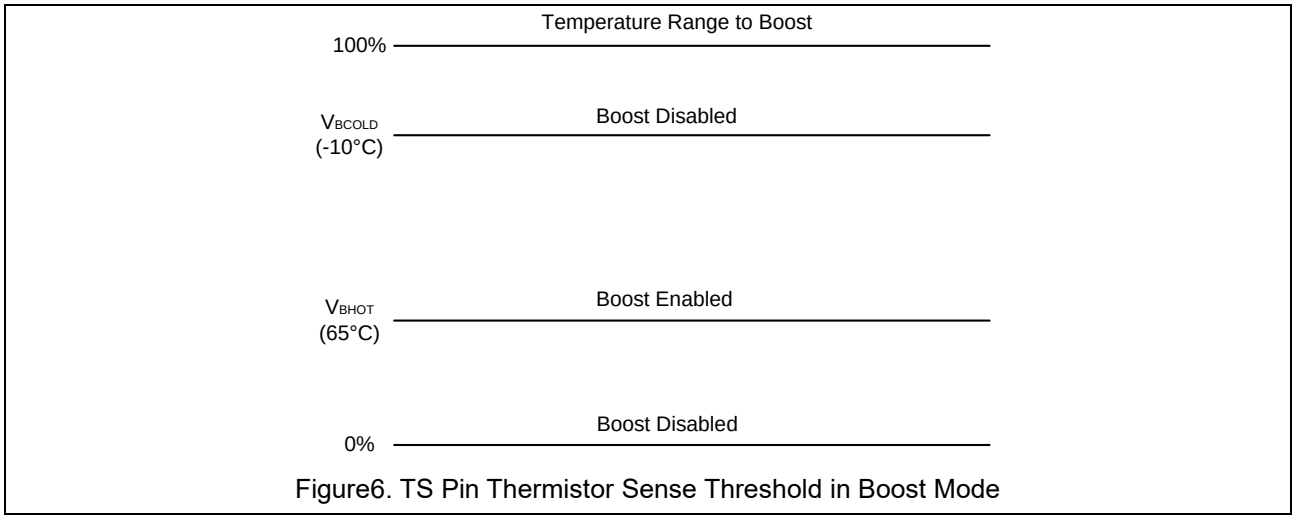


Figure6. TS Pin Thermistor Sense Threshold in Boost Mode

Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below VBATLOWV threshold and 10 hours when the battery is higher than $V_{BATLOWV}$ threshold.

The user can program fast charge safety timer through I²C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can

be disabled through I²C by setting EN_TIMER bit.

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT=1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

During the fault, timer is suspended. Once the fault goes away, fault resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHRG_CONFIG bit).

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_Min bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 150 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50 mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

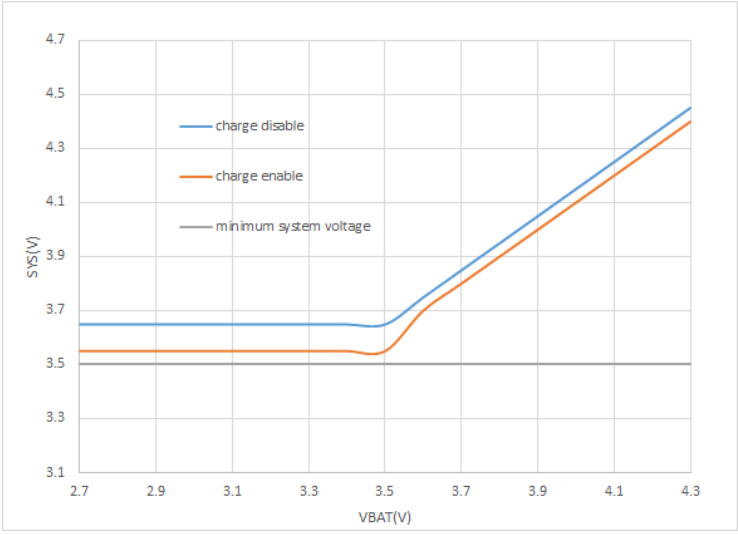


Figure7. System Voltage vs Battery Voltage

Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) or IDPM_STAT (IINDPM) goes high. Figure8 shows the DPM response with 9 V/1.2 A adapter, 3.2 V battery, 2.8 A charge current and 3.5 V minimum system voltage setting.

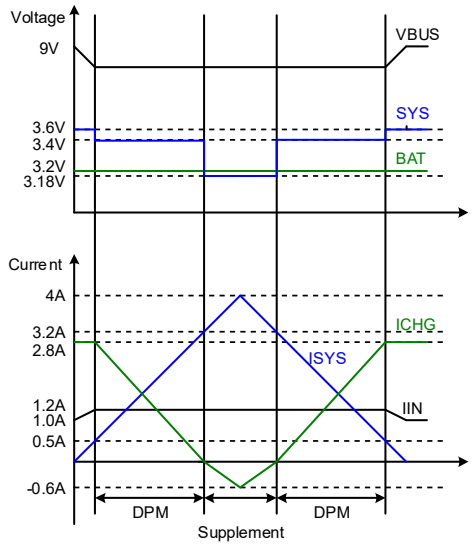


Figure8. DPM Response

Supplement Mode

When the system voltage falls 150 mV (VBAT >VSYSMin) or 75 mV (VBAT<VSYSMin) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 40 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce RDSON until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. Figure9 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

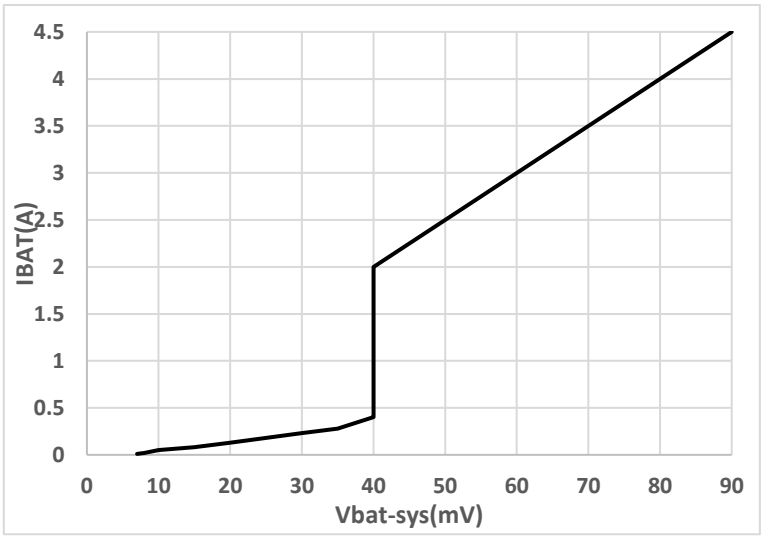


Figure9. BAFET V-I Curve

Shipping Mode and $\overline{QON}$ Pin

BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)
4. A logic high to low transition on $\overline{QON}$ pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The $\overline{QON}$ pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the $\overline{QON}$ pin is driven to logic low for t_{QON_RST} while input source is not plugged in and BATFET is enabled (BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

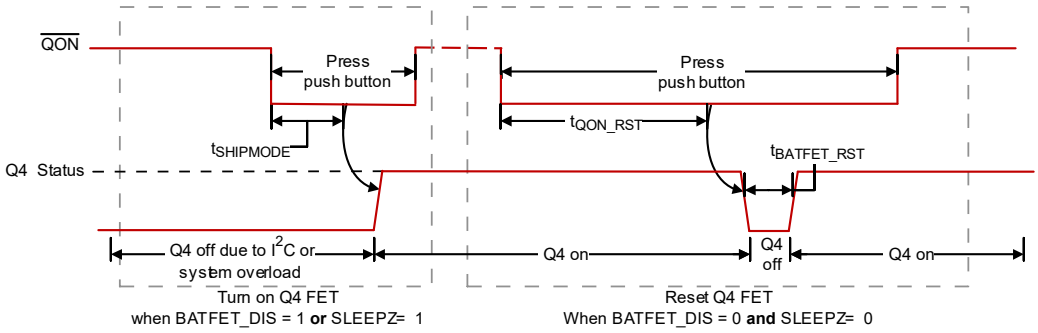
$\overline{\text{QON}}$ Pin Operations

The $\overline{\text{QON}}$ pin incorporates two functions to control BATFET.

1. BATFET Enable: A $\overline{\text{QON}}$ logic transition from high to low with longer than $t_{SHIPMODE}$ deglitch turns on BATFET and exit shipping mode.

2. BATFET Reset: When $\overline{\text{QON}}$ is driven to logic low by at least t_{QON_RST} while adapter is not plugged in (and BATFET_DIS=0), the BATFET is turned off for t_{BATFET_RST}. The BATFET is re-enabled after t_{BATFET_RST} duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting BATFET_RST_EN bit to 0.

Figure10 shows the sample external configurations for each.



Fogure10. $\overline{\text{QON}}$ Timing

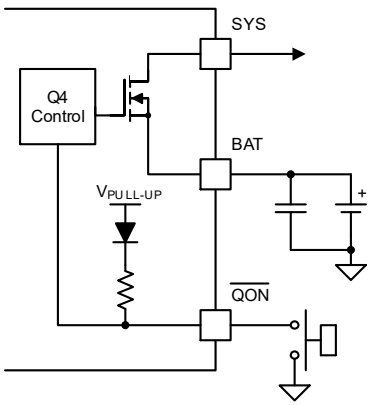


Figure11. $\overline{\text{QON}}$ Circuit

Status Outputs (STAT, $\overline{INT}$)

Power Good indicator (PG_STAT Bit)

The PG_STAT bit goes HIGH to indicate a good input source when:

- VBUS above V_{VBUS_UVLO}
- VBUS above battery (not in sleep)
- VBUS below V_{VAC_OV} threshold
- VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed input Source Type Detection

Charging Status indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the STAT_DIS bit = 1.

Table5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage) Boost Mode suspend (due to TS fault)	Blinking at 1 Hz

Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256 μs INT pulse.

- USB/adapter source identified (through DPDM detection)
- Good input source detected
  - – VBUS above battery (not in sleep)
  - – VBUS below V_{VAC_OV} threshold
  - – VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Input removed
- Charge Complete
- Any FAULT event in REG09
- VINDPM / IINDPM event detected (maskable)

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

Protections

Voltage and Current Monitoring in Converter Operation

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck and boost mode operation.

Voltage and Current Monitoring in Buck Mode

(1) Input Overvoltage (ACOV)

If VBUS voltage exceeds V_{VAC_OV} (programmable via OVP[1:0] bits), the device stops switching immediately. During input overvoltage event (ACOV), the fault register CHRG_FAULT bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

(2) System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above minimum system regulation voltage when the system is regulate at VSYSMIN. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30 mA discharge current to bring down the system voltage.

Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

(1) VBUS Soft Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

(2) VBUS Output Protection

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The boost build in accurate constant current regulation to allow OTG to adaptive to various types of load.If short circuit is detected on VBUS, the device operates in hiccup mode for protection. When short circuit condition continues to exist, the device repeats the hiccup cycle until short circuit condition is removed.In addition, when short circuit condition is detected the BOOST_FAULT bit is set and INT pulse is generated. The BOOST_FAULT bit can be cleared when BOOST_FAULT bit is read by I^2C interface.

(3) Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds VOTG_OVP, the device enters overvoltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. At Boost overvoltage duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

Thermal Regulation and Thermal Shutdown

(1) Thermal Protection in Buck Mode

The ET95601CX monitors the internal junction temperature TJ to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (120 °C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}(160 ºC). The fault register CHRG_FAULT is set to 1 and an $\overline{INT}$ is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is T_{SHUT_HYS} (30 ºC) below T_{SHUT}(160 ºC).

(2) Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT} (160 ºC), the boost mode is disabled by setting OTG_CONFIG bit low and BATFET is turned off. When IC junction temperature is below T_{SHUT}(160 ºC) -T_{SHUT_HYS} (30 ºC), the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG_CONFIG bit to recover.

Battery Protection

Battery overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

When BAT_LOADEN=1, when the battery is overvoltage, the device will pull current $I_{BATLOAD}$ (~30mA) from the VBAT pin to the ground to discharge the battery to prevent the battery voltage from further rising. There is no such behavior when BAT_LOADEN=0.

Battery Over-Discharge Protection

When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with I_{SHORT} (typically 100 mA) current when the V_{BAT} < V_{SHORT}, or precharge current as set in IPRECHG register when the battery voltage is between V_{SHORTZ} and V_{BAT_LOWV}.

System Over-Current Protection

When the system is shorted or significantly overloaded (I_{BAT} > I_{BATOP}) and the current exceeds BATFET overcurrent limit, the BATFET latches off. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

Programming

Serial Interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C™ is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG11. Register read beyond REG11 (0x11) returns 0xFF. The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

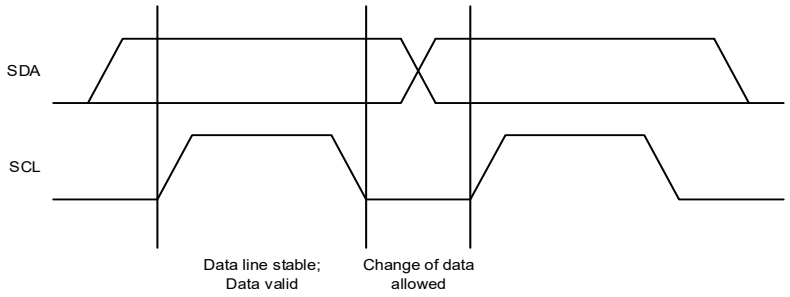


Figure12. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

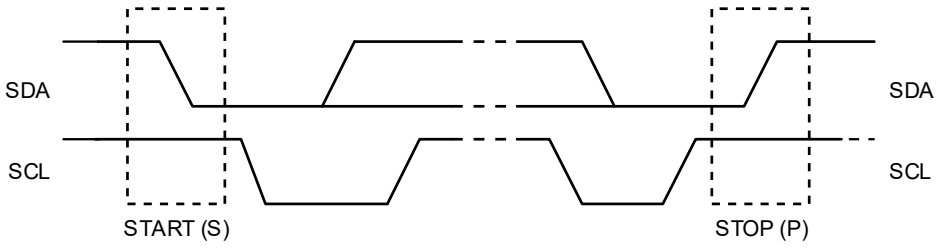


Figure13. TS START and STOP Conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the mAster into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

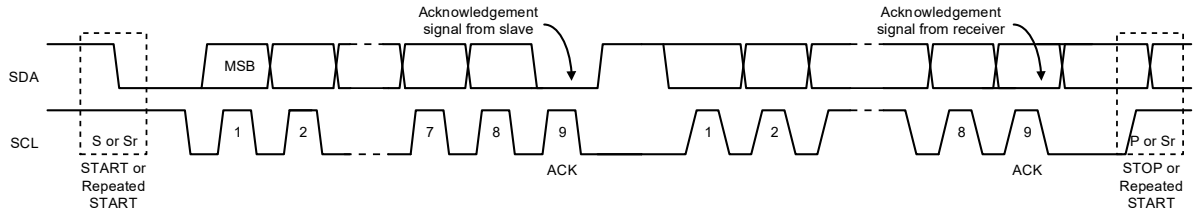


Figure14. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

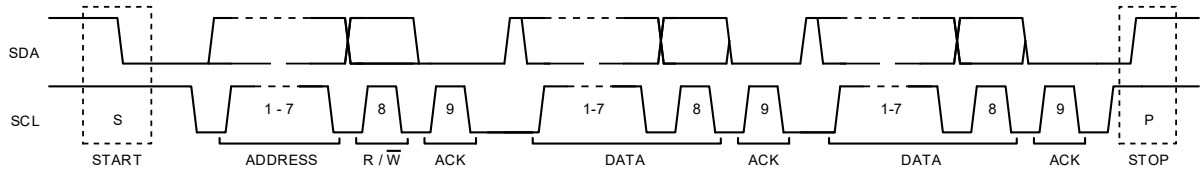


Figure15. Complete Data Transfer

Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

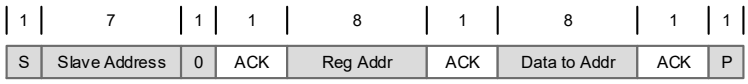


Figure16. Single Write

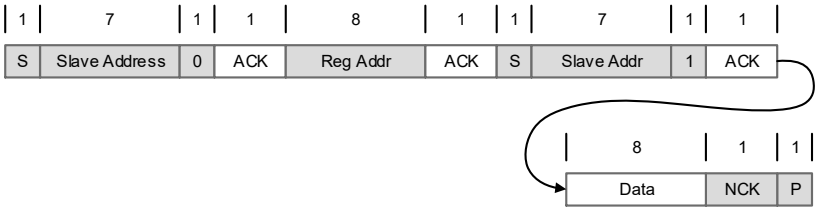


Figure17. Single Read

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG11.

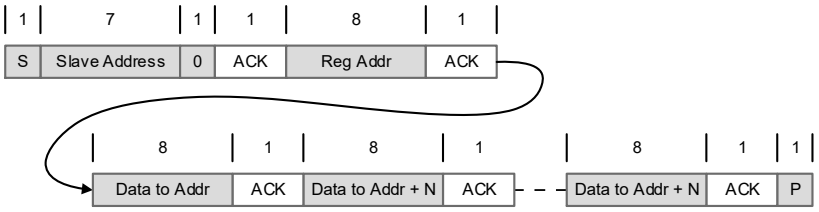


Figure18. Multi-Write

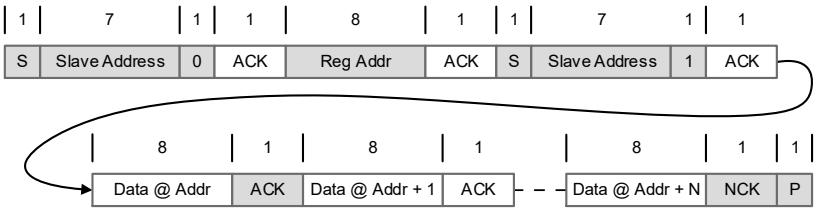


Figure19. Multi-Read

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. in order to get the fault information at present, the host has to read REG09 for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. in addition, REG09 does not support multi-read and multi-write.

Register Maps

I²C Slave Address: 6BH (1101011B + R/W)

REG00 (address = 00) [reset = 00010111]

REG00 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_HIZ	DPDM_DIS	STAT_DIS	IINDPM[4]	IINDPM[3]	IINDPM[2]	IINDPM[1]	IINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG00 Field Descriptions

Bit	Field	POR	Type[9]	Reset	Description	
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	Enable HIZ Mode 0 - Disable (default) 1 - Enable	
6	DPDM_DIS	0	R/W	by REG_RST	Disable D+/D- detection 0 - Enable (default) 1 - Disable	
5	STAT_DIS	0	R/W	by REG_RST	Disable STAT pin function (float pin) 0 - Enable (default) 1 - Disable	
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) - 3.2 A (11111) Default: 2400 mA (10111), maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed. USB SDP=500 mA USB DCP=2.4 A Unknown Adapter=500 mA Non-Standard Adapter=1 A,2A,2.1A,or 2.4A Host can over-write IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

Note9: LEGEND: R/W = Read/Write; R = Read only

REG01 (address = 01) [reset = 00011010]

REG01 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	WD_RST	OTG_CONFIG	CHG_CONFIG	SYS_Min[2]	SYS_Min[1]	SYS_Min[0]	Min_VBAT_SEL
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG01 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	Reserved	0	R	NA	
6	WD_RST	0	R/W	NA	I²C Watchdog Timer Reset 0 - Normal (default) 1- Reset (Back to 0 after watchdog timer reset)
5	OTG _CONFIG	0	R/W	by REG_RST by Watchdog	Boost (OTG) Mode Configuration 0 - OTG Disable (default) 1 - OTG Enable
4	CHG _CONFIG	1	R/W	by REG_RST by Watchdog	Charge Enable Configuration 0 - Charge Disable 1- Charge Enable (default)
3	SYS_Min[2]	1	R/W	by REG_RST	System Minimum Voltage 000: 2.6 V 001: 2.8 V 010: 3.0 V 011: 3.2 V 100: 3.4 V 101: 3.5 V 110: 3.6 V 111: 3.7 V Default: 3.5 V (101)
2	SYS_Min[1]	0	R/W	by REG_RST	
1	SYS_Min[0]	1	R/W	by REG_RST	
0	Min_VBAT_ SEL	0	R/W	by REG_RST	Minimum battery voltage for OTG mode. 0 - 2.8 V BAT falling 1 - 2.5 V BAT falling Default falling threshold 2.8 V, Rising threshold 3.0 V

REG02 (address = 02) [reset = 10100010]

REG02 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BOOST_LIM	Q1_FULLON	ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG02 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	BOOST_LIM	1	R/W	by REG_RST by Watchdog	Boost Mode Current Limit 0 - 0.5 A 1 - 1.2 A (default) The current limit options listed are minimum current limit specs.
6	Q1_FULLON	0	R/W	by REG_RST	0 - Use higher Q1 R_{DSON} when programmed I_{INDPM} < 700 mA (default, better accuracy) 1 - Use lower Q1 R_{DSON} always (better efficiency) In boost mode, full FET is always used and this bit has no effect
5	ICHG[5]	1	R/W	by REG_RST by Watchdog	Fast Charge Current Default: 1955 mA (100010) Range: 0 mA (0000000) – 3047.5 mA (110010) Note: 000000~001101: 0mA~1170mA, 90mA per step 001110~110101: 805mA~3047.5mA, 57.5 mA per step
4	ICHG[4]	0	R/W	by REG_RST by Watchdog	
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	
1	ICHG[1]	1	R/W	by REG_RST by Watchdog	
0	ICHG[0]	0	R/W	by REG_RST by Watchdog	

REG03 (address = 03) [reset = 00100010]

REG03 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG03 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	416 mA	Precharge Current Default: 156 mA (0010) Offset: 52 mA Note: IPRECHG > 676 mA clamped to 676 mA (1100)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	208 mA	
5	IPRECHG[1]	1	R/W	by REG_RST by Watchdog	104 mA	
4	IPRECHG[0]	0	R/W	by REG_RST by Watchdog	52 mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	480 mA	Termination Current Default: 180 mA (0010) Offset: 60 mA Note: ITERM > 780mA clamped to 780mA (1100)
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ITERM[0]	0	R/W	by REG_RST by Watchdog	60 mA	

REG04 (address = 04) [reset = 01011000]

REG04 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	Reserved	Reserved	VRECHG
R/W	R/W	R/W	R/W	R/W	R	R	R/W

REG04 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.856 V Range: 3.856 V to 4.624 V (11000) Default: 4.208 V (01011) Note: Value above 11000 (4.624 V) is clamped to register value 11000 (4.624V) REG04[7:3] is for compatibility, when write to REG04, VREG[0] will be automatically set 0. If need more VREG[5:0] settings, please use REG0E[7:2].
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256 mV	
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128 mV	
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64 mV	
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32 mV	
2	Reserved	0	R/W	N/A		
1	Reserved	0	R/W	N/A		
0	VRECHG	0	R/W	by REG_RST by Watchdog	Recharge threshold 0 - 100 mV (default) 1 - 200 mV	

REG05 (address = 05) [reset = 10011111]

REG05 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_TERM	Reserved	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER	TREG	JEITA_ISET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG05 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	EN_TERM	1	R/W	by REG_RST by Watchdog	Enable Charge termination 0 - Disable 1 - Enable (default)
6	Reserved	0	R/W	by REG_RST by Watchdog	
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	I^2C Watchdog Timer Setting 00 - Disable watchdog timer 01 - 40 s (default) 10 - 80 s 11 - 160 s
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog	
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	Charging Safety Timer Enable 0 - Disable 1 - Enable (default)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	Fast Charge Timer Setting 0 - 5 hrs 1 - 10 hrs (default)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 - 100 °C 1-120 °C (default) Note: REG05[1] is for compatibility, when write to REG05, TREG[1] will be automatically set 1. If need more TREG[1:0] settings, please use REG0F[7:6].
0	JEITA_ISET (0°C-10°C)	1	R/W	by REG_RST by Watchdog	JEITA Low Temperature Charge Current Setting 0 - 50% of ICHG 1 - 20% of ICHG (default)

REG06 (address = 06) [reset = 01100110]

REG06 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OVP[1]	OVP[0]	BOOSTV[1]	BOOSTV[0]	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG06 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	OVP[1]	0	R/W	by REG_RST	VAC OVP threshold: 00 - 5.5 V 01 - 6.5 V (5 V input, default) 10 - 10.5 V (9 V input) 11 - 14 V (12 V input)	
6	OVP[0]	1	R/W	by REG_RST		
5	BOOSTV[1]	1	R/W	by REG_RST	256 mV	Boost Regulation Voltage: Offset: 4.870V Range: 4.870V – 5.254V Default: 5.126V (10)
4	BOOSTV[0]	0	R/W	by REG_RST	128 mV	
3	VINDPM[3]	0	R/W	by REG_RST	Absolute VINDPM Threshold Offset: 3.9 V Range: 3.9 V (0000) - 5.4 V (1111) Default: 4.5 V (0110)	
2	VINDPM[2]	1	R/W	by REG_RST		
1	VINDPM[1]	1	R/W	by REG_RST		
0	VINDPM[0]	0	R/W	by REG_RST		

REG07 (address = 07) [reset = 01001100]

REG07 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IINDET _EN	TMR2X _EN	BATFET _DIS	JEITA _VSET	BATFET _DLY	BATFET _RST_EN	VDPM_BAT _TRACK[1]	VDPM_BA _TRACK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG07 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	Input Current Limit Detection 0 – Not in D+/D- detection 1 – Force D+/D- detection (Back to 0 after ICL detection is complete)
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation
5	BATFET_DIS	0	R/W	by REG_RST	Force BATFET off to enable ship mode 0 – Allow BATFET turn on 1 – Force BATAFET off
4	JEITA_VSET (45°C - 60°C)	0	R/W	by REG_RST by Watchdog	JEITA High Temperature Charge Voltage Setting 0 – Set Charge Voltage to VREG-200mV during JEITA high temperature 1 – Set Charge Voltage to VREG during JEITA high temperature
3	BATFET_DLY	1	R/W	by REG_RST	BATFET turn off delay control 0 – BATFET turn off immediately when BATET_DIS bit is set 1 – BATFET turn off delay by t_{SM_DLY} (typ. 10 s) when BATFET_DIS bit is set
2	BATFET_ RST_EN	1	R/W	by REG_RST by Watchdog	BATFET full system reset enable 0 – Disable BATFET full system reset 1 – Enable BATFET full system reset
1	VDPM_BAT _TRACK[1]	0	R/W	by REG_RST	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT+VDPM_TRACK. 00 – Disable tracking function (VINDPM is set by register) 01 – VBAT + 200mV 10 – VBAT + 250mV 11 – VBAT + 300mV
0	VDPM_BAT _TRACK[0]	0	R/W	by REG_RST	

REG08 (address = 08) [reset = 00000000]

REG08 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VBUS _STAT[2]	VBUS _STAT[1]	VBUS _STAT[0]	CHRG _STAT[1]	CHRG _STAT[0]	PG _STAT	THERM _STAT	VSYS _STAT
R	R	R	R	R	R	R	R

REG08 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_STAT[2]	0	R	NA	VBUS Status register 000: No input 001: USB Host SDP 010: USB CDP: (1.5A) 011: USB DCP (2.4 A) 101: Unknown Adapter (500mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Software current limit is reported in IINDPM register
6	VBUS_STAT[1]	0	R	NA	
5	VBUS_STAT[0]	0	R	NA	
4	CHRG_STAT[1]	0	R	NA	Charging status: 00 - Not Charging 01 - Pre-charge (< VBATLOWV) 10 - Fast Charging 11 - Charge Termination Done
3	CHRG_STAT[0]	0	R	NA	
2	PG_STAT	0	R	NA	Power Good status: 0 - Power Not Good 1 - Power Good
1	THERM_STAT	0	R	NA	Thermal Regulation Status 0 - Normal 1 - In Thermal regulation
0	VSYS_STAT	0	R	NA	VSYS Regulation Status 0 - Not in VSYSMIN regulation (BAT > VSYSMIN) 1 - In VSYSMIN regulation (BAT < VSYSMIN)

REG09 (address = 09) [reset = 10000000]

REG09 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WATCHDG _FAULT	OTG_FAULT	CHRG _FAULT[1]	CHRG _FAULT[0]	BAT _FAULT	NTC _FAULT[2]	NTC _FAULT[1]	NTC _FAULT[0]
R	R	R	R	R	R	R	R

REG09 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	WATCHDOG_FAUL T	1	R	NA	I²C Watchdog Fault Status 0 - Normal 1 - Watchdog timer expiration
6	OTG_FAULT	0	R	NA	Boost Mode Fault Status 0 - Normal 1 - VBUS overloaded in OTG, or VBUS OVP, or battery is too low in boost mode
5	CHRG_FAULT[1]	0	R	NA	Charger Fault Status 00 - Normal 01 - Input fault (VAC OVP or VBAT < VBUS < 3.8V) 10 - Thermal shutdown 11 - Charge Safety Timer Expiration
4	CHRG_FAULT[0]	0	R	NA	
3	BAT_FAULT	0	R	NA	Battery Fault Status 0 - Normal 1 - BATOVP
2	NTC_FAULT[2]	0	R	NA	NTC Fault Status Charge Mode: 000 - Normal 010 - TS Warm 011 - TS Cool 101 - TS Cold 110 - TS Hot Boost mode: 000 - Normal 101 - TS Cold 110-TS Hot
1	NTC_FAULT[1]	0	R	NA	
0	NTC_FAULT[0]	0	R	NA	

REG0A (address = 0A) [reset = 00000000]

REG0A Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VBUS_GD	VINDPM _STAT	IINDPM _STAT	Reserved	Reserved	ACOV_STAT	Reserved	Reserved
R	R	R	R	R	R	R	R

REG0A Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_GD	0	R	NA	VBUS Good Status 0 – Not VBUS attached 1 – VBUS attached
6	VINDPM_STAT	0	R	NA	0 - Not in VINDPM 1 - In VINDPM
5	IINDPM_STAT	0	R	NA	0 - Not in IINDPM 1 - In IINDPM
4	Reserved	0	R	NA	
3	Reserved	0	R	NA	
2	ACOV_STAT	0	R	NA	0 - Device is NOT in ACOV 1 - Device is in ACOV
1	Reserved	0	R/W	NA	
0	Reserved	0	R/W	NA	

REG0B (address = 0B) [reset = 0xxxxxxx]

REG0B Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REG_RST	PN[3]	PN[2]	PN[1]	PN[0]	Reserved	DEV_REV[1]	DEV_REV[0]
R/W	R	R	R	R	R	R	R

REG0B Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	REG_RST	0	R/W	NA	Register reset 0 - Keep current register setting 1- Reset to default register value and reset safety Timer Note: Bit resets to 0 after register reset is completed
6	PN[3]	x	R	NA	0111
5	PN[2]	x	R	NA	
4	PN[1]	x	R	NA	
3	PN[0]	x	R	NA	
2	Reserved	x	R	NA	
1	DEV_REV[1]	x	R	NA	
0	DEV_REV[0]	x	R	NA	

REG0C (address = 0C) [reset = 01100100]

REG0C Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BOOST_FREQ	BCOLD	BHOT[1]	BHOT[0]	Reserved	Reserved	Reserved	ICO_EN
R/W	R/W	R/W	R/W	R	R	R	R/W

REG0C Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	BOOST_FREQ	0	R/W	by REG_RST by Watchdog	Boost Mode Frequency Selection 0 - 1.5MHz (default) 1 - 500kHz
6	BCOLD	1	R/W	by REG_RST by Watchdog	Boost Mode Cold Temperature Monitor Threshold 0 - V_{BCOLD0} Threshold (77%, -10°C) 1 - V_{BCOLD1} Threshold (80%, -20°C) (default)
5	BHOT[1]	1	R/W	by REG_RST by Watchdog	Boost Mode Hot Temperature Monitor Threshold 00 - V_{BHOT1} Threshold (34.75%, 60°C) 01 - V_{BHOT0} Threshold (37.75%, 55°C) 10 - V_{BHOT2} Threshold (31.25%, 65°C) (default) 11 - Disable boost mode thermal protection
4	BHOT[0]	0	R/W	by REG_RST by Watchdog	
3	Reserved	0	R	NA	
2	Reserved	1	R	NA	
1	Reserved	0	R	NA	
0	ICO_EN	0	R/W	by REG_RST	Enable Input Current Limit Optimization (ICO) 0 - Disable Optimization 1 - Enable Optimization

REG0D (address = 0D) [reset = 00000000]

REG0D Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FORCE_ICO	ICO_OPTIMIZED	IDPM_LIM[5]	IDPM_LIM[4]	IDPM_LIM[3]	IDPM_LIM[2]	IDPM_LIM[1]	IDPM_LIM[0]
R/W	R	R	R	R	R	R	R

REG0D Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	FORCE_ICO	0	R/W	by REG_RST	Force Start Input Current Limit Optimization (ICO) 0 - Do not force ICO 1 - Force ICO (can be set only and will back to 0 after ICO starts)	
6	ICO_OPTIMIZED	0	R	NA	Input Current Limit Optimization (ICO) Status 0 - Optimization is in progress 1 - Maximum Input Current Detected	
5	IDPM_LIM[5]	0	R	NA	1600 mA	Input Current Limit in effect while Input Current Optimizer (ICO) is enabled Offset: 100mA Range: 100mA (000000) - 3.25A (111111)
4	IDPM_LIM[4]	0	R	NA	800 mA	
3	IDPM_LIM[3]	0	R	NA	400 mA	
2	IDPM_LIM[2]	0	R	NA	200 mA	
1	IDPM_LIM[1]	0	R	NA	100 mA	
0	IDPM_LIM[0]	0	R	NA	50 mA	

REG0E (address = 0E) [reset = 01011000]

REG0E Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VREG[5]	VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	VREG[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG0E Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	VREG[5]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.856 V Range: 3.856 V to 4.624 V (110000) Default: 4.208 V (010110) Note: Value above 1100 00 (4.624 V) is clamped to register value 110000 (4.624 V)
6	VREG[4]	1	R/W	by REG_RST by Watchdog	256 mV	
5	VREG[3]	0	R/W	by REG_RST by Watchdog	128 mV	
4	VREG[2]	1	R/W	by REG_RST by Watchdog	64 mV	
3	VREG[1]	1	R/W	by REG_RST by Watchdog	32 mV	
2	VREG[0]	0	R/W	by REG_RST by Watchdog	16 mV	
1	VREG_FT	0	R/W	by REG_RST by Watchdog	8 mV	VREG Fine Tuning 0 = Disable (default) 1 = VREG+8mV
0	BAT_LOADEN	0	R/W	by REG_RST by Watchdog	Battery Load ($I_{BATLOAD}$) Enable 0 - Disable 1 - Enable	

REG0F (address = 0F) [reset = 11000000]

REG0F Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TREG[1]	TREG[0]	BAT_COMP[2]	BAT_COMP[1]	BAT_COMP[0]	VCLAMP[2]	VCLAMP[1]	VCLAMP[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG0F Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	TREG[1]	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold 00 - Disable TREG 01 - 80°C 10 - 100°C 11 - 120°C (default)	
6	TREG[0]	1	R/W	by REG_RST by Watchdog		
5	BAT_COMP[2]	0	R/W	by REG_RST by Watchdog	80 mΩ	IR Compensation Resistor Setting Range: 0 - 140 mΩ Default: 0 mΩ (000) (i.e. Disable IR Comp)
4	BAT_COMP[21]	0	R/W	by REG_RST by Watchdog	40 mΩ	
3	BAT_COMP[0]	0	R/W	by REG_RST by Watchdog	20 mΩ	
2	VCLAMP[2]	0	R/W	by REG_RST by Watchdog	128 mV	IR Compensation Voltage Setting Offset: 0 mV Range: 0 - 224 mV Default: 0 mV (000)
1	VCLAMP[1]	0	R/W	by REG_RST by Watchdog	64 mV	
0	VCLAMP[0]	0	R/W	by REG_RST by Watchdog	32 mV	

REG10 (address = 10) [reset = 00000000]

REG10 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_12V	DP_DAC[2]	DP_DAC[1]	DP_DAC[0]	HVDCP_EN	DM_DAC[2]	DM_DAC[1]	DM_DAC[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

REG10 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	EN_12V	0	R/W	by REG_RST	Enable HVDCP 12V 0 - HVDCP 9 V (default) 1 - HVDCP 12 V
6	DP_DAC[2]	0	R/W	by REG_RST	D+ Pin Output Driver 000 - HiZ mode (default) 001 - 0V 010 - 0.6V 011 - 1.2V 100 - 2.0V 101 - 2.7V 110 - 3.3V 111 - 3.3V
5	DP_DAC[1]	0	R/W	by REG_RST	
4	DP_DAC[0]	0	R/W	by REG_RST	
3	HVDCP_EN	0	R/W	by REG_RST	High Voltage DCP handshake Enable on D+/D- 0 - Disable HVDCP handshake (default) 1 - Enable HVDCP handshake
2	DM_DAC[2]	0	R/W	by REG_RST	D- Pin Output Driver 000 - HiZ mode (default) 001 - 0V 010 - 0.6V 011 - 1.2V 100 - 2.0V 101 - 2.7V 110 - 3.3V 111 - 3.3V
1	DM_DAC[1]	0	R/W	by REG_RST	
0	DM_DAC[0]	0	R/W	by REG_RST	

REG11(address = 11) [reset = 00000110]

REG11 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	VINDPM[6]	VINDPM[5]	VINDPM[4]	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

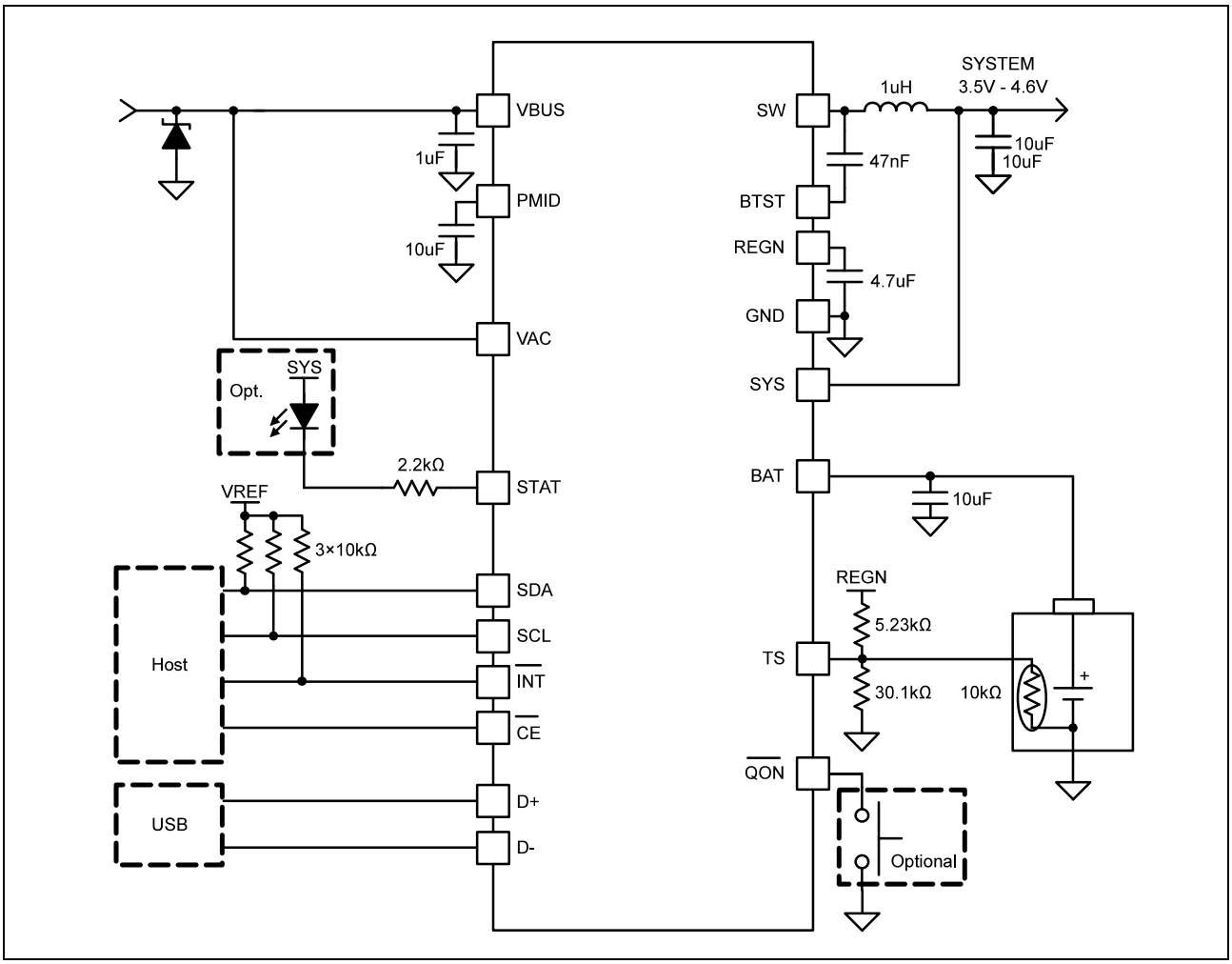
REG11 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	Reserved	0	R	NA		
6	VINDPM[6]	0	R/W	by REG_RST	6400 mV	Absolute VINDPM Threshold Offset: 3.9V Range: 3.9V (0000000) - 14.2V (1100111) Default: 4.5V (0000110)
5	VINDPM[5]	0	R/W	by REG_RST	3200 mV	
4	VINDPM[4]	0	R/W	by REG_RST	1600 mV	
3	VINDPM[3]	0	R/W	by REG_RST	800 mV	
2	VINDPM[2]	1	R/W	by REG_RST	400 mV	
1	VINDPM[1]	1	R/W	by REG_RST	200 mV	
0	VINDPM[0]	0	R/W	by REG_RST	100 mV	

Application information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

Typical Application Circuit



Design Requirements

Inductor Selection

The 1.5 MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2) \times I_{RIPPLE}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current IC in occurs where the duty cycle is closest to 50% and can be estimated using:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25 V or higher capacitor is preferred for 15 V input voltage. Capacitance of 22 µF is suggested for typical of 3 A charging current.

Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. The formula shows the output capacitor RMS current I_{COUT} calculation:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE}$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

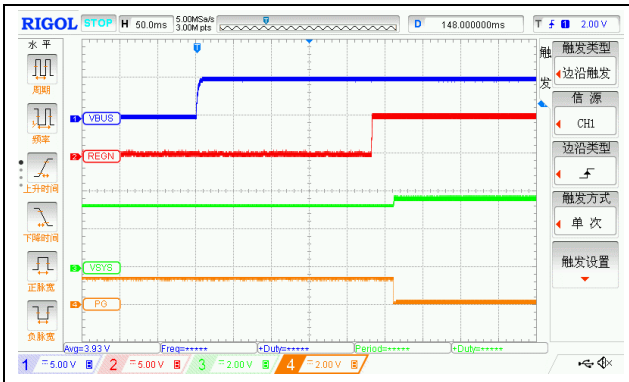
At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for >20 µF ceramic output capacitance. The preferred ceramic capacitor is 10 V rating, X7R or X5R.

Power Supply Recommendations

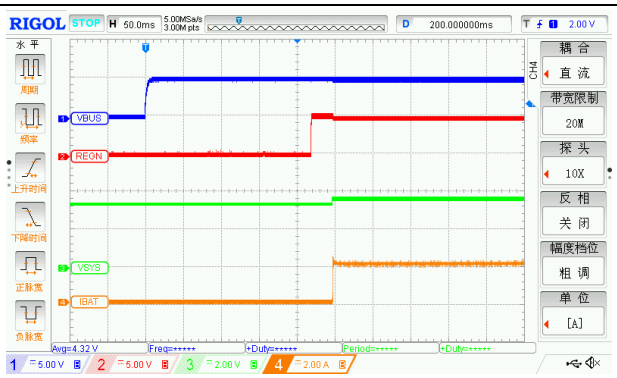
In order to provide an output voltage on SYS, the ET95601CX device requires a power supply between 3.9 V and 14.2 V input with at least 100 mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

Application Curves



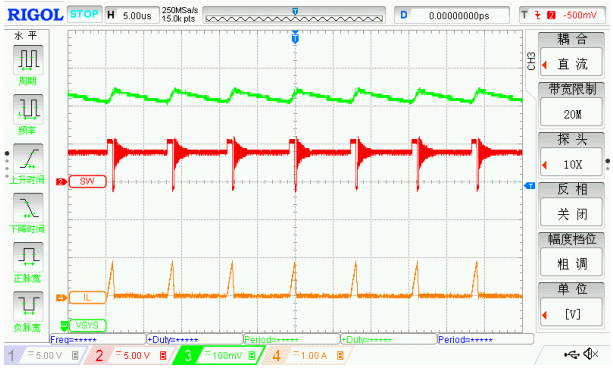
VBUS=5V, VBAT=3.2V

Figure 20. Power-Up with Charge Disabled



VBUS=5 V, VBAT=3.2 V, ICHG=2 A

Figure 21. Power-Up with Charge Enabled

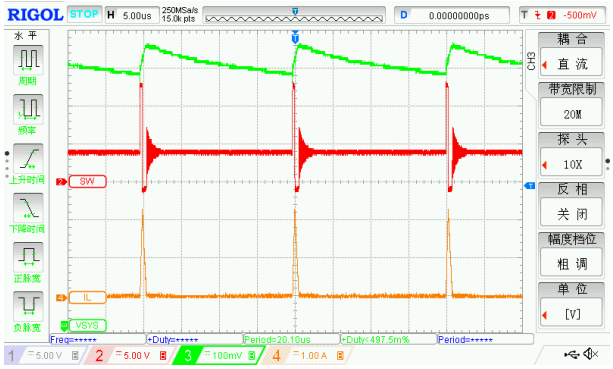


VBUS=5V, ISYS=50mA, charge disabled, no bat

Figure 22. PFM Switching in Buck Mode

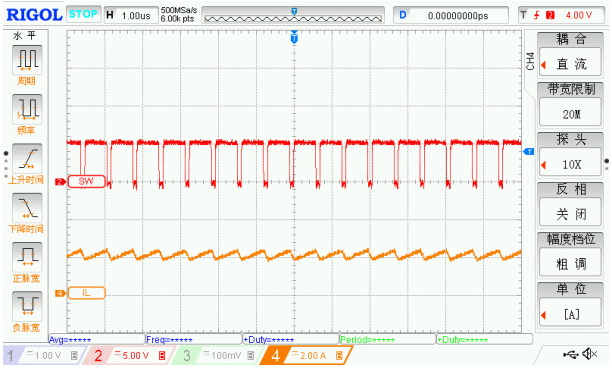
VBUS=9V, ISYS=50mA, charge disabled, no bat

Figure 23. PFM Switching in Buck Mode



VBUS=12V, ISYS=50mA, charge disabled, no bat

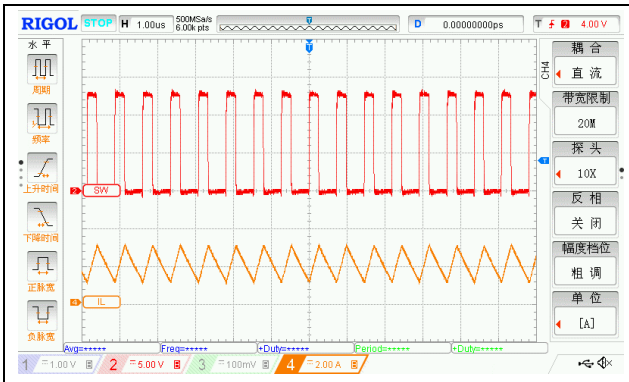
Figure 24. PFM Switching in Buck Mode



VBUS=5V, VBAT=3.8V, ICHG=2A

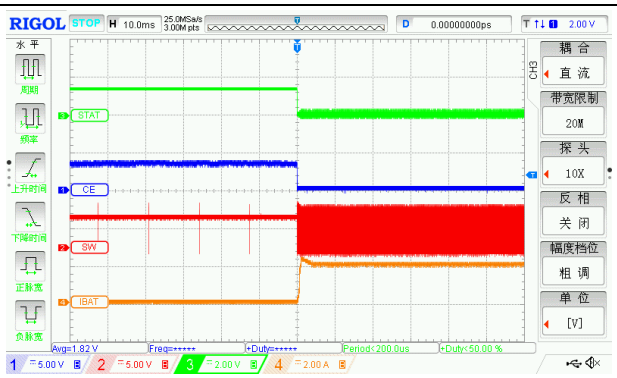
Figure 25. PWM Switching in Buck Mode

Application Curves(Continued)



VBUS=12V, VBAT=3.8V, ICHG=2A

Figure 26. PWM Switching in Buck Mode



VBUS=5V, VBAT=3.2 V, ICHG=2 A

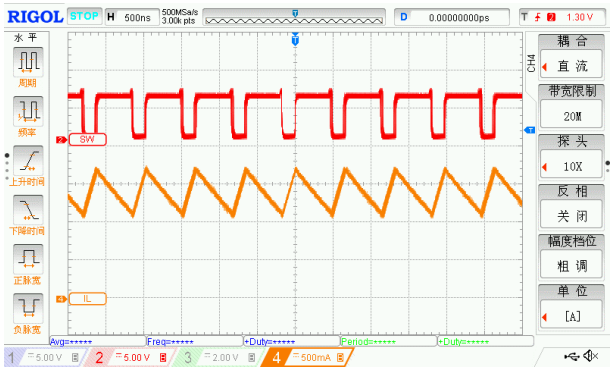
Figure 27. Charge Enabled

VBUS=5V, VBAT=3.2V, ICHG=2A

Figure 28. Charge Disable

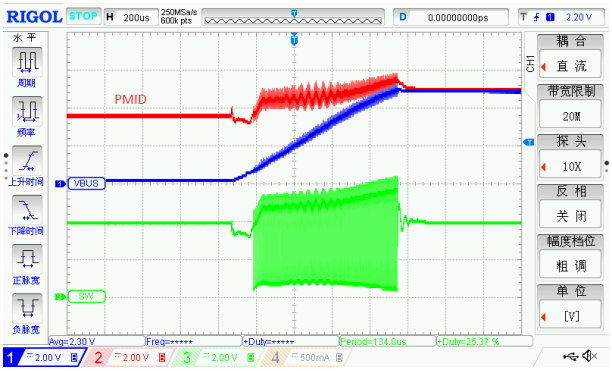
VBAT=4V, ILOAD=50 mA , PFM Enabled

Figure 29. OTG Switching



VBAT=4V, ILOAD=1A , PFM Enabled

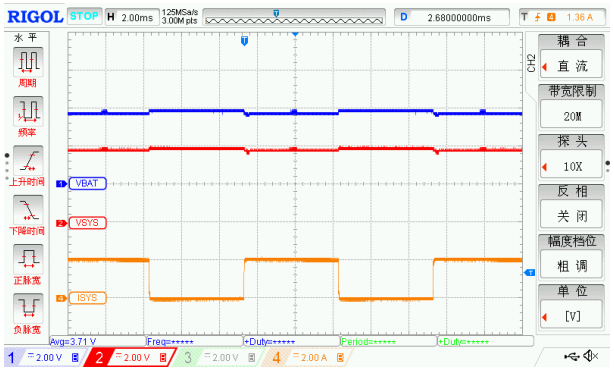
Figure 30. OTG Switching



VBAT=3.8V, Cload=470uF

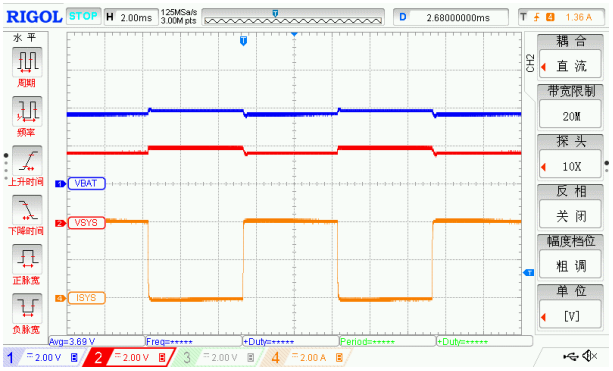
Figure 31. OTG Start-Up

Application Curves(Continued)



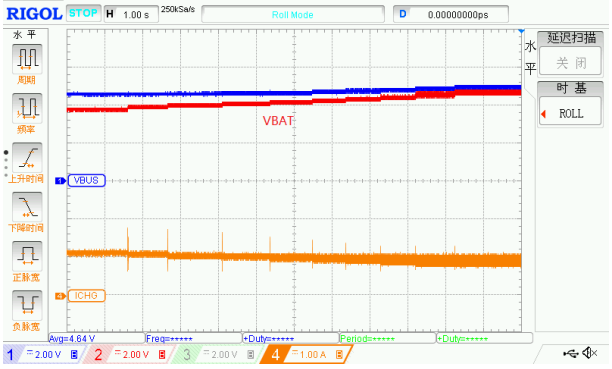
VBUS=5V, IINDPM=2A, ISYS from 0 A to 2 A
ICHG=2 A, VBAT=3.7 V

Figure 32. System Load Transient



VBUS=5V, IINDPM=2A, ISYS from 0 A to 4 A,
ICHG=2 A, VBAT = 3.7 V

Figure 33. System Load Transient



VBAT=3.6V~4.4V, Adaptor ILIM=1 A

Figure 34. VINDPM Tracking Battery Voltage

Layout

Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see the picture) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.

2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.

4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0 Ω resistor to tie analog ground to power ground.

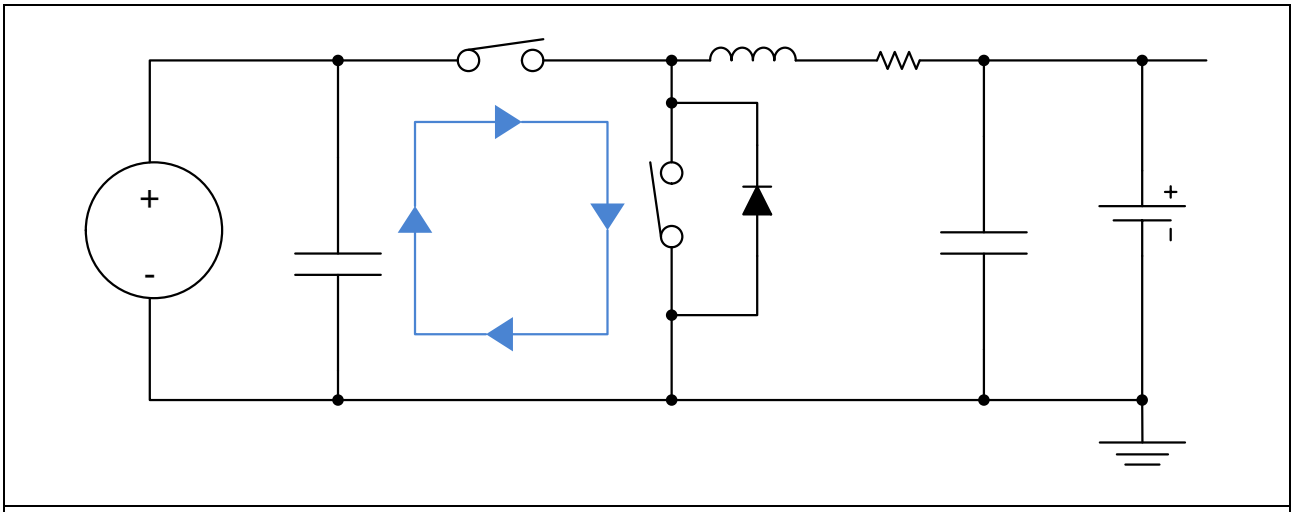
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.

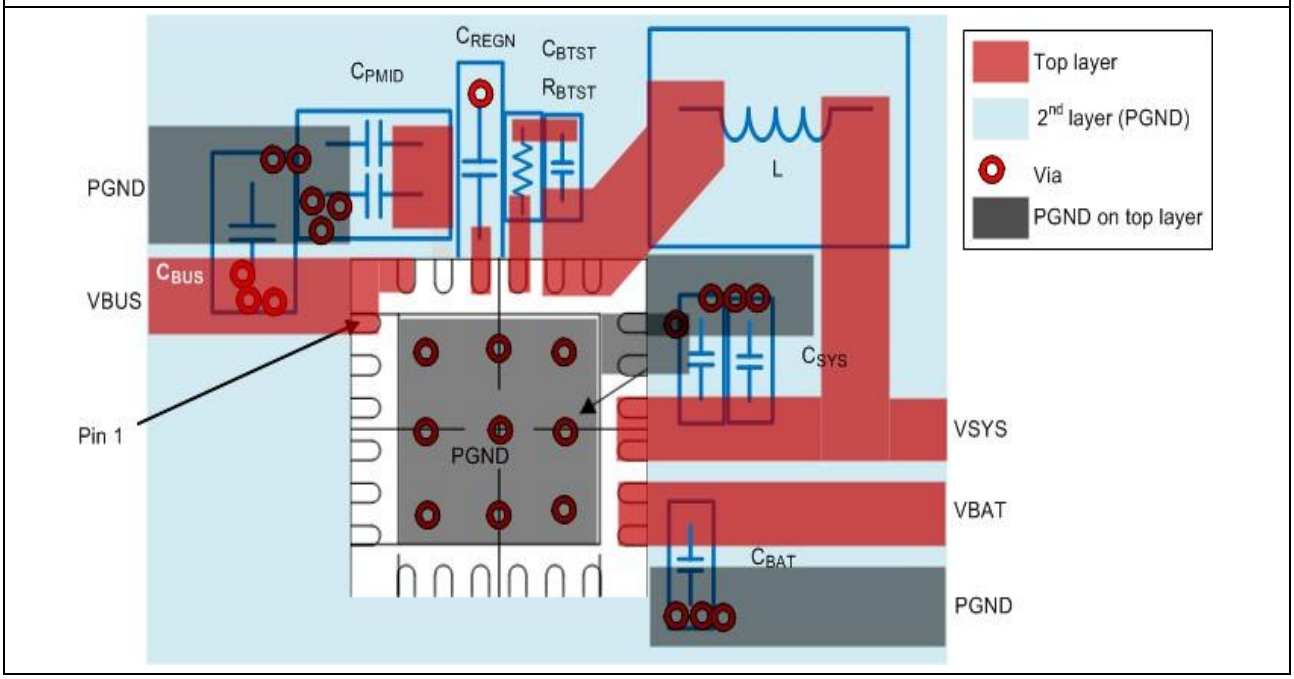
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.

7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

8. Ensure that the number and sizes of vias allow enough copper for a given current path.

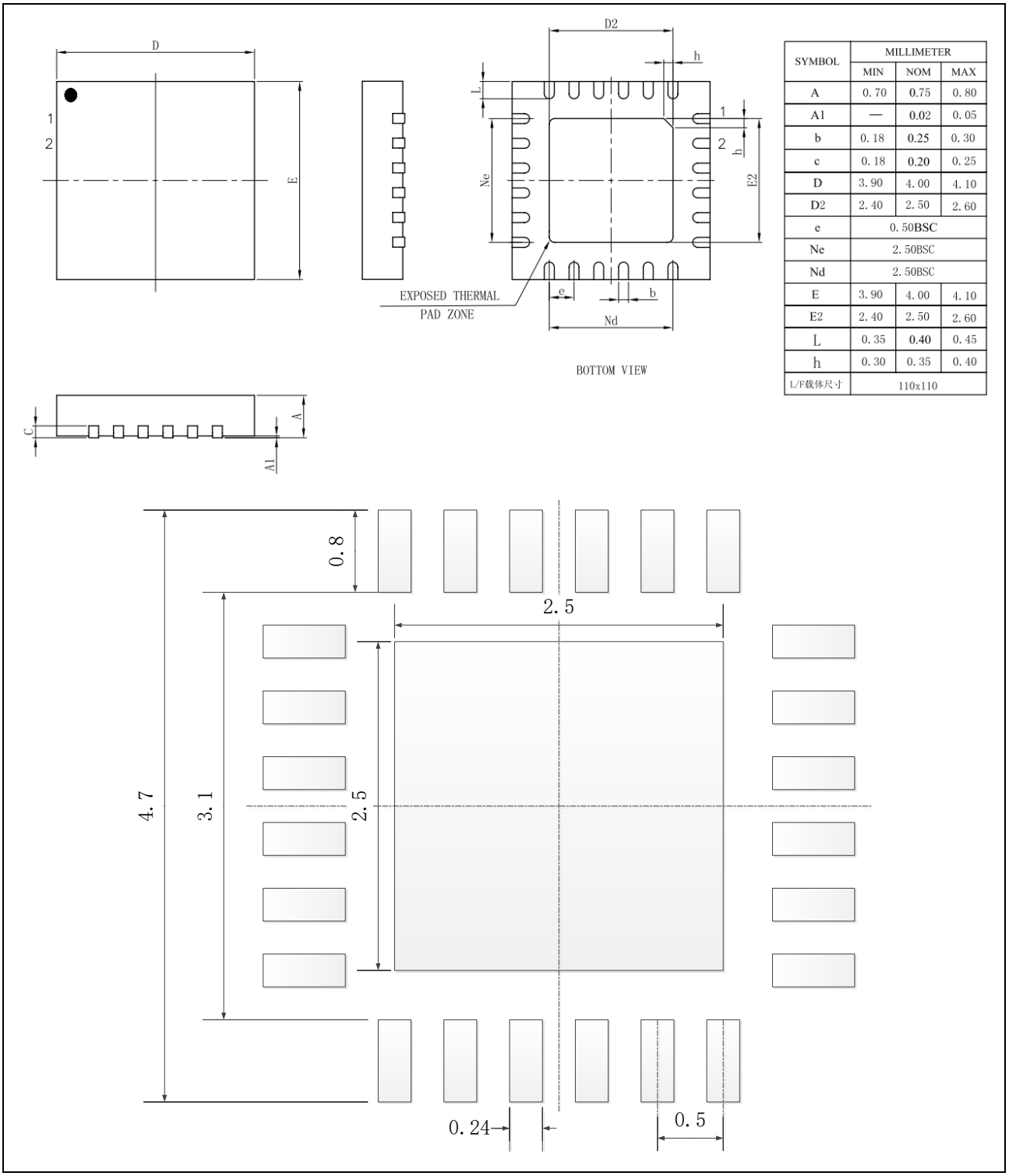
Layout Example





Package Dimension

QFN24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	110x110		

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2023-10-12	Initial Version	Chenzx	Xiayj	Liujy
1.1	2024-12-04	Update Typeset	Chenzx	Xiayj	Liujy