Linear Single Cell Li-Ion Battery Charger with Power Path Management, I²C Control and UART Communication

General Description

ET9563 is a linear single cell Li-ion battery charger integrated power path management. The charger uses a CC/CV charge profile required by Li-ion battery. It also accepts an input voltage up to 18V and will cut off rapidly when the input voltage exceeds OVP threshold (Typically 6.0V). The charger features precharge, constant current and constant voltage regulation, charge termination, and charge status.

The internal Power Path Management can balance the input current to system and battery, which ensures continuous power to the system from input, battery or both. Also ET9563 integrates dynamic power management. When system load is heavy, the charge current will be reduced to keep input current or input voltage in regulation.

ET9563 provides over-current protection from input to the system and battery to the system. This can prevent the Li-on battery from being damaged by excessively high current. Input and battery under-voltage lockout(UVLO) will cuts off the load path when power supply is unstable. An integrated I²C control interface allows the ET9563 to program the critical parameters, such as battery constant voltage, constant charge current, precharge threshold, battery regulation voltage, battery UVLO, input voltage regulation, input current regulation, and system voltage regulation.

The ET9563 can support UART communication channel between UART and VIN pin.

The ET9563 can support TWS earphones in/out auto-detection.

The ET9563's high integration can simply system design and reduce the number of components outside. The device is packaged in advanced Full-Green compliant CSP12 package.

Device Information

Part No.	Package	MSL
ET9563	CSP12(1.65mm×2.05mm,0.4mm pitch)	Level 1

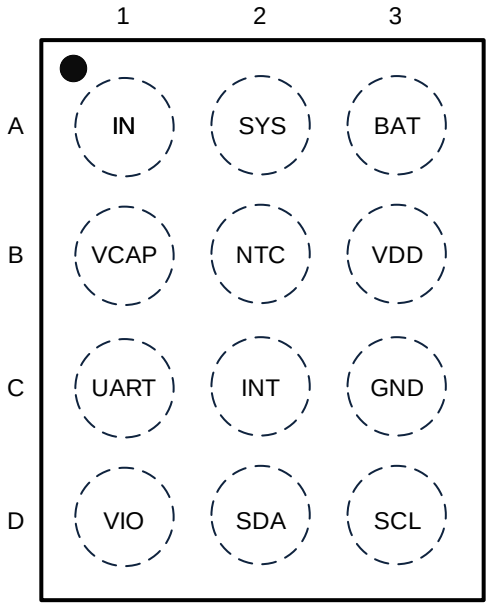
Features

- 18V Maximum Rating for VIN Power
- Internal 6.0V Over Input Voltage Protection
- Fully Autonomous Charger for Single-Cell Li-on Battery
- Auto Power Path Management for Powering the System and Charging the Battery
- Integrated Power MOSFETs for System Load and Charging Mode
- ±0.5% Charging Voltage Accuracy
- Support Setting Communication Channel Between UART and VIN Port
- Support JACK-in/OUT Auto-detection.
- Support One-wire Protocol Commutation with TWS BOX Through Voltage De-modulation and Current Modulation in VIN Port.
- I^2C Interface for Setting Parameters
- Built-In Input and Battery UVLO Protection
- Thermal Limiting Regulation On-Chip
- Outside OTP Sensing by NTC Pin
- CSP12 Package

Application

- Smart Watches
- Wearable Devices
- IP Camera

Pin Configuration

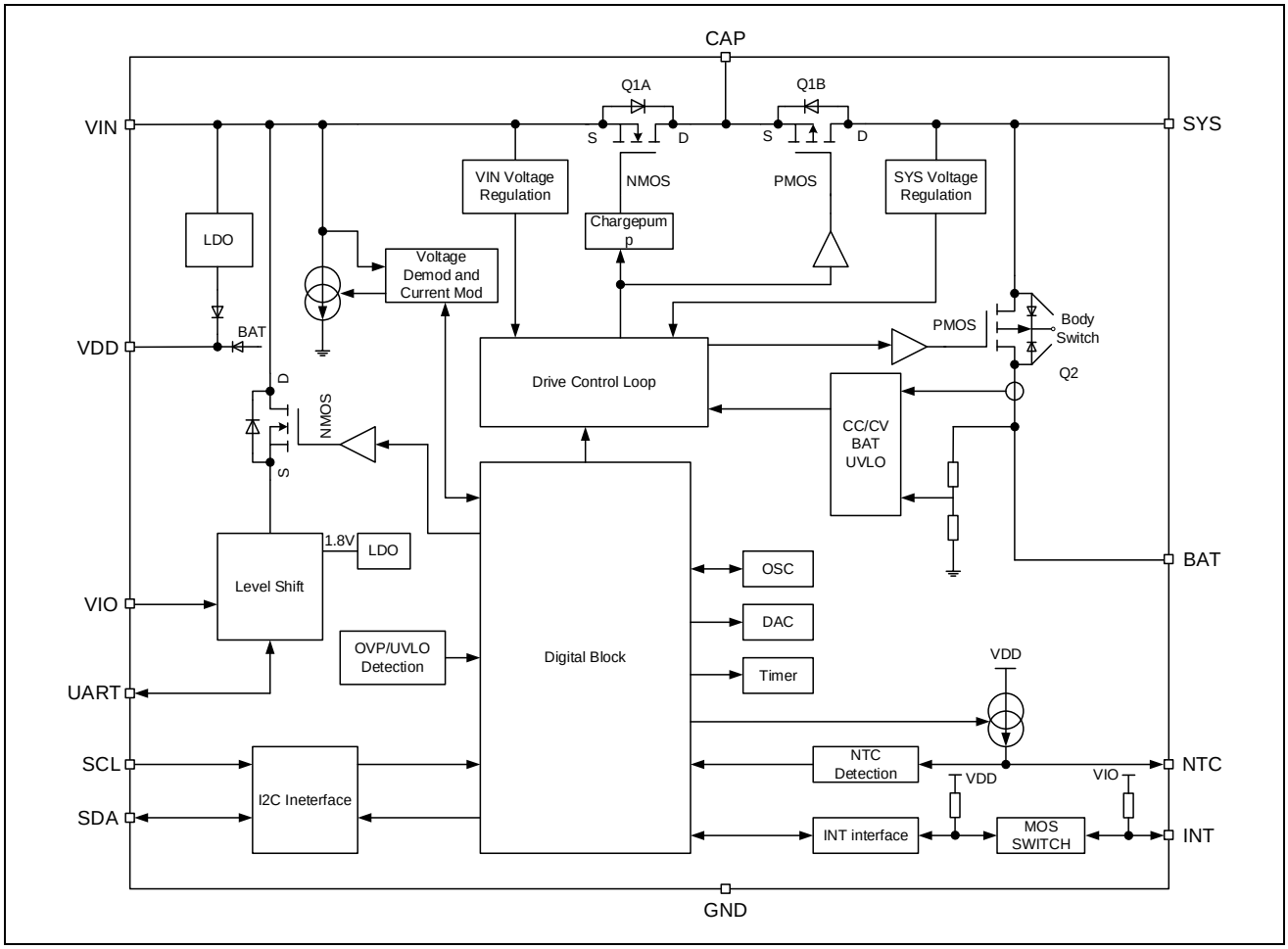


Top View

Pin Function

Pin No.	Pin Name	Description
A1	IN	Power Supply Input Pin
A2	SYS	System Connect Pin
A3	BAT	Charge Output Pin
B1	VCAP	Capacitor of VIN
B2	NTC	Thermal Sense Pin
B3	VDD	Internal Control Power Supply
C1	UART	UART Communication Pin
C2	INT	Open Drain Interrupt Output(with 200k pull-up resistor to VIO)
C3	GND	Ground
D1	VIO	Power Supply of UART Communication
D2	SDA	I^2C interface data
D3	SCL	I^2C interface clock

Block Diagram



Functional Description

ET9563 is a linear single cell Li-ion battery charger integrated power path management. The charger uses a CC/CV charge profile required by Li-ion battery. It also accepts an input voltage up to 24V and will cut off rapidly when the input voltage exceeds OVP threshold(Typically 6.0V). The charger features precharge, constant current and constant voltage regulation, charge termination, and charge status.

The internal Power Path Management can balance the input current to system and battery, which ensures continuous power to the system from input, battery or both. It allows for separate control between the system and the battery, and has high priority to power supply system.

The internal Dynamic Power Management can regulates the input voltage to V_{IN_REG} when the load is over the input power capacity. The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero and the input source is still over-loaded, system voltage starts to fall down. Once the system voltage falls below the battery voltage, ET9563 enters battery supplement mode.

ET9563 provides over-current protection from input to the system and battery to the system. This can prevent the Li-on battery from being damaged by excessively high current. Input and battery under-voltage lockout(UVLO) will cuts off the load path when power supply is unstable. An integrated I^2C control interface

allows the ET9563 to program the critical parameters, such as battery constant voltage, constant charge current, precharge threshold, battery regulation voltage, battery UVLO, input voltage regulation, input current regulation, and system voltage regulation.

The ET9563 can support UART communication channel between UART and VIN pin.

The ET9563 can support TWS earphones in/out auto-detection.

ET9563 can support one-wire protocol commutation with TWS BOX through voltage de-modulation and current modulation in VIN port.

ET9563 include Battery Discharge Mode, Battery Supplement Mode, Battery Charge Mode, Only Power System Mode and Shipping Mode, Figure 1 is shown the internal state machine conversion.

(1) Battery Discharge Mode: Only Battery to SYS Path is enabled.
(2) Battery Supplement Mode: IN to SYS path and Battery to SYS path are enabled.
(3) Battery Charge Mode: IN to SYS path and IN to Battery path are enabled.
(4) Only Power System Mode: Only IN to SYS Path is enabled.
(5) Shipping Mode: All paths are disabled,ET9563 enters into low power consumption state.

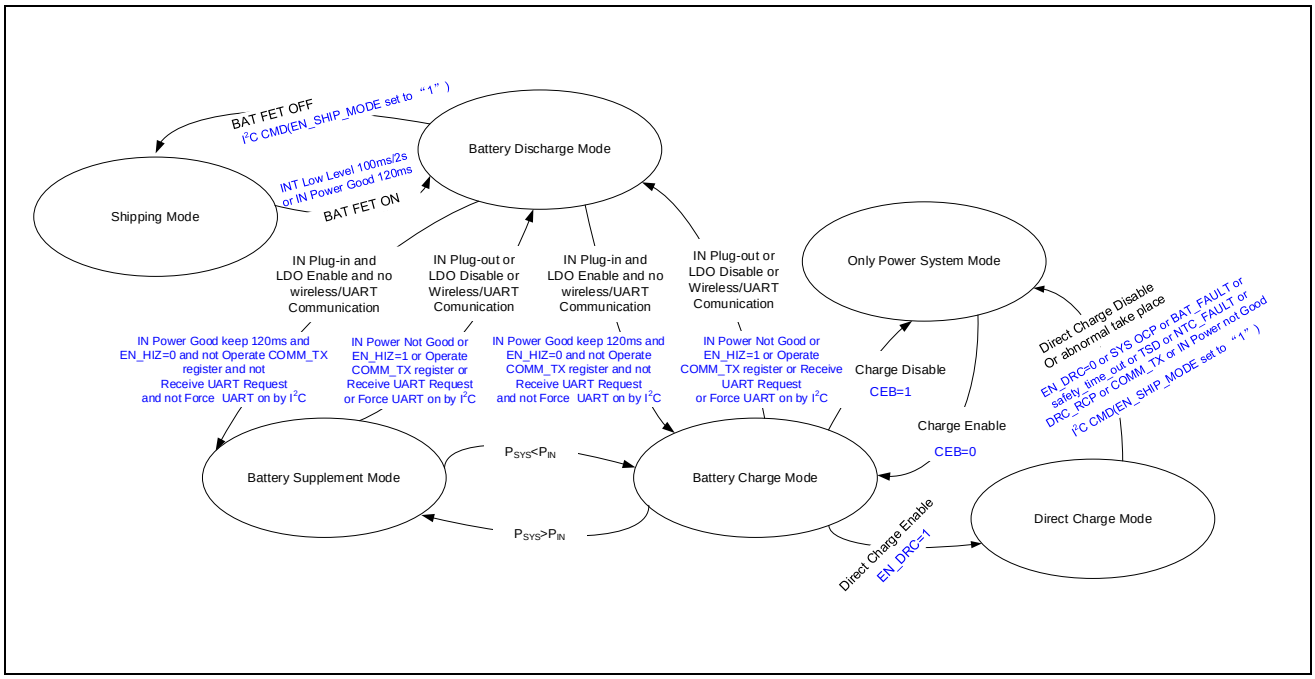


Figure 1. State Machine Conversion

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN or BAT. When IN>2.4V or BAT>2V, the sleep comparator, battery depletion comparator, and the battery MOSFET driver are active. After 2ms, the I²C interface is ready for communication and all registers are reset to the default value. The host can access all registers.

Input OVP and UVLO

The ET9563 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the

input voltage exits the normal input voltage range, the Q1 MOSFET is turned off immediately.

When the input voltage is identified as a good source, a 20ms handshake timer(include ACK time) is active. If the input power is still sufficient until the 20ms timer expires, the system starts up. Otherwise, Q1 remains off. Figure 2 depicts the operation profile.

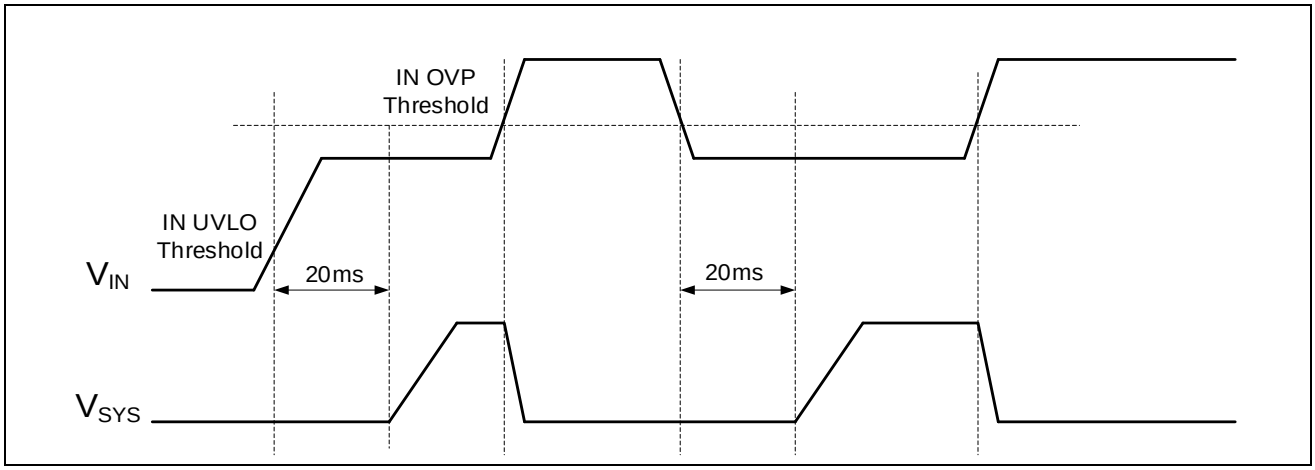


Figure 2. Input Power Detection Operation Profile

Power Path Management

The IC employs a direct power path structure with the battery MOSFET decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missed battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_VSET} by the integrated LDO MOSFET. The system voltage can be programmable via Reg15[7:4].

As shown in Figure 3, the direct power structure is composed of a frond-end LDO MOSFET between IN and SYS and a battery FET between SYS and BAT. The Input LDO can be changed to switch mode by set EN_DRC: Reg1D[5]=1; And The input LDO can be closed by set EN_HIZ: Reg1D[7]=1.

IN LDO mode, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO MOSFET is fully on with the input current limit.

IN switch mode, the voltage of SYS will not higher than the V_{SYS_VSET} which set by Reg15[7:4].

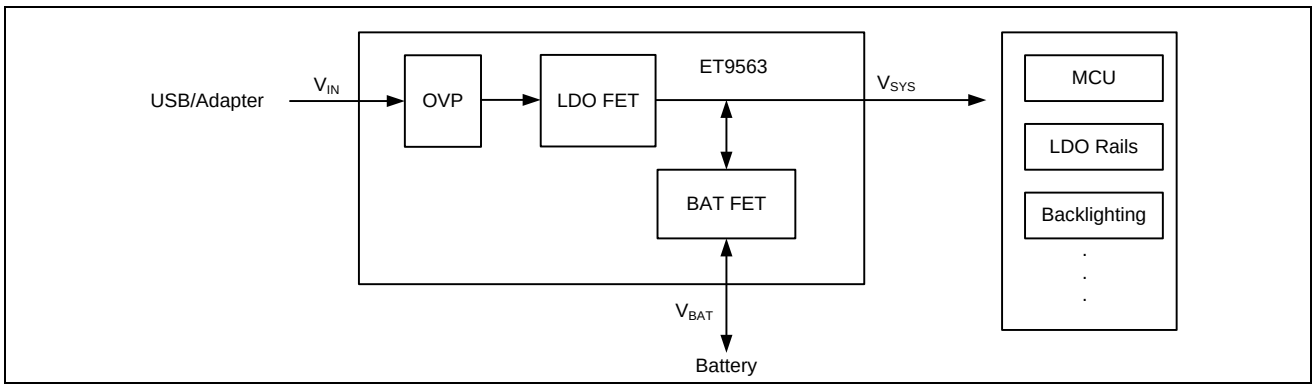


Figure 3. Power Path Management Structure

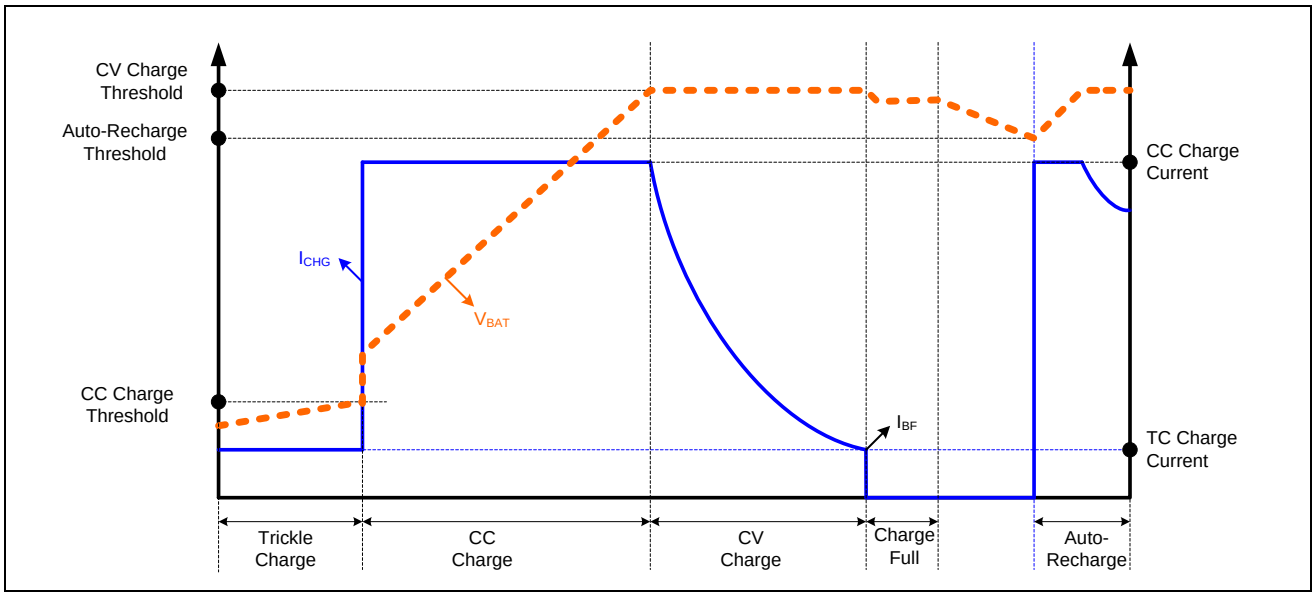


Figure 4. Battery Charge Profile

Battery Charge Profile

The IC provides three main charging phases: precharge, constant current charge, and constant voltage charge (see Figure 4).

1. Phase 1 (precharge): The IC is able to safely precharge the deeply depleted battery until the battery voltage reaches the precharge to the fast charge threshold (V_{BAT_LOW}). The precharge current is programmable via Reg13[3:0]. If V_{BAT_LOW} is not reached before the precharge timer (1hr) expires, the charge cycle is ceased, and a corresponding timeout fault signal is asserted.

2. Phase 2 (constant current charge): When the battery voltage exceeds V_{BAT_LOW}, the IC enters a constant-current charge (fast charge) phase. The fast charge current can be programmable via Reg12[7:0].

3. Phase 3 (constant voltage charge): When the battery voltage rises to the pre-programmable charge full voltage (V_{BAT_REG}) set via Reg13 bit [6:0], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

Assuming the termination function (EN_TERM) is set via Reg17[7] = 1, the charge cycle is considered complete when the following conditions are valid:

- The charge current (I_{BAT}) reaches the end of charge (EOC) current threshold(I_{TERM}), and the 64ms delay timer is initiated.
- During the 64ms delay period, I_{BAT} is always smaller than I_{EOC}.

After the 64ms delay timer expires, the ET9563 enters into Top Off mode, the charge current will tape off until the Top Off timer expires. The charge current will be terminated, and the charge status is marked after Top Off timer expires.

The charge current is terminated at the same time if TERM_TMR is set via Reg17[6] = 0; otherwise, the charge current keeps tapering off.

If EN_TERM=0(Reg17[7] = 0), the termination function is disabled, the above actions will not occur. During

the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. If the input current or the input voltage reach their limits during the CV charge, the charge full termination is not influenced when the charge current is not so close to the EOC current specification.

A new charge cycle starts when the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by the I^2C

Under the following conditions:

- No thermistor fault at NTC
- No safety timer fault
- No battery over-voltage
- BATFET is not forced to turn off

Switch Charge Mode

The Charge mode can be changed to switch mode by set Reg1D[5]=1(EN_DRC). And the fast charge current set by Reg12[7:0] can be used as limit current in switch mode. In switch mode, the MOSFETs of VIN to SYS, SYS to BAT are in switch state. And the low current protection can be set by Reg17[5:0] (I_{UCP}), when the charge current smaller than I_{UCP}, the state register Reg32[4]=1.

In switch charge mode, when the ET9563 enter into OVP, UVP, OTP, OCP, NTC and so on, it will exit from switch charge mode and stop charging. It will enter into switch charge mode again after setting registers CEB(Reg1D[6]), EN_DRC(Reg1D[5]) again.

Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold, and VIN is still in the operation range, the IC begins another new charging cycle automatically without the requirement of restarting a charging cycle manually.

The auto-recharge function is valid only when EN_TERM=1 and TERM_TMR=0.

Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 130mV higher than V_{BAT_REG}. When the battery over-voltage event occurs, the IC suspends the charging immediately and asserts a fault.

Input Current and Input Voltage Based Power Management

To meet the input source (usually USB) maximum current limit specification, the IC uses input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the I^2C to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, back-up input voltage-based power management also works to prevent the input source from being overloaded. If either the input current

limit or the input voltage limit is reached, the Q1 MOSFET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to the minimum value of V_{SYS}-90mV or V_{IN}-160mV, the charge current is reduced to prevent the system voltage from dropping further.

Voltage-based DPM regulates the input voltage to V_{IN_REG} when the load is over the input power capacity. V_{IN_REG} set by Reg10[7:4].

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero, and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the IC enters battery supplement mode. When the system voltage is 30mV below the battery voltage, the ideal diode mode is enabled. The battery MOSFET is regulated to maintain V_{BAT}-V_{SYS} at 22.5mV. If the supplement current I_{DSG}*R_{ON_BAT} is higher than 22.5mV, the battery MOSFET is fully turned on to keep the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BAT}+20mV, ideal diode mode is disabled.

Figure 5 shows the dynamic power management and battery supplement mode operation profile.

When VIN is not available, the IC operates in discharge mode, and the battery MOSFET is always fully on to reduce loss.

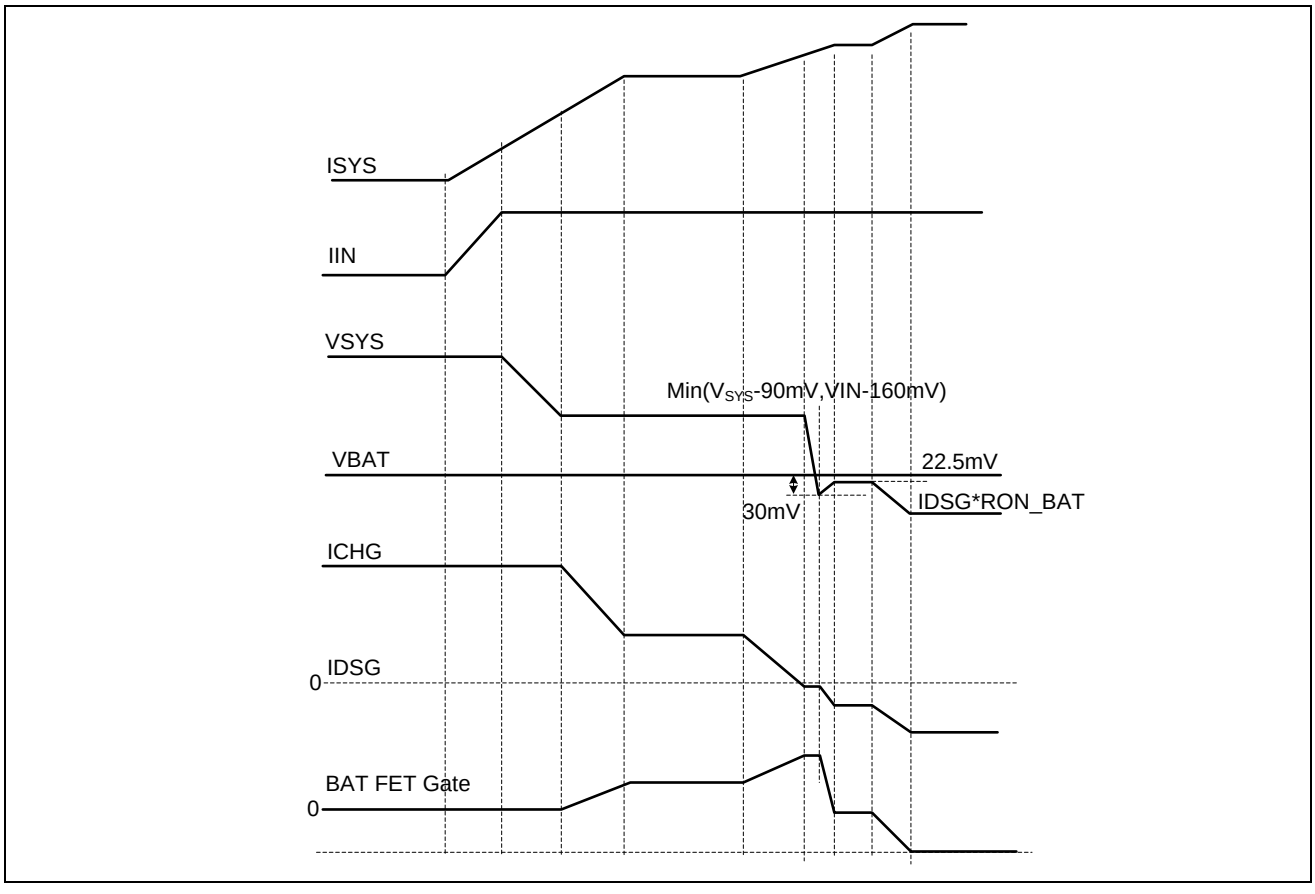


Figure 5. Dynamic Power Management and Battery Supplement Operation Profile

Battery Charge Full Voltage

The battery voltage for the constant voltage regulation phase is V_{BAT_REG}. When V_{BAT_REG} is 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating.

When the internal junction temperature reaches the pre-set limit of T_{REG} (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications.The junction temperature regulation threshold can be set via Reg18 bit [6:5].

When the junction temperature reaches 150°C, IN to SYS path and SYS to BAT path will be closed. But the BAT to SYS discharge path is still open.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment for the chip. A thermistor with an appropriate value(10K, B25/85=3435K) should be connected from NTC to GND. A 50μA bias current will be added to the thermistor, and the voltage on NTC port depends on the temperature. In order to reduce the power consumption, the ET9563 will detect the voltage of the NTC port by using a periodic interval, the register Reg18[2:1] can set the duty of sampling the voltage for NTC port, the cycle is 5 seconds.

The I²C default setting is the PCB OTP. The function can be changed through the I²C (see Table 1).

I²C Control		Function
EN_NTC	EN_PCB_OTP	
0	X	Disable
1	1	NTC(JEITA)
1	0	PCB OTP

Table 1. NTC Function Selection Table

When PCB OTP is selected, if the NTC voltage is lower than the NTC hot threshold, both the LDO MOSFET and battery MOSFET are off. The PCB OTP fault sets the NTCH_FAULT status (Reg31 bit [2:0]=101) to indicate the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function only works in charge mode. Once the NTC voltage falls out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

When Reg18[4:3]=11, ET9563 enter into NTC(JEITA) mode, there are four thermal threshold T1, T2, T3, T4. T2, T3 can be set by Reg19[3:2] (JEITA_T3_TEMP, JEITA_T2_TEMP).

If the battery temperature lower than T1, ET9563 enters into cold state, and stop charging.

If the battery temperature lower than T2, higher than T1, ET9563 enters into cool state, and the charge current will be reduced. The charge current in cool mode can be set by Reg19[7:6] (JEITA_T2_ISET).

If the battery temperature lower than T3, higher than T2, it is normal state.

If the battery temperature lower than T4, higher than T3, ET9563 enters into warm state, the battery regulation voltage will be reduced. The battery regulation voltage can be set by Reg19[5:4] (JEITA_T3_VSET).

If the battery temperature higher than T4, ET9563 enters into hot state, and stop charging.

The NTC state can be read by Reg31[2:0].

Safety Timer

The IC provides both a precharge and a fast charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer is one hour when the battery voltage is below $V_{PRE\_CHAR\_VSET}$. The fast charge safety timer begins when the battery enters fast charging. The fast charge safety timer can be programmed through the I^2C. The safety timer feature can be disabled via the I^2C.

The following actions restart the safety timer:

- A new charge cycle is kicked in Reg1D bit[6] is written from 1 to 0 (charge enable)
- Reg1B bit [3] is written from 0 to 1 (safety timer enable)
- Reg1D bit [0] is written from 0 to 1 (software reset)

Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, all registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are programmable. If the watchdog timer (Reg1C bit [2:1]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the Reg5A bit [0] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode, and the SYS will be pull down to GND by 2s, at this time, Reg31 bit[7]=1, then the next watchdog time cycle will be started automatically. If the watchdog timer has not been reset all the time, the SYS reset pulses will be generated all the time.

The watchdog timer limit can also be programmed or disabled by Reg1C bit[2:1]. When there is VIN, the default state of the watchdog timer is on, and the value is set as 160s. When there is no VIN, the default state of the watchdog timer is suspended. (Figure 6) Also, if the Reg1C bit[0] set to 1, then watchdog timer can also work when there is only Battery and no VIN, at this time, if watchdog timer expires, the SYS will be reset by 2s only once.

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no VIN
- Register reset Reg1D bit [0] is reset

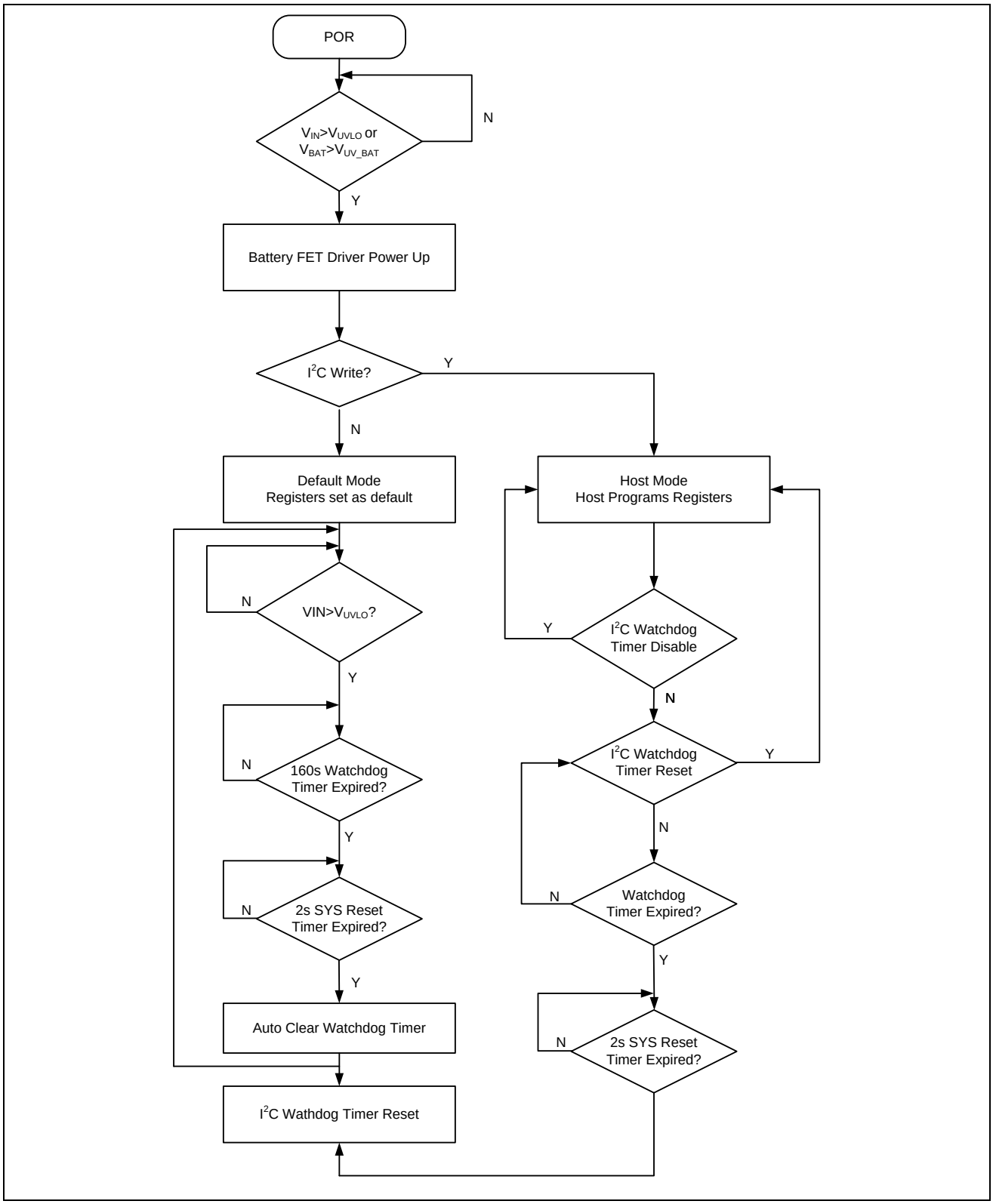


Figure 6. Default mode and Host mode Selection

Battery Discharge Function

If battery is connected and the input source is missing, the battery MOSFET is fully on when VBAT is above the V_{UV_BAT} threshold. The 100mΩ battery MOSFET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 13μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once I_{BAT} exceeds the programmable discharge current limit (default 2A), the battery MOSFET is turned off after a 60us delay, and the ET9563 enters hiccup mode in over-current protection. The discharge current can be programmed high to 3.2A through the I^2C.If the discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery MOSFET is turned off and starts hiccup mode immediately. The interval of the hiccup mode is 800μs.

Similarly, when the battery voltage falls below the programmable V_{UV_BAT} threshold (default 2.8V), the battery MOSFET is turned off to prevent over-discharge.

System Short-Circuit Protection (SCP)

The ET9563 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BAT to SYS path.

The system voltage is continuously monitored. If V_{SYS} is lower than 1.5V, the system (SCP) for the IN to SYS path and the BAT to SYS path are active. I_{BATOC} is decreased to half of the original value.

1) IN to SYS path: Once I_{IN} is over the 360mA protection threshold, both the LDO MOSFET and the BAT MOSFET are turned off immediately, and the IC enters hiccup mode. Otherwise, the max current limit (360mA) are not reached and the setting input current limit are reached, and I_{IN} is regulated at IN_ILMTI_SET. Hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800μs.

2) BAT to SYS path: Once I_{BAT} is over the 3.7A protection threshold, both the LDO MOSFET and the BAT MOSFET are turned off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The interval of the hiccup mode is 800μs.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation. (Figure 7)

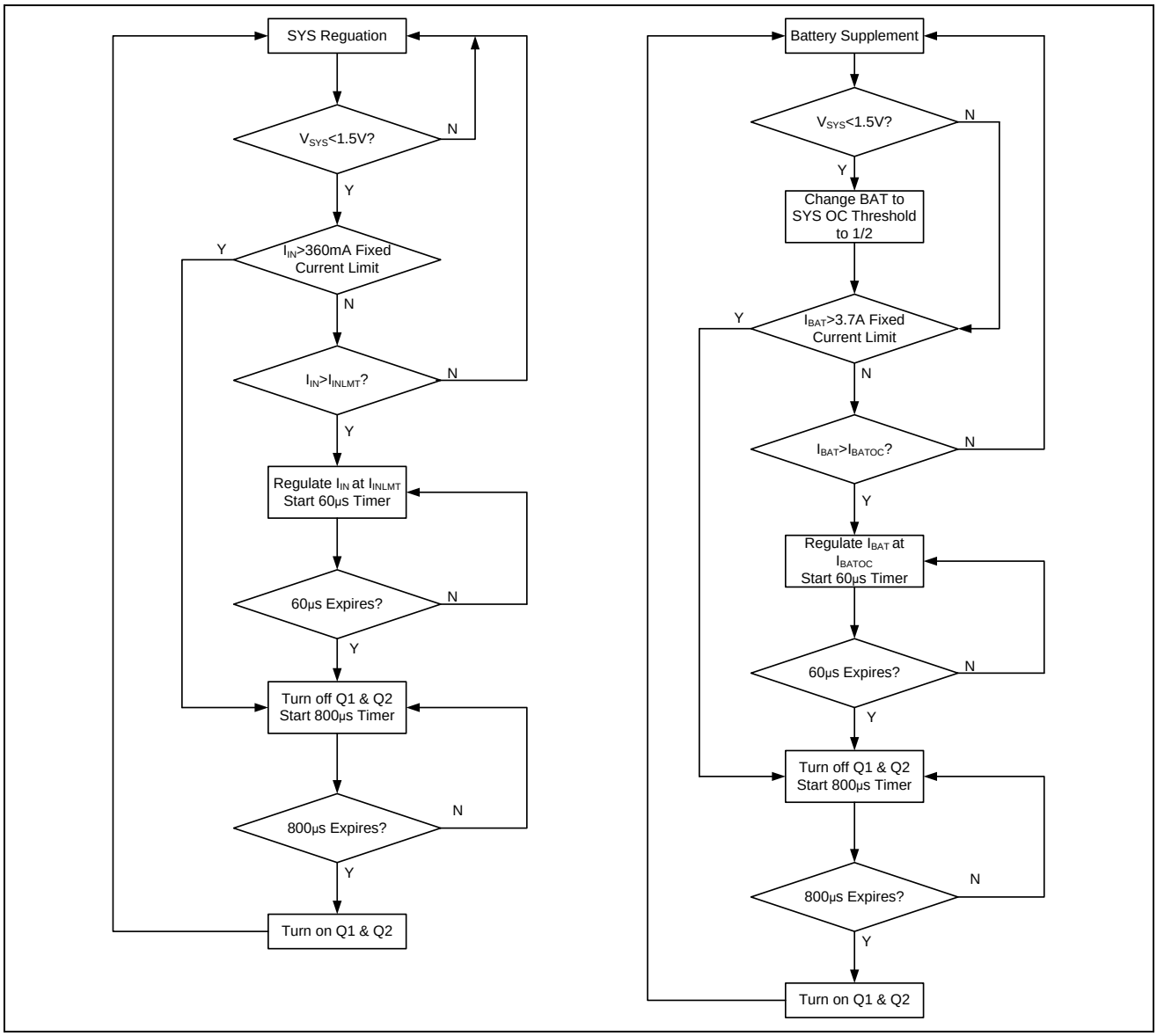


Figure 7. System Short-Circuit Protection

Interrupt to Host (INT)

The IC has an alert mechanism which can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of below events can trigger the INT output:

- Input Good Source detected
- UVLO or OVP for IN Port
- Charge Completed
- Incoming and outgoing box detection

INT state register can be read through Reg40、Reg41、Reg42H、Reg43H、Reg44H.

When any fault occurs, the IC sends out an INT pulse and latches the fault state in Reg40H, Reg41H, Reg42H, Reg43H, Reg44H.

The NTC fault is not latched and always reports the current thermistor conditions.

If we set Reg1B[7]=0, the INT interrupt output will be closed. The reset and wake up function of INT still work. The corresponding interrupt can be closed separately by Reg50H、Reg51H、Reg52H、Reg53H、Reg54H.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system:

Case A: to prevent excessive capacity discharge during the device is in shipping or storage.
Case B: allow the system power reset

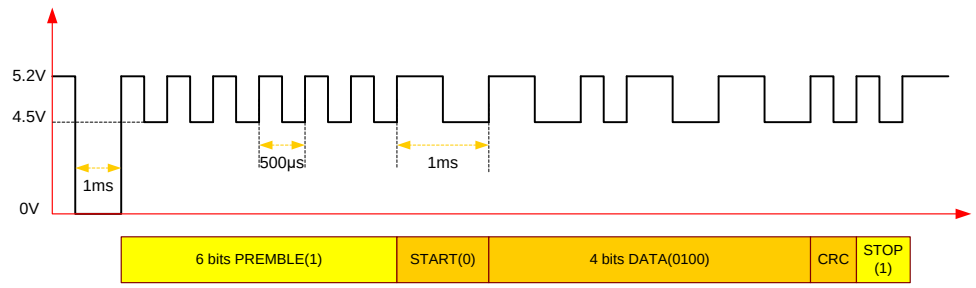
The ET9563 provides both shipping mode and system reset mode for different application requirements.

1). Shipping Mode:

Entering the Shipping mode:

1) Enter the shipping mode by setting the register bit (EN_SHIPPING_MODE), Reg1D bit[4].
During the normal operation, the battery MOSFET is turned on and this bit is 0. If this bit is set to 1 through I^2C, the battery MOSFET is turned off, and the ET9563 enters shipping mode after a delay time, the delay time can be set by Reg1A bit[4:3] (SHIPMODE_ENTER_TIME), the default time is 1s.
When VIN is in place, we enter the shipping mode, the SYS will not be closed, and the chip will enter the shipping mode after the VIN removed.

2) Enter the shipping mode by decoding the code of VIN voltage (Serial Communication of VIN).
When VIN receives the following wave, the value of Reg22(COMT_RX) is 04H, then Reg43[1]=1 (RCV_SD_INT), this bit will start the shipping mode enter timer (SHIPMODE_ENTER_TIME), before the shipping mode enter timer expires, the register RCV_SD_INT(REG43[1]) is reset, ET9563 will stop entering shipping mode.



SHIPMODE waveform from VIN (0→1ms, 1→500µs)

Exiting shipping mode: The IC can exit the shipping mode by pulling INT down or a valid VIN power on.

1) When the IC is in the shipping mode and only the Battery is present, pulling INT down by pushing KEY1 (see the "TYPICAL APPLICATION CIRCUIT") to make INT keep low with 100ms/2s, could wake the ET9563 up from shipping mode. After exiting shipping mode, the EN_SHIPPING_MODE will be reset to 0. (refer to table 2 and figure 8)

	INT Signal	IC Exists the Shipping Mode
Case1($T_{INT\_EX\_SHIPP\ ING\_DEL}$=0),	One negedge of INT and	At Once

Reg1B Bit6	INT Keep Low level>2s	
Case2($T_{INT\_EX\_SHIPP\ ING\_DEL}$=1), Reg1B Bit6	One negedge of INT and INT Keep Low level >100ms	At Once

Table 2. Exit Shipping mode with BAT present only

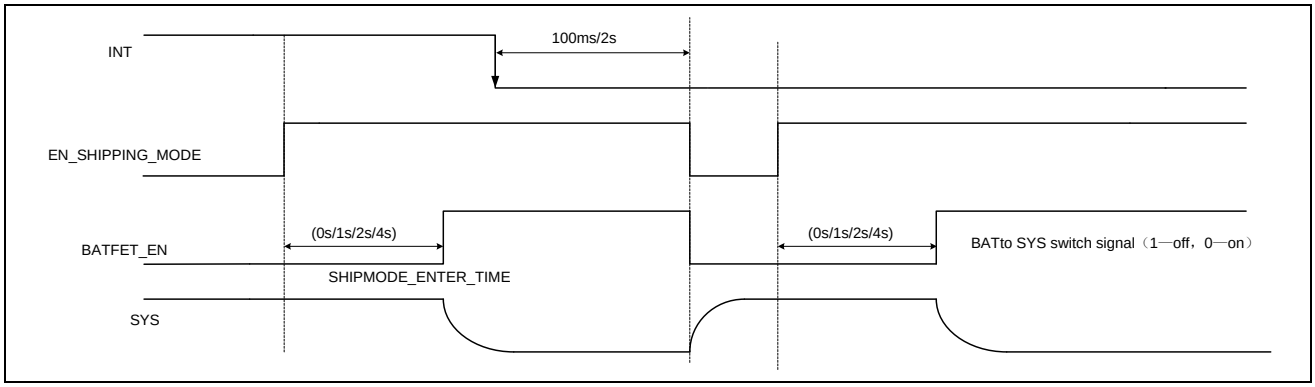


Figure 8. Enter Shipping Mode and Exit Shipping Mode by INT Low Level

2) When the IC is in the shipping mode and VIN connects to a valid power supply, the ET9563 could be woken up after 120ms. (refer to Table 3 and Figure 9).

VIN voltage effective condition：

V_{IN}>V_{IN_UVP} and V_{IN}<V_{IN_OVP}

IN Signal(Power Good Signal)	IC Exists the Shipping Mode
One posedge of IN Power Good and Keep Power Good Signal>120ms	At Once

Table 3. Exit Shipping mode with VIN powers on

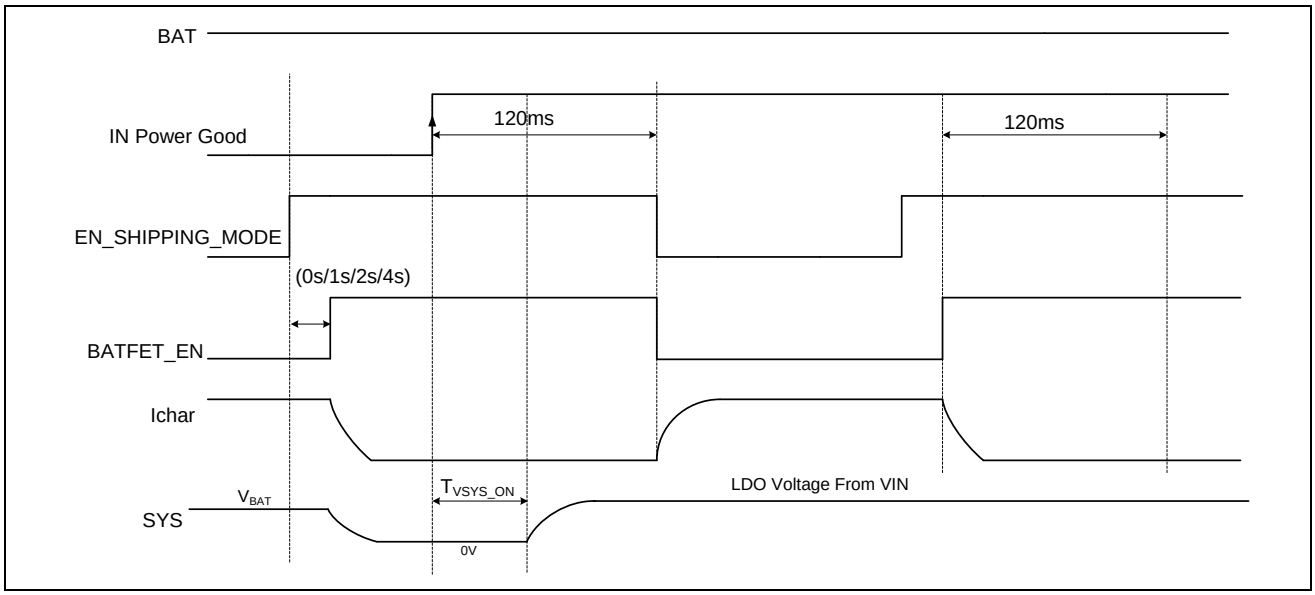


Figure 9. Enter Shipping Mode and Exit Shipping Mode by VIN Good Signal

In Figure 9, T_{VSYS_ON} (SYS voltage output time when ET9563 enter shipping mode with VIN is present) has following conditions:

- Reg31[5:4](PLUAG_STAT[1:0])=11(In box state),VIN is present, when T_{VSYS_ON}=250μs, SYS will have an output.

- Reg31[5:4](PLUAG_STAT[1:0])=00/01/10(other states),VIN is present, if communication is finished, received ACK,SYS will have an output, T_{VSYS_ON} = 20ms.
- Reg31[5:4](PLUAG_STAT[1:0])=00/01/10(other states),VIN is present, if communication isn't finished, received NO ACK,SYS will have an output, T_{VSYS_ON} = 60ms。

3) In shipping mode, EN_SHIPPING_MODE keeps high level, ET9563 can exit shipping mode by setting Reg1D[0] = 1(REG_RST), then EN_SHIPPING_MODE reset to 0.

4) If reset the EN_SHIPPING_MODE during the shipping delay time (SHIPMODE_ENTER_TIME), ET9563 will stop entering shipping mode.

5) If VIN is present, ET9563 is in shipping mode, ET9563 can exit shipping mode by reset EN_SHIPPING_MODE.

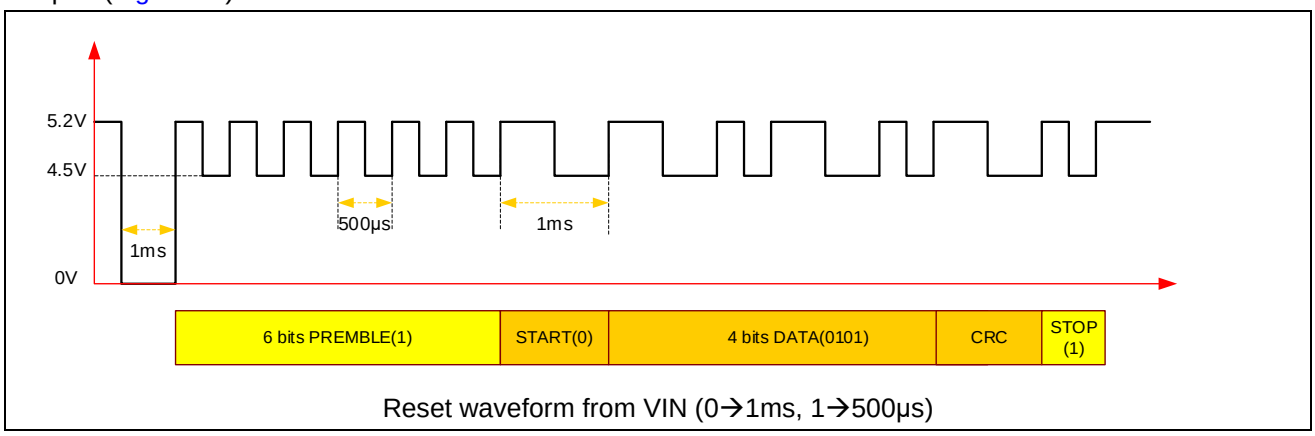
2). Reset Mode(SYS pull down to GND for a period of time)

When the system needs to be reset, ET9563 provides three methods to reset system:

1) Once the logic at INT is set to low for more than 6s/12s/16s/20s (T_{RST_DEL},Reg1A[2:1]), the SYS is disconnected from the system by turning off the LDO MOSFET and the BAT MOSFET. At the same time SYS will be discharged by internal discharge circuit, the reset time is 2s/4s (Reg1A[0]), then the LDO MOSFET and the BAT MOSFET will work again, SYS will have an output. (Figure 10)

2) When watchdog time is overflow, the SYS is disconnected from the system by turning off the LDO MOSFET and the BAT MOSFET, SYS will pull down to GND for 2s, then the LDO MOSFET and the BAT MOSFET will work again, SYS will have an output. If ET9563 is in charge watchdog, the watchdog timer has not been reset all the time, the SYS reset pulses will be generated all the time. If ET9563 is in discharge watchdog, the SYS reset pulses will be generated only once.

3) When VIN receives voltage data Reg22[3:0]=0x05 (COMT_RX) by serial communication, see following wave, ET9563 will start the delay timer. The timer can be set by REBOOT_ENTER_TIME, Reg1A[7:6] (0s/1s/2s/4s). When the timer expires, ET9563 will turn off the LDO MOSFET and the BAT MOSFET, SYS will pull down to GND for 2s, then the LDO MOSFET and the BAT MOSFET will work again, SYS will have an output. (Figure 10)



Reset waveform from VIN (0→1ms, 1→500µs)

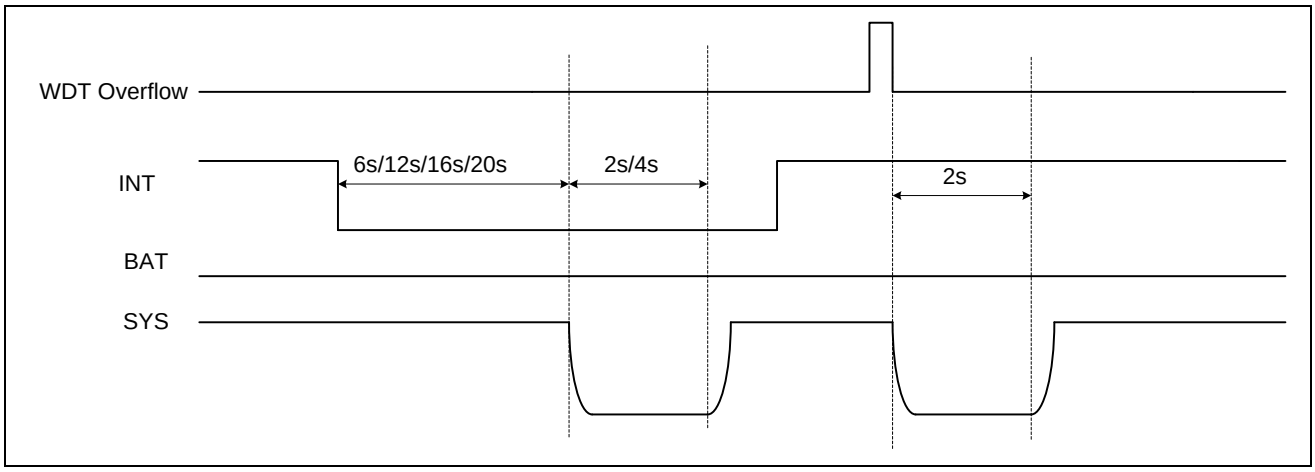


Figure 10. System Reset Function Operation Profile

Turn on Communication Channel Between UART and VIN

1) Force on

(1) $V_{IN} < V_{UVLO}$

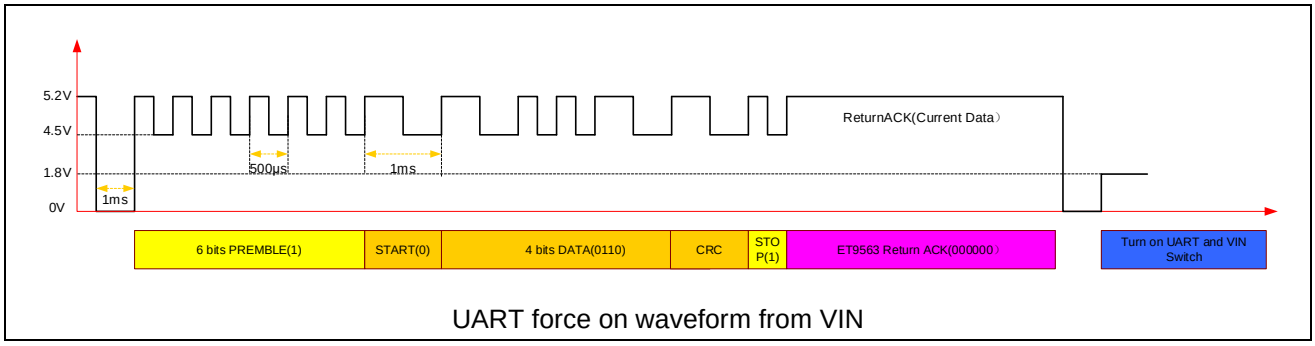
(2) Set Reg20[7] = 1（FORCE_UART_ON）

When the condition (1) is satisfied, operation (2) can immediately open the path from VIN to UART, otherwise, it will not be opened.

2) VIN receives voltage data by serial communication

(1) VIN receives 06H data by serial communication (See following figure), and reply ACK to Buck-Boost (ET9580) through VIN pin.

(2) After receiving the 06H data and reply ACK, ET9563 waits for the VIN waveform to jump back from 0V to 1.8V. If this change occurs, the VIN to UART path will be automatically opened, and vice versa.



UART force on waveform from VIN

Turn off Communication Channel Between UART and VIN

1) Force off, set Reg20[6]=1(FORCE_UART_OFF).

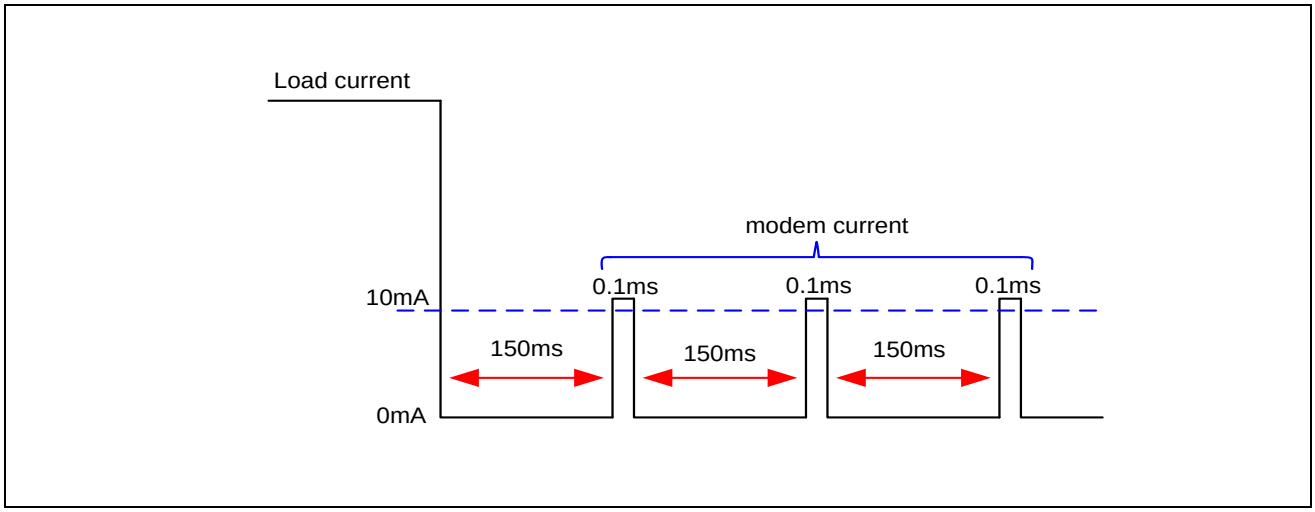
2) Make $V_{IN} > V_{UVLO}$, the VIN to UART path will be automatically closed.

Heart Beat Mode

The heartbeat mode periodically generates a fixed pulse current at the VIN pin, in order to provide detection conditions for the box to determine whether the earphone is in the box. The start conditions are as follows:

(1) enable Reg1C[6]（EN_HB）
(2) VIN is not in serial communication mode
(3) The current from VIN to SYS is smaller than 15mA (including VIN to SYS off)

The pulse current waveform in Heart Beat Mode as follows:

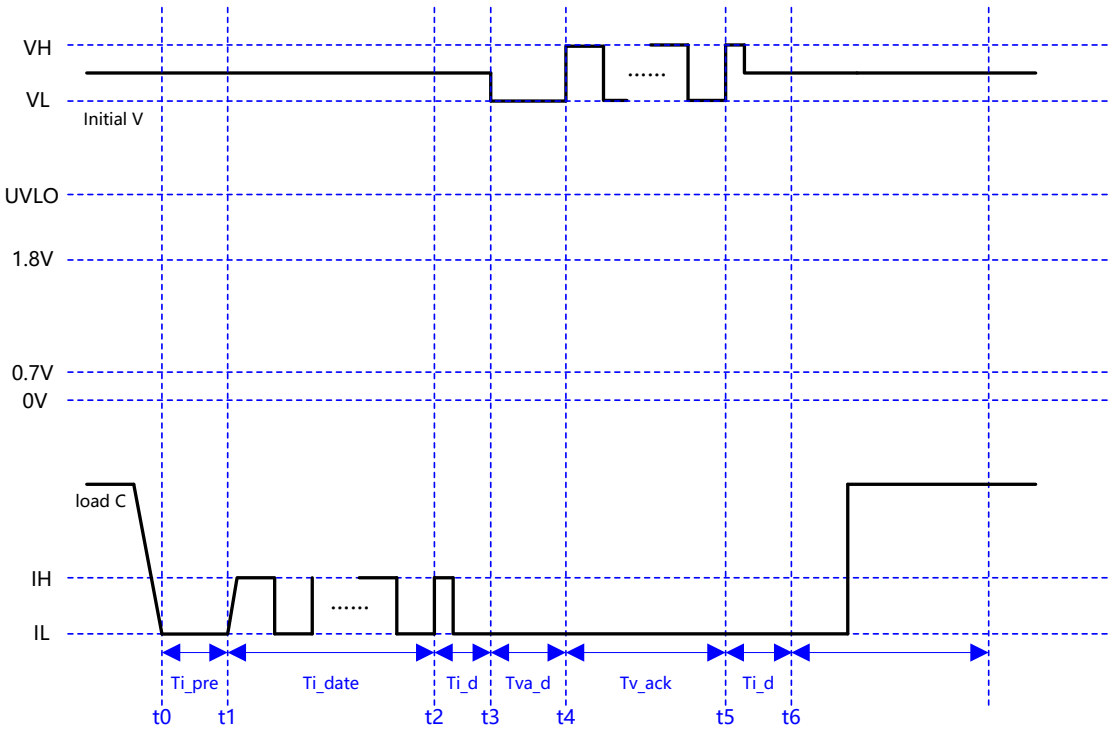


Earphone in/out Auto-detection

1). Earphone in Auto-detection

When ET9563's VIN pin is powered on, VIN pin will send a handshake data. When BAT voltage lower than V_{BAT_LOW} (Reg1C[4:3]),VIN will send data 05H. When BAT voltage higher than V_{BAT_LOW} (Reg1C[4:3]), VIN will send data 04H. If VIN receives ACK, ET9563 will set Reg31[5:4] = 11 (PULG_STAT, In Box state). If no response is received after three times, the status flag Reg31 [5:4] (PULG_STAT) will be automatically set to 10 (illegal power supply)

ET9653 can operate the Reg21 register through I^2C, and can send any data. As long as it receives an ACK response, it will immediately set the box in flag Reg31[5:4] = 11 (PULG_STAT). If an ACK is not received, it will be repeated twice every 10ms. If no response is received after three times, the status flag Reg31[5:4] (PULG_STAT) will be automatically set to 10 (illegal power supply)



Earphone in auto-detection waveform

Timing - Time Specification

Symbol	Min	Typ	Max	Unit	Note
Ipre			1	mA	
IH	8	10	12	mA	Voltage High Level
IL			1	mA	Voltage Low Level
Ti_transition			100	μs	VH to VL;VL to VH;
Ti_pre	0.7	1	1.3	ms	Pretreatment time
Tva	0.4	0.5	0.6	ms	Reply ACK preprocessing time
Ti_data“1”	0.4	0.5	0.6	ms	
Ti_data“0”	0.8	1	1.2	ms	
Ti_d			150	μs	Demodulated current signal response time

2). Earphone in Auto-detection

Earphone out auto-detection condition:

(1) Enable earphone out auto-detection, set Reg1C[5]=1 (EN_ONLINE_DET)

(2) V_{IN} < 0.7V, keep 50ms

(3) When the condition (2) is just satisfied, ET9563 will automatically send a 2mA current with 32μs width pulse at the VIN pin to detect the VIN voltage. When the VIN voltage is detected to be less than 1.5V, the state register Reg31[5:4] (PULG_STAT) will be set to 01 (abnormal in box). When the VIN voltage is detected to be higher than 1.5V, the state register Reg31[5:4] (PULG_STAT) will be set to 00 (Out of Box).

In addition, after an automatic detection in (3), the function of periodically sending 2mA current pulses at the VIN pin can also be activated through I^2C. The activation condition is to set Reg1B[4] =1 (EN_RC). When the enable sends a 2mA current with 32μs width pulse once, if an abnormality in the box (PULG_STAT=01) is detected, the bit will not be cleared. After every 100ms, a 2mA current with 32μs width pulse will continue to be sent, and the out of box and abnormal in box detection will be performed again, until the out of box state is detected (PULG_STAT=00), this bit will automatically reset and periodic detection will stop. This bit can be activated repeatedly.

If the VIN pin periodically sends a 2mA current pulse function through the operation register in the out of box state, when the out of box state is detected again, the periodic transmission will not be started, and Reg1B [4] (EN_RC) will not be cleared. If it is necessary to detect again, it needs to be cleared and reset.

I²C REGISTER MAP

Chip Address: 0000110b (7bit) = 06H

Product ID/Address: 00H (Default: 90H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	PROD_ID [7]	Product ID	NA	NA	Read Only	10010000b
Bit 6	PROD_ID [6]		NA	NA		
Bit 5	PROD_ID [5]		NA	NA		
Bit 4	PROD_ID [4]		NA	NA		
Bit 3	PROD_ID [3]		NA	NA		
Bit 2	PROD_ID [2]		NA	NA		
Bit 1	PROD_ID [1]		NA	NA		
Bit 0	PROD_ID [0]		NA	NA		

Device ID/Address: 01H (Default: 0EH)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	DEV_ID [7]	Device ID	NA	NA	Read Only	00001110b
Bit 6	DEV_ID [6]		NA	NA		
Bit 5	DEV_ID [5]		NA	NA		
Bit 4	DEV_ID [4]		NA	NA		
Bit 3	DEV_ID [3]		NA	NA		
Bit 2	DEV_ID [2]		NA	NA		
Bit 1	DEV_ID [1]		NA	NA		
Bit 0	DEV_ID [0]		NA	NA		

I²C Address/Address: 02H (Default: C0H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	I²C_ADDR[2]	000b:00H 001b: 01H 010b: 02H 011b: 03H 100b: 04H 101b: 05H 110b: 06H 111b: 07H	NA	NA	Read only	Default:110(06H) ET9563
Bit 6	I²C_ADDR[1]		NA	NA		
Bit 5	I²C_ADDR[0]		NA	NA		
Bit 4	Reserved		NA	NA	Read only	0
Bit 3	Reserved		NA	NA	Read only	0
Bit 2	Reserved		NA	NA	Read only	0
Bit 1	Reserved		NA	NA	Read only	0
Bit 0	Reserved		NA	NA	Read only	0

Input Source Control Register/Address:10H (Default: 9FH)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Input Voltage Regulation (V_{IN_REG})						
Bit 7	IN_VSET[3]	1b: 640mV	Y	N	Read/write	Offset: 3.88V Range:3.88V-5.08V Default:4.60V(1001b)
Bit 6	IN_VSET[2]	1b: 320mV	Y	N		
Bit 5	IN_VSET [1]	1b: 160mV	Y	N		
Bit 4	IN_VSET [0]	1b: 80mV	Y	N		
Input Current Limit (I_{IN_LIM})						
Bit 3	IN_ILIMT[3]	1b: 240mA	Y	N	Read/write	Offset: 50mA Range: 50mA-500mA Default:500mA(1111b)
Bit 2	IN_ILIMT[2]	1b: 120mA	Y	N		
Bit 1	IN_ILIMT[1]	1b: 60mA	Y	N		
Bit 0	IN_ILIMT[0]	1b: 30mA	Y	N		

Termination Current/Pre_Charge Current/Address: 11H (Default: 22H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Termination Current (I_{TERM})						
Bit 7	EOC_CHAR_ISET[3]	1b: 8mA	Y	Y	Read/write	Offset: 1mA Range: 1mA-16mA Default: 3mA (0010b)
Bit 6	EOC_CHAR_ISET[2]	1b: 4mA	Y	Y		
Bit 5	EOC_CHAR_ISET[1]	1b: 2mA	Y	Y		
Bit 4	EOC_CHAR_ISET[0]	1b: 1mA	Y	Y		
Pre_Charge Current (I_{PRE})						
Bit 3	PRE_CHAR_ISET[3]	1b: 8mA	Y	Y	Read/write	Offset: 1mA Range: 1mA-16mA Default: 3mA (0010b)
Bit 2	PRE_CHAR_ISET[2]	1b: 4mA	Y	Y		
Bit 1	PRE_CHAR_ISET[1]	1b: 2mA	Y	Y		
Bit 0	PRE_CHAR_ISET[0]	1b: 1mA	Y	Y		

Charge Current Control Register/Address: 12H (Default: 40H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
CC Charge Current Setting						
Bit 7	CHAR_ISET [7]	1b: 256mA	Y	Y	Read/write	Offset: 0mA Range: 2mA -510mA Default:128mA (01000000b) 00000000b=2mA 00000001b=2mA
Bit 6	CHAR_ISET [6]	1b: 128mA	Y	Y		
Bit 5	CHAR_ISET [5]	1b: 64mA	Y	Y		
Bit 4	CHAR_ISET [4]	1b: 32mA	Y	Y		
Bit 3	CHAR_ISET [3]	1b: 16mA	Y	Y		
Bit 2	CHAR_ISET [2]	1b: 8mA	Y	Y		
Bit 1	CHAR_ISET [1]	1b: 4mA	Y	Y		
Bit 0	CHAR_ISET [0]	1b: 2mA	Y	Y		

Charge Voltage Control Register/Address: 13H (Default: D2H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Pre_Charge Threshold						
Bit 7	PRE_CHAR_VSET	0b: 2.8V 1b: 3.0V	Y	Y	Read/write	3.0V (1b)
Battery Regulation Voltage						
Bit 6	BATREG_VSET[6]	1b: 467.2mV	Y	Y	Read/write	Offset: 3.60V Range: 3.60V~4.5271V Default: 4.2V (1010010b) Clamp to 4.5271V
Bit 5	BATREG_VSET[5]	1b: 233.6mV	Y	Y		
Bit 4	BATREG_VSET[4]	1b: 116.8mV	Y	Y		
Bit 3	BATREG_VSET[3]	1b: 58.4mV	Y	Y		
Bit 2	BATREG_VSET[2]	1b: 29.2mV	Y	Y		
Bit 1	BATREG_VSET[1]	1b: 14.6mV	Y	Y		
Bit 0	BATREG_VSET[0]	1b: 7.3mV	Y	Y		

Charge Configuration/Address: 14H (Default:84H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Battery Recharge Threshold (below BATREG_VSET)						
Bit 7	BAT_RCHAR_VSET	0b: 100mV 1b: 200mV	Y	Y	Read/write	200mV (1b)
Top Off Time (T_{TOP_OFF})						
Bit 6	TOP_OFF_TIME [3]	1b: 40min	Y	Y	Read/write	Offset:0min(disable) Range: 0min-75min Default:0min(0000b)
Bit 5	TOP_OFF_TIME [2]	1b: 20min	Y	Y		
Bit 4	TOP_OFF_TIME [1]	1b: 10min	Y	Y		
Bit 3	TOP_OFF_TIME [0]	1b: 5min	Y	Y		
Battery UVLO Threshold						
Bit 2	BAT_UVLO_SET[2]	1b: 360mV	Y	Y	Read/write	Offset: 2.4V Range: 2.4V-3.03V Default:2.76V (100b)
Bit 1	BAT_UVLO_SET[1]	1b: 180mV	Y	Y		
Bit 0	BAT_UVLO_SET[0]	1b: 90mV	Y	Y		

SYS Voltage/Discharge Current Limit/Address: 15H (Default: 89H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
System Output Voltage Regulation (V_{SYS_REG})						
Bit 7	SYS_VSET[3]	1b: 400mV	Y	N	Read/write	Offset: 4.2V Range: 4.2V-4.95V Default: 4.6V (1000b)
Bit 6	SYS_VSET[2]	1b: 200mV	Y	N		
Bit 5	SYS_VSET[1]	1b: 100mV	Y	N		
Bit 4	SYS_VSET[0]	1b: 50mV	Y	N		
BAT to SYS Discharge Current Limit (I_{DISCHG}) ***Note:*** Should not Exceed Max P_D to Use						
Bit 3	BATTOSYS_ISET [3]	1b:1600mA	Y	Y	Read/write	Offset: 200mA Range:400mA~3.2A Valid range: 0001b ~1111b 0000b=0001b=400mA Default: 2A (1001b)
Bit 2	BATTOSYS_ISET [2]	1b: 800mA	Y	Y		
Bit 1	BATTOSYS_ISET [1]	1b: 400mA	Y	Y		
Bit 0	BATTOSYS_ISET [0]	1b: 200mA	Y	Y		

Reserved Register/Address: 16H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Reserved		NA	NA	Read only	0
Bit 6	Reserved		NA	NA	Read only	0
Bit 5	Reserved		NA	NA	Read only	0
Bit 4	Reserved		NA	NA	Read only	0
Bit 3	Reserved		NA	NA	Read only	0
Bit 2	Reserved		NA	NA	Read only	0
Bit 1	Reserved		NA	NA	Read only	0
Bit 0	Reserved		NA	NA	Read only	0

Termination Setting/UCP/Address: 17H (Default: 9FH)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	EN_TERM	0b: Disable 1b: Enable	Y	Y	Read/write	Termination setting Enabled (1b)
TERM_TMR: When TERM_TMR is enabled, the IC will not suspend the charge current after the charge termination						
Bit 6	TERM_TMR	0b: Disable 1b: Enable	Y	Y	Read/write	Termination timer control. Disable (0b)
UCP						
Bit 5	UCP[5]	480mA	Y	Y	Read/write	Offset: 30mA Range: 30mA - 600mA Default: 495mA (011111b)
Bit 4	UCP[4]	240mA	Y	Y		
Bit 3	UCP[3]	120mA	Y	Y		
Bit 2	UCP[2]	60mA	Y	Y		
Bit 1	UCP[1]	30mA	Y	Y		
Bit 0	UCP [0]	15mA	Y	Y		

Thermal/NTC Configuration Register/Address: 18H (Default: F2H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Thermal Configuration						
Bit 7	EN_THERMAL	0b: Disable 1b: Enable	Y	Y	Read/write	Enable Thermal loop Enabled (1b)
Bit 6	T_{JEG}[1]	00b: 60°C 01b: 80°C 10b: 100°C 11b: 120°C	Y	Y	Read/write	120°C (11b)
Bit 5	T_{JEG}[0]		Y	Y		
NTC Configuration						
Bit 4	NTC_EN	0b: Disable 1b: Enable	Y	Y	Read/write	Enable (1b)
Bit 3	PCB_OTP_EN	0b: Enable 1b: Disable	Y	Y	Read/write	Enable (0b)
Bit 2	D_{NTC}[1]	00b: 0.05% 01b: 5% 10b: 10% 11b: 100%	Y	Y	Read/write	The Time period is 5s (0.2Hz) Default: 5% (01b)
Bit 1	D_{NTC}[0]		Y	Y		
Bit 0	Reserved		NA	NA	Read only	Default: 0b

JEITA Configuration Register/Address: 19H (Default: B5H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
CC current setting during T2(Cool) temperature range, as percentage of ICC						
Bit 7	JEITA_T2_ISET[1]	00b : No Charge 01b : 20% of ICC 10b: 50% of ICC 11b: 100% of ICC	Y	Y	Read/write	Default:50% of ICC in NTC COOL (10b)
Bit 6	JEITA_T2_ISET[0]		Y	Y		
CV charge voltage setting during T3(warm) temperature range.						
Bit 5	JEITA_T3_VSET[1]	00b: No Charge 01b: V_{BAT_REG} 10b: V_{BAT_REG} -50mV 11b: V_{BAT_REG} -100mV	Y	Y	Read/write	Default: VBAT_REG-100mV in NTC WARM (11b)
Bit 4	JEITA_T3_VSET[0]		Y	Y		
T2(Cool) temperature						
Bit 3	JEITA_T2_TEMP[1]	00b: 1.145V(5°C) 01b: 0.921V (10°C) 10b: 0.746V (15°C) 11b: 0.609V (20°C)	Y	Y	Read/write	Default:10°C (01b)
Bit 2	JEITA_T2_TEMP[0]		Y	Y		
T3(warm) temperature						
Bit 1	JEITA_T3_TEMP[1]	00b: 0.288V (40°C) 01b: 0.242V (45°C) 10b : 0.205V (50°C) 11b: 0.174V (55°C)	Y	Y	Read/write	Default:45°C (01b)
Bit 0	JEITA_T3_TEMP[0]		Y	Y		

SYS Control_1 Register/Address: 1AH (Default: 0CH)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	T_{REBOOT_DLY}[1]	00b: 0s 01b: 1s 10b: 2s 11b: 4s	Y	Y	Read/write	Enter Reboot mode deglitch time Default: 0s (00b)
Bit 6	T_{REBOOT_DLY}[0]		Y	Y	Read/write	
Bit 5	Reserved		Y	Y	Read/write	
Bit 4	$T_{SHIPPING\_DLY}$[1]	00b: 0s 01b: 1s 10b: 2s 11b: 4s	Y	N	Read/write	Enter shipping mode deglitch time Default: 1s (01b)
Bit 3	$T_{SHIPPING\_DLY}$[0]		Y	N	Read/write	
Bit 2	T_{RST_DEL}[1]	00b: 6s 01b: 12s 10b: 16s 11b: 20s	Y	Y	Read/write	Pull INT low to reset system. Default: 16s (10b)
Bit 1	T_{RST_DEL}[0]		Y	Y		
Bit 0	T_{RST_DUR}	0b: 2s 1b: 4s	Y	Y	Read/write	VSYS Keep Low Level Time during system reset. Default: 2s (0b)

SYS Control_2 Register/Address: 1BH (Default: ABH)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
EN_INT_PULSE: Do not affect INT existing shipping mode and system reset function.						
Bit 7	EN_INT_PULSE	0b: Disable 1b: Enable	Y	Y	Read/write	Default: enable (1)
$T_{INT\_EX\_SHIPPING\_DEL}$: INT Port Low Level Time Setting for Exit Shipmode						
Bit 6	$T_{INT\_EX\_SHIPPING\_DEL}$	0b: 2s 1b: 100ms	Y	Y	Read/write	Default: 2s (0)
Bit 5	EN_BATOCP	0b: Disable 1b: Enable	Y	N	Read/write	Default: enable (1)
EN_RC: Period detection for reserve current online detection (ONLY WORKS IN VIN < 0.7V and keep 50ms) RCD detection periodically (100ms): (1) EN_RC is not enabled, an out-of-box RCD detection will occur. (2) EN_ After RC is enabled, during the first automatic RCD out of box detection, an abnormal power down in box state is detected, and then the RCD detection is performed at a 100ms cycle. If the abnormal power down in box state persists, the 100ms cycle detection is continued; If not, exit the abnormal power down detection in the box for a 100ms cycle and clear the EN_ RC。 (3) EN_RC is enabled, if the box out state is found during the first automatic RCD box out detection, cycle detection will not be started,EN_RC will not automatically be cleared.						
Bit 4	EN_RC	0b: Disable 1b: Enable	Y	Y	Read/write	Default: disable (0)
Bit 3	EN_TIMER	0b:Disable 1b:Enable	Y	Y	Read/write	Safety timer setting. Default: Enable timer (1)
Bit 2	T_{CHG}[1]	00b: 3hrs 01b: 5hrs 10b: 8hrs 11b: 12hrs	Y	Y	Read/write	CC charge safety timer Default: 5hrs(01b)
Bit 1	T_{CHG}[0]		Y	Y		
EN_TMR_2X: 2X extended safety timer during PPM and thermal regulation						
Bit 0	EN_TMR_2X	0b:Disable 1b:Enable	Y	Y	Read/write	Default: enable (1b)

SYS Control_3 Register/Address: 1CH (Default: F6H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
EN_LOOP_INT : Enable loop interrupt when interrupt status is not cleared						
Bit 7	EN_LOOP_INT	0b: Disable 1b: Enable	Y	Y	Read/write	Default: Enable (1b)
Bit 6	EN_HB	0b: Disable 1b: Enable	Y	Y	Read/write	Default: Enable Heartbeat (1b)
Bit 5	EN_ONLINE_DET	0b: Disable 1b: Enable	Y	Y	Read/write	Default: Enable Online Det (1b)
V_{BAT_LOW}: Only works for communication battery voltage						
Bit 4	V_{BAT_LOW}[1]	00: 3.2V; 01: 3.3V; 10: 3.4V; 11: 3.5V	Y	Y	Read/write	Default:3.4V (10b)
Bit 3	V_{BAT_LOW}[0]		Y	Y	Read/write	
T_{WD}: disable watchdog works for both charging and discharge						
Bit 2	T_{WD}[1]	00: Disable 01: 40s 10: 80s 11: 160s	Y	N	Read/write	Default: 160s (11b)
Bit 1	T_{WD}[0]		Y	N		
EN_WD_DISCHG : Enable watchdog control in discharge mode.						
Bit 0	EN_WD_DISCHG	0b:Disable 1b:Enable	Y	N	Read/write	Default: Disable (0)

Enable & Reset Register/Address: 1DH (Default: 42H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	EN_HIZ	0b: Disable 1b: Enable	Y	Y	Read/write	Default: Disable (0b)
Bit 6	CEB	0b: Enable 1b: Disable	Y	Y	Read/write	Default: Charge Disable(1b)
Bit 5	EN_DRC	0b: Disable 1b: Enable	Y	Y	Read/write	Control the Direct mode Default: Disable (0b)
Bit 4	EN_SHIPPING_MODE	0b: Enable 1b: Turn off	Y	N	Read/write	Default: Enable (0b) (BATFET ON)
Bit 3	C_Q1_2X_EN	0b: Disable 1b: Enable	Y	Y	Read/write	Both offset and step double Default: Disable (0b)
Bit 2	C_BATFET_2X_EN	0b: Disable 1b: Enable	Y	Y	Read/write	Both offset and step double Default: Disable (0b)
Bit 1	VIN_DPM_EN	0b: Disable 1b: Enable	Y	Y	Read/write	Default: Enable (1)
Bit 0	REG_RST	0: Keep current setting 1: Reset (then reset to 0)	Y	N	Read/write	Default: Keep current setting(0b)

UART Register/Address: 20H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	FORCE_UART_ON	0: Not turn on UART 1:Turn on the UART (then reset to 0)	Y	Y	Read/write	Force on UART channel if VIN<UVLO. Default: Disable (0b)
Bit 6	FORCE_UART_OFF	0: Not turn off UART 1: Turn off the UART (then reset to 0)	Y	Y	Read/write	Force off UART channel. Default: Disable (0b)
Bit 5	Reserved		NA	NA	Read only	Default: 000000b
Bit 4	Reserved		NA	NA	Read only	
Bit 3	Reserved		NA	NA	Read only	
Bit 2	Reserved		NA	NA	Read only	
Bit 1	Reserved		NA	NA	Read only	
Bit 0	Reserved		NA	NA	Read only	

COMM_TX Register/Address: 21H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Reserved		NA	NA	Read only	Default: 0000b
Bit 6	Reserved		NA	NA	Read only	
Bit 5	Reserved		NA	NA	Read only	
Bit 4	Reserved		NA	NA	Read only	
TX_CTRL: Communication instructions send out bit. If no ACK is required within 10ms, the instruction will be send again; After 3 times retry, this bit will be also cleared and report this communication failure event.						
Bit 3	TX_CTRL	0000b/0001b: Reserved 0100b: NORMAL PACKAGE 0101b: PRECHARGE PACKAGE 0110b: UART REQUESET PACKAGE (0010b, 0011b, 0111b-1111b: Customize PACKAGE)	Y	Y	Read/write	Default: 0000b
Bit 2			Y	Y		
Bit 1			Y	Y		
Bit 0			Y	Y		

COMM_RX Register/Address: 22H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Reserved		NA	NA	Read only	Default: 0000b
Bit 6	Reserved		NA	NA	Read only	
Bit 5	Reserved		NA	NA	Read only	
Bit 4	Reserved		NA	NA	Read only	
Bit 3	RX_STAT	0000/0001: Reserved 0100：receive SD 0101：receive reboot 0110：receive UART REQUEST 0111-1111: OTHERS 0010b,0011b,0111b-1111b: Customize PACKAGE	NA	NA	Read only	Default: 0000b
Bit 2			NA	NA		
Bit 1			NA	NA		
Bit 0			NA	NA		

STAT0 Register/Address: 30H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Reserved		NA	NA	Read only	Default: 0b
Bit 6	CHG_STAT	00b: Not charging 01b: precharge 10b:CC Charge 11b: Charge done	NA	NA	Read only	Not charging (00b)
Bit 5			NA	NA	Read only	
Bit 4	PPM_STAT	0b: No PPM 1b: In PPM	NA	NA	Read only	No PPM (0b)
Bit 3	PG_STAT	0b: Power fail 1b: Power good	NA	NA	Read only	Power good (0b)
Bit 2	THERMAL_STAT	0b: No thermal regulation 1b: In thermal regulation	NA	NA	Read only	No thermal regulation (0b)
Bit 1	DIRECT_MODE_STAT	0b: Not in direct mode 1b: In direct mode	NA	NA	Read only	Not in direct mode (0b)
Bit 0	Q1_STAT	0b: OFF 1b: ON	NA	NA	Read only	OFF (0b)

STAT1 Register/Address: 31H (Default: 0AH)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	WD_STAT	0b: Normal 1b: Watchdog timer out	NA	NA	Read only	0b: Normal
Bit 6	UART_STAT	0b: Not in UART mode 1b: In UART mode	NA	NA	Read only	0: Not in UART mode
Bit 5	PLUG_STAT	00: Earphone out of the box (requires a second handshake after re powering on) 01：The earphone is abnormally powered off and in the box (it needs to send a handshake again after being powered on again) 10：Illegal power supply (requires a handshake again after powering on): still use Linear charger to charge。 11：Normally in the box (no handshake required after re powering on)	NA	NA	Read only	00b: Out of the box (handshake required after re powering on）
Bit 4			NA	NA	Read only	
BAT_SYS_PRE: the reading value is effective when $V_{UV\_IN}<V_{IN}<V_{IN\_OVP}$; otherwise,not reflected the real value when reading.						
Bit 3	BAT_SYS_PRE	1b: VBAT lower than system pre voltage (3.2V-3.5V) 0b: VBAT higher than system pre voltage (3.2V-3.5V)	NA	NA	Read only	1b: VBAT lower than system pre voltage (3.2V-3.5V)
Bit 2	NTC_STAT	000:Cold 001:Cool 010:Normal 011:Warm 100:Hot 101:PCB OTP 111:NTC disable	NA	NA	Read only	010b: NTC normal
Bit 1			NA	NA	Read only	
Bit 0			NA	NA	Read only	

STAT2 Register/Address: 32H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	VIN OVP/UVLO	0b: VIN is good 1b: VIN is OVP/UVLO	NA	NA	Read only	0b: VIN is good
Bit 6	TSD	0: IC not in thermal shutdown 1: IC in thermal shutdown	NA	NA	Read only	0b: IC not in thermal shutdown
Bit 5	SAFETY_TIMER_OUT	0:No Safety timer out 1:Safety timer out	NA	NA	Read only	0b: No Safety timer out
Bit 4	UCP_STAT	0: $I_{BAT} > I_{UCP}$ 1: $I_{BAT} < I_{UCP}$	NA	NA	Read only	0b: $I_{BAT} > I_{UCP}$ (Only works in direct mode)
Bit 3	TOPOFF_ACTIVE	0: Top off timer not counting 1: Top off timer counting	NA	NA	Read only	0b: Top off timer not counting
Bit 2	TX_STATUS	0: Not Busy 1:Busy Is the LC in the state of busy TX serial communication transmission (including normal sending and ACK reply)	NA	NA	Read only	Default: 0b
Bit 1	CC_LOOP	0: BATFET not in CC charger mode 1: BATFET in CC loop during charger mode	NA	NA	Read only	Default: 0b
Bit 0	CV_LOOP	0: BATFET not in charger mode 1: BATFET in CV loop during charger mode	NA	NA	Read only	Default: 0b

INT0 Register/Address: 40H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	CHARGING STATUS_INT	0b: not trigger 1b: Charge state change triggered	NA	NA	RW1C	0b: not trigger
Bit 6	EOC_INT	0b: not trigger 1b: End of Charge triggered	NA	NA	RW1C	0b: not trigger
Bit 5	PPM_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 4	PG_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 3	THERMAL_STAT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 2	DRC_STAT_INT	0b: not trigger 1b: Exit Direct charge state triggered	NA	NA	RW1C	0b: not trigger
Bit 1	VINDPM_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 0	TOP_OFF_TIMER_INT	0b: not trigger 1b: Start to count the TOP OFF time triggered	NA	NA	RW1C	0b: not trigger

INT1 Register/Address: 41H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	VIN_FAULT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (OVP or UVLO)
Bit 6	THERMAL_SD_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 5	BAT_FAULT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (BAT OVP)
Bit 4	SAFETY_TIMER_ OUT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 3	NTC_FAULT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (NTC COLD/HOT, PCB OTP)
Bit 2	DRC_LIN_IBAT_CU RRENT_LIMIT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 1	DRC_UC_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 0	DRC_RCP_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (Interruption of current reversal in direct charging mode)

INT2 Register/Address: 42H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	PWR_2_COMM_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (Power path transfer to UART channel done)
Bit 6	COMM_2_PWR_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (UART transfer to power path done)
Bit 5	ILLEGAL_POWER_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 4	PLUG_OUT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 3	PLUG_IN_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 2	BAT_SYS_PRE_INT	0b: not trigger 1b: BAT voltage arrived to setting value triggered (BAT higher than system pre voltage (3.2V-3.5V))	NA	NA	RW1C	0b: not trigger
Bit 1	NTC_STAT_CHANGE_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 0	WD_FAULT_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger

INT3 Register/Address: 43H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Q1_ON_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 6	Q1_OFF_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 5	RCV_NACK_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (Do not receive a ACK) In a communication conflict scenario, the BuckBoost (ET9580) response takes precedence, and ET9563 packets are directly discarded, but NO ACK INT is reported
Bit 4	RCV_ACK_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger (Receive a ACK)
Bit 3	RCV_CUSTOMIZE_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 2	RCV_UART_REQUEST_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 1	RCV_SD_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 0	RCV_RESET_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger

INT4 Register/Address: 44H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	MIN_UCP_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 6	ABNORMAL_PLUG_IN_INT	0b: not trigger 1b: triggered	NA	NA	RW1C	0b: not trigger
Bit 5	Reserved		NA	NA	Read only	Default:0b
Bit 4	Reserved		NA	NA	Read only	Default:0b
Bit 3	Reserved		NA	NA	Read only	Default:0b
Bit 2	Reserved		NA	NA	Read only	Default:0b
Bit 1	Reserved		NA	NA	Read only	Default:0b
Bit 0	Reserved		NA	NA	Read only	Default:0b

MASK0 Register/Address: 50H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	CHARGING_STATUS_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 6	EOC_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 5	PPM_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 4	PG_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 3	THERMAL_STAT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 2	DRC_STAT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 1	VINDPM_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 0	TOP_OFF_TIMER_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse

MASK1 Register/Address: 51H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	VIN_FAULT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 6	THERMAL_SD_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 5	BAT_FAULT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 4	SAFTER_TIMER_OUT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 3	NTC_FAULT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 2	DRC_LIN_IBAT_CURRENT_LIMIT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 1	DRC_UC_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 0	DRC_RCP_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse

MASK2 Register/Address: 52H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	PWR_2_COMM_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 6	COMM_2_PWR_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 5	ILLEGAL_POWER_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 4	PLUG_OUT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 3	PLUG_IN_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 2	BAT_SYS_PRE_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 1	NTC_STAT_CHARGE_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 0	WD_FAULT_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse

MASK3 Register/Address: 53H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Q1_ON_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 6	Q1_OFF_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 5	RCV_NACK_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 4	RCV_ACK_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 3	RCV_CUSTOMIZE_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 2	RCV_UART_REQUEST_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 1	RCV_SD_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 0	RCV_RESET_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse

MASK4 Register/Address: 54H (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	MIN_UCP_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 6	ABNORMAL_PLUG_IN_INT_M	0b: not mask for INT pulse 1b: mask	Y	Y	Read/write	0b: not mask for INT pulse
Bit 5	Reserved		NA	NA	Read only	Default:0b
Bit 4	Reserved		NA	NA	Read only	Default:0b
Bit 3	Reserved		NA	NA	Read only	Default:0b
Bit 2	Reserved		NA	NA	Read only	Default:0b
Bit 1	Reserved		NA	NA	Read only	Default:0b
Bit 0	Reserved		NA	NA	Read only	Default:0b

WD_RESET Register/Address: 5AH (Default: 00H)

Bit	Symbol	Description	REG_RST	WDT_RST	Read/Write	Default
Bit 7	Reserved		NA	NA	Read only	Default:0b
Bit 6	Reserved		NA	NA	Read only	Default:0b
Bit 5	Reserved		NA	NA	Read only	Default:0b
Bit 4	Reserved		NA	NA	Read only	Default:0b
Bit 3	Reserved		NA	NA	Read only	Default:0b
Bit 2	Reserved		NA	NA	Read only	Default:0b
Bit 1	Reserved		NA	NA	Read only	Default:0b
Bit 0	WD_RESET	0: Normal 1:Reset(then reset to 0)	Y	N	Read/write	Normal(0b)

Serial Port Interface (I²C)

Bus Interface

Baseband Processor can transmit data with ET9563 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET9563 will send a low level response signal with one period width to the SDA port. During the reading mode, ET9563 will not send response signal and the host will send a high response signal one period width to the SDA.

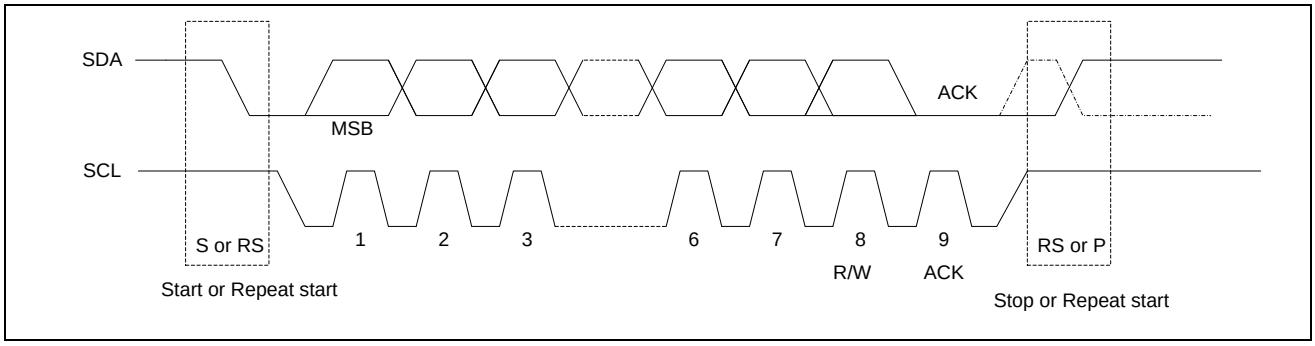


Figure 11. I²C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =400KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform

Chip Address：00001100b (Writing Register mode)/00001101b (Reading Register Mode)

I²C Writing Command Register Interface Protocol (continuous):

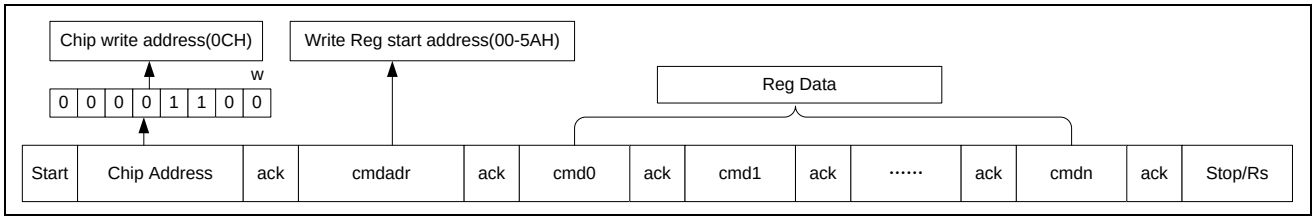


Figure 12. I²C Writing Command Register(continuous)

- Start=Start Conditions
- Chip address=Write register address =0000110+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge
- ……
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single):

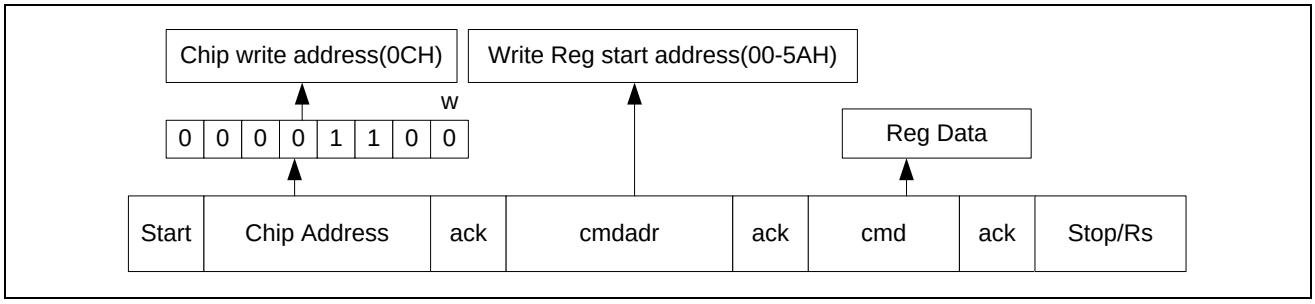


Figure 13. I²C Writing Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=0000110+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(REG's8bit address)
- ack=Acknowledge
- Reg data= cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(continuous)

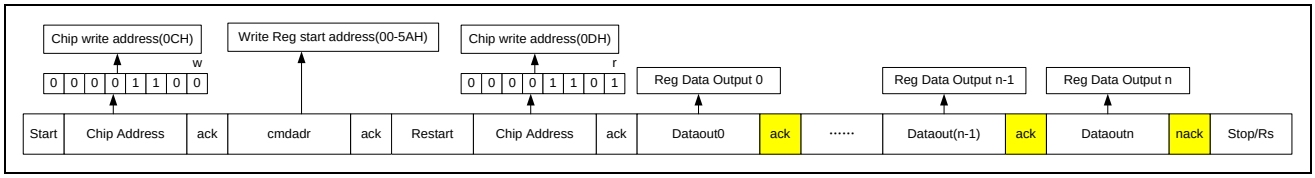


Figure 14. I²C Reading Command Register

- Start=Start Conditions
- Chip address =Write register address=0000110+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack=Acknowledge
- Restart=Restart condition
- Chip address Read register address=0000110+1(r)b
- ack=Acknowledge
- Dataout=Register data output
- Ack= Acknowledge from Host Device
- Dataout=Register data output
- …….
- Dataout=Register data output
- nack=No Acknowledge from Host Device
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(single)

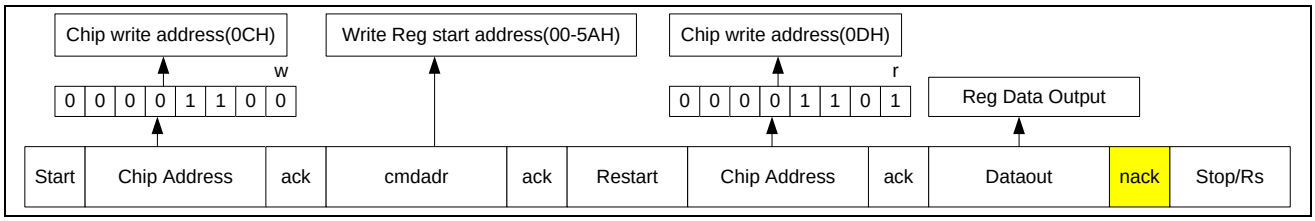


Figure 14. I²C Reading Command Register

- Start=Start Conditions
- Chip address =Write register address=0000110+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack=Acknowledge
- Restart=Restart condition
- Chip address Read register address=0000110+1(r)b
- ack=Acknowledge
- Dataout=Register data output
- nack=No Acknowledge from Host Device
- Stop/Rs=Stop Condition/Restart Condition

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Range		Unit
V_{IN},V_{CAP}	VIN, VCAP		-0.3~20		V
V_{IO}	Other Pins		-0.3~6.0		V
I_{MAX1}	Maximum Continuous Current of IN to BAT		<1.0		A
I_{MAX2}	Maximum Continuous Current of IN to SYS		<1.0		A
I_{MAX3}	Maximum Continuous Current of BAT to SYS		<3.2		A
P_D	Power Dissipation at T_A= +25°C		<1.5		W
T_{STG}	Storage Junction Temperature		-65~150		°C
T_{JMAX}	Junction Temperature		<+150		°C
T_A	Operating Temperature Range		-40~85		°C
T_L	Soldering Temperature (reflow)		<+260		°C
V_{ESD}	Electrostatic Discharge Capability	Human Body Model	All Pins	1.5	kV
		Charged Device Model	All Pins	2.0	kV

Electrical Characteristics

Unless otherwise noted, typical values are at V_{IN}=5V, V_{BAT}=4V, T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Input Voltage				20	V
V_{IN}	Input Operation Voltage		3	5	5.5	V
I_{IN1}	Supply Current at IN, Charge Enable	V_{IN}=5.5V, I_{CHG}=0A, V_{BAT}=4.3V, I_{SYS}=0A,Charge Enable, NTC Disable		450	550	μA
I_{IN2}	Supply Current at IN, Charge Disable	V_{IN}=5.5V, I_{CHG}=0A, I_{SYS}=0A, Charge Disable, V_{BAT}=4.3V, NTC Disable		430	530	μA
I_{IN3}	Supply Current at IN, LDO Disable	V_{IN}=5.5V, I_{CHG}=0A, I_{SYS}=0A, LDO Disable, V_{BAT}=4.3V, NTC Disable		300	400	μA
I_{BAT}	Supply Current at BAT	V_{IN}=0V, I_{SYS}=0A, V_{BAT}=4.35V, NTC Disable		13	16	μA
		V_{IN}=0V, I_{SYS}=0A, V_{BAT}=4.35V, NTC Enable, the Current on the External NTC Resistor is not Included		21	26	μA
		V_{SYS}=V_{IN}=0V, I_{SYS}=0A, V_{BAT}=4.35V, Disable NTC Function, Disable Watchdog, Disable BAT OCP, Disable INT		1	2	μA
		V_{SYS}=V_{IN}=0V, I_{SYS}=0A, V_{BAT}=4.35V, Shipping Mode		0.3	1	μA
V_{IN_OVP}	Input Over-voltage Protect Threshold	Input Rising Threshold	5.85	6.0	6.15	V
	OVP Threshold Hysteresis	Input Voltage Falling		300		mV
V_{UV_IN}	Input Under-voltage Threshold	Input Rising Threshold	2.75	2.9	3.05	V
	UVLO Hysteresis			130		mV
V_{UV_BAT}	Battery Under-voltage Threshold	Battery Voltage Falling Reg01[2:0]=100b	2.6	2.76	2.92	V
	Battery UVLO Range		2.4		3.03	V
	Battery UVLO Hysteresis			200		mV

Electrical Characteristics(Continued)

Unless otherwise noted, typical values are at V_{IN}=5V, V_{BAT}=4V, T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BAT_OVP}	Battery Over-voltage Protect Threshold	Battery Voltage Rising, Higher than V_{BATREG_VSET}		130		mV
Power Path Management						
I_{IN_LIM}	Input Current Limit	Default Reg10[3:0]=1111	450	500	550	mA
	Input Current Limit Range		50		500	mA
V_{IN_REG}	Input Voltage Regulation Threshold	Default Reg10[7:4]=1001	4.45	4.60	4.75	V
	Input Voltage Regulation Range		3.88		5.08	V
V_{SYS_REG}	System Output Voltage	V_{IN}=5.5V, I_{SYS}=10mA, I_{CHG}=0A Reg15[4:7]=1000b, Default	4.50	4.60	4.70	V
	System Output Voltage Range		4.2		4.95	V
V_{SYS}	System Output Voltage	BAT Discharge Mode, V_{BAT}=3.7V, I_{BAT}=100mA	3.6			V
		V_{IN}<V_{UV_IN} and V_{BAT}<V_{UV_BAT}		0		V
R_{ON_SYS}	IN to SYS Switch on Resistance	V_{SYS}=4.6V, I_{SYS}=100mA		150	200	mΩ
R_{ON_BAT}	BAT to SYS Switch on Resistance	V_{IN}<2V, V_{BAT}=3.5V, I_{SYS}=100mA		100	150	mΩ
I_{BAT_MAX}	BAT to SYS Current Limit	Reg15[3:0]=1001b	1700	2000[1]	2300	mA
	BAT to SYS Current Limit Range	Not Exceed Max P_D	400		3200[1]	mA
I_{BAT_LEK}	BAT to SYS Leakage Current	V_{BAT}=4.5V, V_{IN}=V_{SYS}=0V, BAT to SYS Close			1	μA
I_{SYS_LEK}	SYS to BAT Leakage Current	V_{SYS}=5.0V, V_{IN}=4.5V, V_{BAT}=0V			1	μA
T_{INT}	BAT Discharge Function Controlled by INT	INT Pull-low Lasting Time to Turn Off the Battery Discharge Function (Default)		16		s
		Battery MOSFET Lasts for the Off Time Duration before Auto-on (Default)		2		s

Electrical Characteristics(Continued)

Unless otherwise noted, typical values are at V_{IN}=5V, V_{BAT}=4V, T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Battery Charger						
V_{BAT_REG}	Battery Voltage Regulation Range	Programmed by I²C V_{SYS_REG}>V_{BAT_REG}+200mV	3.60		4.527	V
V_{BAT}	Default Battery Regulation Voltage	Reg13[6:0]=1010010b	4.179	4.200	4.221	V
I_{CHG}	Battery Charge Current Range	V_{IN}=5V, V_{BAT}=3.8V, Step=2mA	2		510	mA
	Default Charge Current	V_{IN}=5V, V_{BAT}=3.8V Reg12[7:0]=01000000b	121	128	135	mA
	Charge Current	V_{IN}=5V, V_{BAT}=3.8V Reg12[7:0]=00100000b	60	64	68	mA
		V_{IN}=5V, V_{BAT}=3.8V Reg12[7:0]=00000000b	1.7	2	2.3	mA
T_{Fold}	Charging Current Thermal Foldback Threshold	Junction Temperature Regulation Reg18[6:5]=11b		120 (1)		°C
I_{PRE}	Precharge Range	Programmed Range Reg11H[3:0]	1		16	mA
	Precharge Current	$I_{TC\_SETTING}$=2mA	1.7	2	2.3	mA
		$I_{TC\_SETTING}$=16mA	15	16	17	mA
I_{EOC}	End of Charge Current Range	Programmed Range Reg11H[7:4]	1		16	mA
	End of Charge Current	$I_{EOC\_SETTING}$=2mA	1	2	3	mA
		$I_{EOC\_SETTING}$=16mA	14	16	18	mA
V_{PRE}	Precharge Threshold Voltage	V_{BAT} Rising, set 3.0V	2.8	3.0	3.2	V
V_{PRE_HYS}	Precharge Threshold Voltage Hysteresis			60		mV
V_{RECHG}	Recharge Threshold Below V_{BAT_REG}	Reg14[7]=0b	60	100	140	mV
		Reg14[7]=1b	150	200	250	mV
I_{UCP}	Low Current Protection Range in Direct Charge Mode	Programmed Range, Reg17H[4:0]	30		600	mA
	Low Current Protection	$I_{UCP\_SETTING}$=90mA	65	90	110	mA

Electrical Characteristics(Continued)

Unless otherwise noted, typical values are at V_{IN}=5V, V_{BAT}=4V, T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Thermal Protection						
T_{SD}	Thermal Shutdown Rising Threshold			150 (1)		°C
T_{SD_HYS}	OTP Threshold Hysteresis			20 (1)		°C
I_{NTC}	NTC Output Current		48	50	52	uA
V_{COLD}	NTC Cold Protection Threshold	JEITA_T1_TEMP	1.244	1.294	1.344	V
V_{COOL}	NTC Cool Protection Threshold	JEITA_T2_TEMP，Reg19H[3:2]=01(Default)	0.89	0.921	0.95	V
V_{WARM}	NTC Warm Protection Threshold	JEITA_T3_TEMP，Reg19H[1:0]=01(Default)	0.23	0.242	0.254	V
V_{HOT}	NTC Hot Protection Threshold	JEITA_T4_TEMP	0.14	0.156	0.172	V
UART Communication						
V_{BAT_LOW}	Low Battery Voltage Threshold	Programmed Range Reg1CH[4:3]	3.2		3.5	V
		Reg1C[4:3]=10,BAT Rising $I_{BAT\_LOW\_SETTING}$=3.4V	3.3	3.4	3.5	V
Logic I/O Characteristics						
V_{IL}	Low Logic Voltage Threshold				0.4	V
V_{IH}	High Logic Voltage Threshold		1.3			V
Digital Clock and Watchdog Timer						
F_{DIG}	Digital Clock		28	32	36	kHz
T_{WDT}	Watchdog Timer	Reg1C[2:1]=11b		160		s

Note1. Guaranteed by design and characterization. Not a FT item.

I²C mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time (Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	0.1	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	20+0.1Cb (2)	300	ns
t_F	Data Hold Time2	-	20+0.1Cb (2)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note2. Cb=total capacitance of one bus line in pF.

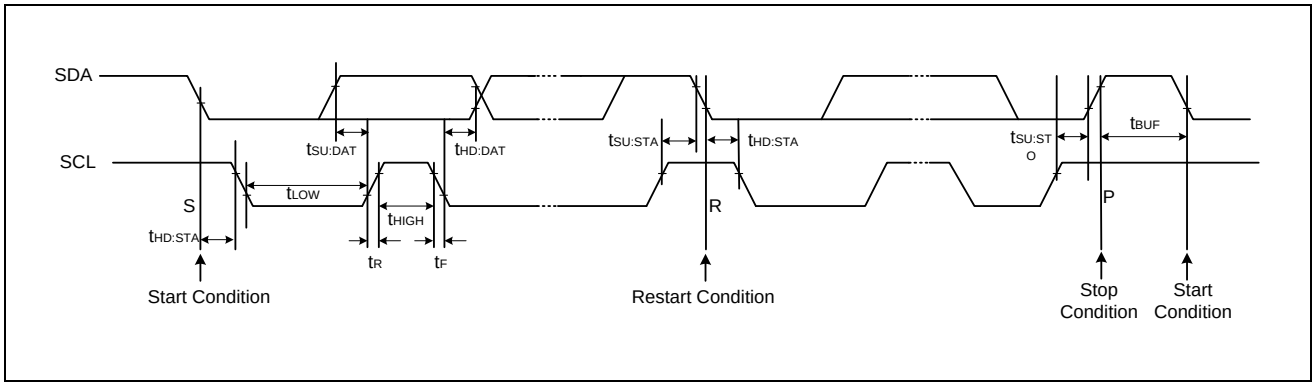
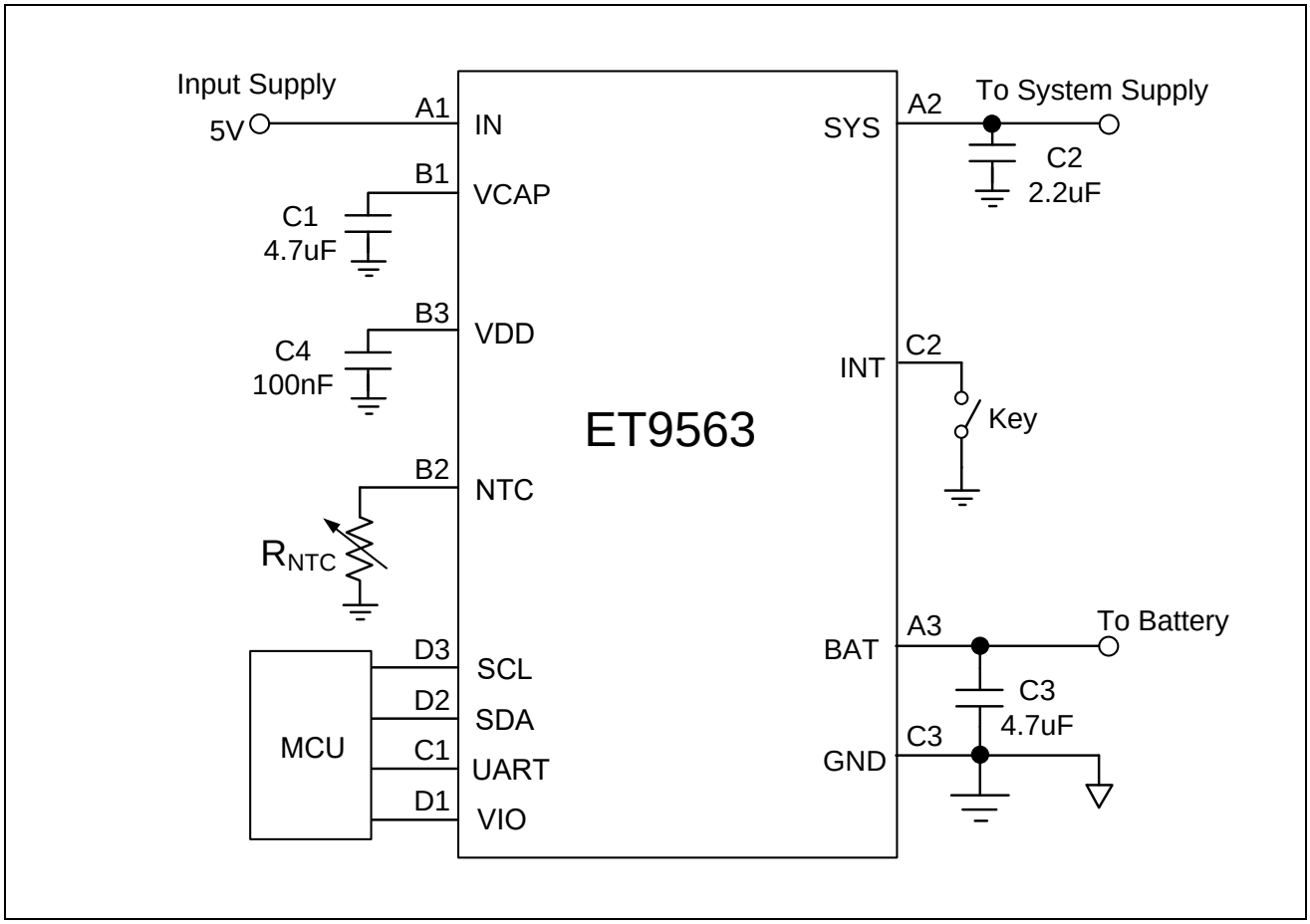


Figure 15. I²C mode Timing Diagram

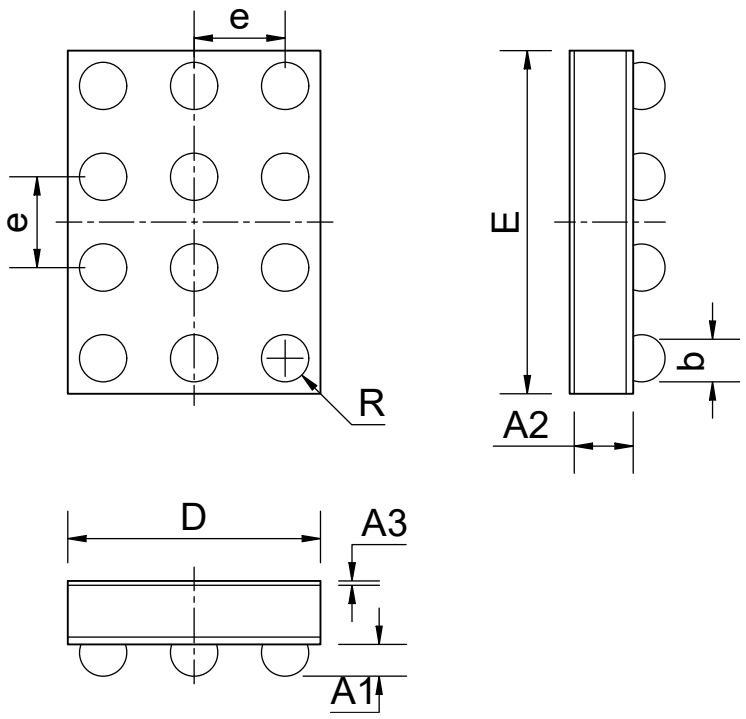
Typical Application Circuits



Note*. This electric circuit only supplies for reference.

Package Dimension

CSP12



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.18	0.20	0.22
A2	0.33	0.34	0.35
A3	0.028	0.035	0.042
b	0.23	0.26	0.29
D	1.60	1.65	1.70
E	2.00	2.05	2.10
e	0.40REF		
R	0.23	0.26	0.29

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-02-18	Preliminary Version	Xia Yong Jie	Xia Yong Jie	Liu Jia Ying
1.0	2023-10-17	Update EC Table Spec	Yin Peng	Xia Yong Jie	Liu Jia Ying
1.1	2024-05-23	Update Typeset and EC Table Spec	Yin Peng	Xia Yong Jie	Liu Jia Ying