12.4V, 7A Fully-Integrated Synchronous Boost Converters

General Description

The ET84501 is a fully-integrated synchronous boost converter with a 19mΩ main power switch and a 23mΩ rectifier switch. The device provides a high-efficiency and small-size power solution for portable equipment. The ET84501 features a wide input voltage range from 2.7V to 12V to support applications powered with single-cell or two-cell Lithium ion/polymer batteries. The ET84501 has 7A continuous switch current capability and provides output voltage up to 12.4V.

The ET84501 uses adaptive constant off-time peak current control topology to regulate the output voltage. In moderate to heavy load condition, the ET84501 works in the pulse width modulation (PWM) mode. In light load condition, the ET84501 works in the pulse frequency modulation (PFM) mode to improve the efficiency, while the ET84501 still works in the PWM mode to avoid application problems caused by low switching frequency. The switching frequency in PWM mode is adjustable from 200kHz to 2.2MHz. The ET84501 also implements a built-in 3ms soft start function and an adjustable peak switch current limit function. In addition, the device provides 13.0V output over-voltage protection, cycle-by-cycle over-current protection, and thermal shutdown protection.

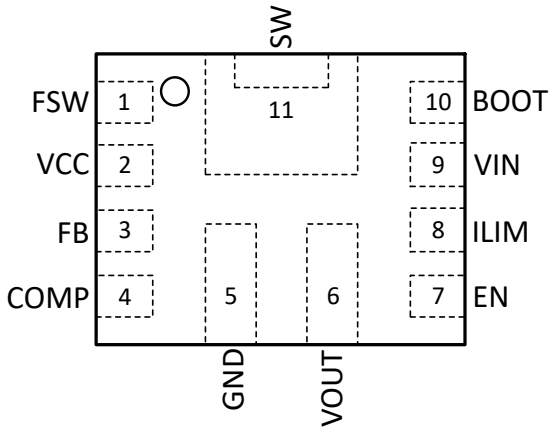
Features

- Input Voltage Range: 2.7 to 12V
- Output Voltage Range: 4.5 to 12.4V
- Up to 90% Efficiency at V_{IN} = 3.3V, V_{OUT} = 9V, and I_{OUT} = 2A
- Resistor-Programmable Peak Current Limit up to 11.5A for High Pulse Current
- Adjustable Switching Frequency: 200kHz to 2.2MHz
- 3ms Built-in Soft Start Time
- PFM Operation Mode at Light Load
- Output Over-voltage Protection at 13.0V
- Cycle-by-Cycle Over-current Protection
- Thermal Shutdown
- 2.00mm × 2.50mm UQFN11 Package

Applications

- Portable POS Terminal
- Bluetooth™ Speaker
- Quick Charge Power Bank

Pin Configuration

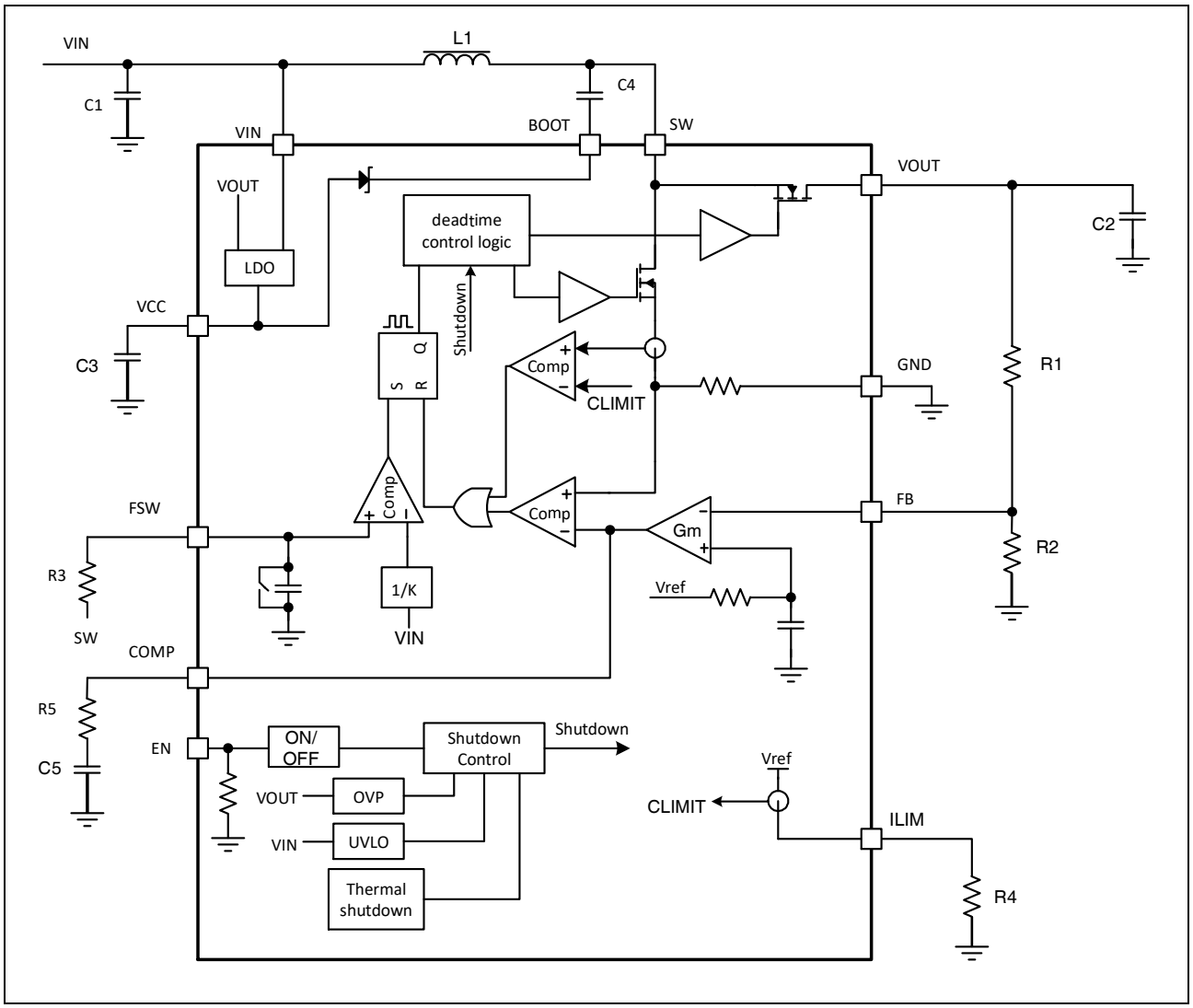


TOP VIEW

Pin Function

Pin Name	Pin No.	I/O	Pin Function
FSW	1	I	The switching frequency is programmed by a resister between this pin and the SW pin.
VCC	2	O	Output of the internal regulator. A ceramic capacitor of more than 1.0μF is required between this pin and ground.
FB	3	I	Output voltage feedback.
COMP	4	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and the GND pin.
GND	5	PWR	Ground
VOUT	6	PWR	Boost converter output.
EN	7	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
ILIM	8	O	Adjustable switching peak current limit. An external resister should be connected between this pin and the GND pin.
VIN	9	I	IC power supply input.
BOOT	10	O	Power supply for high-side MOSFET gate driver. A capacitor must be connected between this pin and the SW pin.
SW	11	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.

Block Diagram



Overview

The ET84501 is a synchronous boost converter, integrating a 19mΩ main power switch and a 23mΩ rectifier switch with adjustable switch current up to 11.5A. It is capable to output continuous power more than 18W from input of a single cell Lithium-ion battery or two-cell Lithium-ion batteries in series. The ET84501 operates at a quasi-constant frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load current, the ET84501 operates in PFM mode . The PFM mode brings high efficiency over the entire load range. The converter uses the constant off-time peak current mode control scheme, which provides excellent line and load transient response with minimal output capacitance. The external loop compensation brings flexibility to use different inductors and output capacitors. The ET84501 supports adjustable switching frequency ranging from 200kHz to 2.2MHz. The device implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The current limit is set by an external resistor.

Functional Description

Under-voltage Lockout (UVLO)

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.1V. A hysteresis of 600mV is added so that the device cannot be enabled again until the input voltage goes up to 2.7V.

Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 2.7V and the EN pin is pulled above the high threshold, the ET84501 is enabled. When the EN pin is pulled below the low threshold, the ET84501 goes into shutdown mode. The device stops switching in shutdown mode and consumes less than 3μA current. Because of the body diode of the high-side rectifier FET, the input voltage goes through the body diode and appears at the V_{OUT} at shutdown mode.

Soft Start

The ET84501 implements the soft start function to reduce the inrush current during start-up. The ET84501 begins soft start when the EN pin is pulled to logic high voltage. The soft start time is typically 3ms.

Adjustable Switching Frequency

The ET84501 features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the ET84501. Do not leave the FSW pin open. Use Equation 1 to calculate the resistor value required for a desired frequency.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{IN}} \right)}{C_{FREQ}} \quad (1)$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin
- C_{FREQ} = 32pF
- f_{SW} is the desired switching frequency
- t_{DELAY} = 72ns
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Adjustable Peak Current Limit

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch turns off immediately as long as the peak switch current touches the limit. The peak inductor current can be set by selecting the correct external resistor value correlating with the required current limit. Use Equation 2 to calculate the correct resistor value for the ET84501.

$$I_{LIM} = \frac{1180}{R_{ILIM}} \quad (2)$$

where

- R_{ILIM} is the resistance connected between the ILIM pin and ground,unit is kΩ.
- I_{LIM} is the switch peak current limit,unit is A.

For a typical current limit of 9.3A, the resistor value is 127kΩ for the ET84501.

Overvoltage Protection

If the output voltage at the V_{OUT} pin is detected above the overvoltage protection threshold of 13.0V (typical value), the ET84501 stops switching immediately until the voltage at the V_{OUT} pin drops the hysteresis voltage lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown happens at the junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 120°C, then the device starts switching again.

Device Functional Modes

Operation

The synchronous boost converter operates at a quasi-constant frequency pulse width modulation(PWM) in moderate to heavy load condition. Based on the V_{IN} to V_{OUT} ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips, and turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Since the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is not turned off until the fixed off-time is reached. After a short dead-time duration, the low-side switch is turned on again and the switching cycle is repeated. In light load condition, the ET84501 implements PFM mode for applications requiring high efficiency at light load.

PFM Mode

The ET84501 improves the efficiency at light load with PFM mode. When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. Once the current through the high-side N-MOSFET is zero, the high-side MOSFET is turned off until the beginning of the next switching cycle. When the output of the error amplifier continuously goes down and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the ET84501 delivers, the output voltage increases above the nominal setting output voltage. The ET84501 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.5% higher than the nominal setting voltage. With the PFM operation mode, the ET84501 keeps the efficiency above 70% even when the load current decreases to 1mA. At light load, the output voltage ripple is much smaller due to low peak inductor current. Refer to Figure 1.

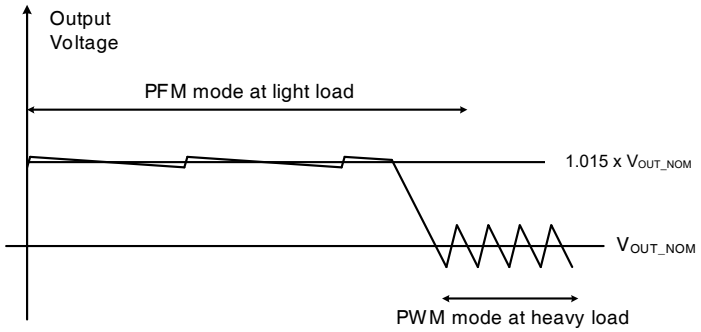


Figure 1 .Output Voltage in PWM Mode and PFM Mode

Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) [1]

Symbol	Parameters		Min	Max	Unit
V_{MAX}[2]	BOOT		-0.3	SW + 7	V
	VIN, SW, FSW, VOUT		-0.3	14.5	
	SW(10ns transient)		-3.5	19	
	EN, VCC, COMP, MODE		-0.3	7	
	ILIM,FB		-0.3	3.6	
T_J	Operating junction temperature		-40	150	°C
T_{STG}	Storage temperature		-65	150	°C
L_U	Latch Up (JESD78F)			±200	mA
ESD	Human Body Model, per JEDEC JS-001-2012	All Pins	±2.0		kV
	Charged Device Model, per JESD22-C101	All Pins	±1.5		

Note1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note2: All voltage values are with respect to network ground terminal.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters	Min	Typ	Max	Unit
V_{IN}	Input voltage range	2.7		12	V
V_{OUT}	Output voltage range	4.5		12.4	V
L	Inductance, effective value	0.47	2.2	10	µH
C_{IIN}	Input capacitance, effective value	10			µF
C_O	Output capacitance, effective value	10	47	1000	µF
T_J	Operating junction temperature	-40		125	°C
T_A	Operating temperature range	-40		85	°C

Electrical Characteristics

V_{IN} = 2.7 V to 5.5 V, V_{OUT} = 9 V, T_A= –40°C to 85°C. Typical values are at T_A = 25°C, unless otherwise noted.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		12	V
V_{IN_UVLO}	Under-voltage lockout (UVLO) threshold	V_{IN} rising	2.5	2.6	2.7	V
		V_{IN} falling	1.9	2.0	2.1	V
V_{IN_HYS}	V_{IN} UVLO hysteresis			600		mV
V_{CC}	regulation voltage	I_{CC}=2mA,V_{IN}=8V	4.5	5.1	5.7	V
V_{CC_UVLO}	UVLO threshold	V_{CC} falling	1.95	2.1	2.25	V
I_Q	Quiescent current from the V_{IN}	IC enabled, No load, V_{IN}=2.7V to 5.5V , V_{FB} = 1.3V, V_{OUT} = 12V,T_J ≤ 85°C	0.1	1	5	μA
	Operating quiescent current from the V_{OUT}		50	100	200	μA
I_{SD}	Shutdown current into the V_{IN}	IC disabled, V_{IN}=2.7V to 5.5V T_J ≤ 85°C	0.1	1	5	μA
OUTPUT						
V_{OUT}	Output voltage range		4.5		12.4	V
V_{REF}	Reference voltage at the FB pin	PFM mode(3)		1.224		V
		PWM mode	1.188	1.212	1.236	V
I_{FB_LKG}	FB pin leakage current	V_{FB} = 1.2V			100	nA
V_{OVP}	Output overvoltage protection threshold	V_{OUT} rising	12.7	13.0	13.4	V
V_{OVP_HYS}	Output overvoltage protection hysteresis	V_{OUT} falling below V_{OVP}	0.15	0.25	0.35	V
t_{SS}	Soft startup time	C_{OUT}(effective) = 47μF, I_{OUT}=0A	1	3	5	ms
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} +200mV, V_{COMP} = 2.2V	13	20	27	μA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} –200mV, V_{COMP} = 2.2V	13	20	27	μA
V_{CCLP_H}	High clamp voltage at the COMP pin	V_{FB} = 1V, R_{ILIM} = 100kΩ	2.1	2.5	2.9	V
V_{CCLP_L}	Low clamp voltage at the COMP pin	V_{FB} = 1.4V, R_{ILIM} = 100kΩ,	1.4	1.8	2.2	V
G_{EA}	Error amplifier trans conductance	V_{COMP} = 2.2V	150	190	250	μS

Electrical Characteristics (Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{CC} = 5.1V		23	40	mΩ
	Low-side MOSFET on-resistance	V_{CC} = 5.1V		19	30	mΩ
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	R_{FSW} = 240kΩ	400	500	600	kHz
		R_{FSW} = 100kΩ	900	1100	1300	kHz
T_{ON_min}	Minimum on time	V_{CC} = 5.1V(3)		90	180	ns
CURRENT LIMIT						
I_{LIM}	Peak switch current limit	R_{ILIM} = 127kΩ	7.9	9.3	10.7	A
		R_{ILIM} = 100kΩ	9.8	11.5	13.2	A
V_{ILIM}	Internal reference voltage at ILIM pin		1.188	1.212	1.236	V
EN LOGIC INPUT						
V_{EN_H}	EN Logic high threshold		1.2		5	V
V_{EN_L}	EN Logic low threshold		0		0.4	V
R_{EN}	EN pull-down resistor		600	980	1550	kΩ
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold(3)		135	150	165	°C
T_{D_HYS}	Thermal shutdown hysteresis(3)		20	30	40	°C

Note3：Guaranteed by design.

Application Circuits

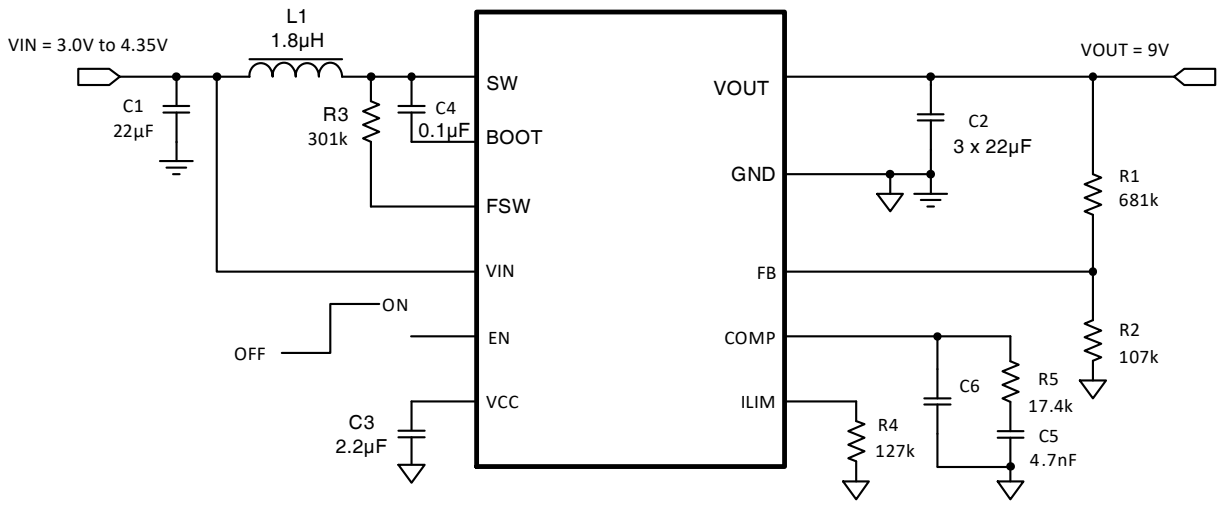


Figure 2. Typical Application Circuit

Design Requirements

Design Parameters	Example Values
Input voltage range	3.0 to 4.35V
Output voltage	9V
Output voltage ripple	100mV peak to peak
Output current rating	2A
Operating frequency	500kHz
Operation mode at light load	PFM

Detailed Design Procedure

Setting Switching Frequency

The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the ET84501. The resistor value required for a desired frequency can be calculated using Equation 3.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{IN}} \right)}{C_{FREQ}} \quad (3)$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin
- C_{FREQ} = 32 pF
- f_{SW} is the desired switching frequency
- t_{DELAY} = 72 ns
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Setting Peak Current Limit

The peak input current is set by selecting the correct external resistor value correlating to the required current limit. Use Equation 4 to calculate the correct resistor value:

$$I_{LIM} = \frac{1180}{R_{ILIM}} \quad (4)$$

where

- R_{ILIM} is the resistance connected between the ILIM pin and ground,unit is kΩ.
- I_{LIM} is the switch peak current limit,unit is A.

For a typical current limit of 9.3A, the resistor value is 127kΩ. Considering the device variation and the tolerance over temperature, the minimum current limit at the worst case can be 0.8A lower than the value calculated by Equation 4. The minimum current limit must be higher than the required peak switch current at the lowest input voltage and the highest output power to make sure the ET84501 does not hit the current limit and still can regulate the output voltage in these conditions.

Setting Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 10μA flowing through the feedback divider gives good accuracy and noise covering. A standard 120kΩ resistor is typically selected for low-side resistor R2.When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus, the value of R1 is calculated as in Equation 5:

$$R1 = \frac{(V_{OUT} - V_{REF}) \times R2}{V_{REF}} \quad (5)$$

Inductor Selection

Because the selection of the inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The ET84501 is designed to work with inductor values between 0.47 and 10µH. A 0.47µH inductor is typically available in a smaller or lower-profile package, while a 10µH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a 10µH inductor can maximize the controller's output current capability.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 6 to Equation 7 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, recommends using the minimum switching frequency, the inductor value with -30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 6 .

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

- V_{OUT} is the output voltage of the boost regulator.
- I_{OUT} is the output current of the boost regulator.
- V_{IN} is the input voltage of the boost regulator.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 7.

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \quad (7)$$

- I_{PP} is the inductor peak-to-peak ripple.
- L is the inductor value.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Therefore, the peak current, ILpeak, seen by the inductor is calculated with Equation 8.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \quad (8)$$

Set the current limit of the ET84501 higher than the peak current I_{Lpeak}. Then select the inductor with saturation current higher than the setting current limit.

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the inductor's core loss. The ET84501 has optimized the internal switch resistance. However, the overall efficiency is affected significantly by the inductor's DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally. Would recommend an inductor with lower DCR and ESR. However, there is a tradeoff among the inductor's inductance, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors.

Input Capacitor Selection

For good input voltage filtering, recommends low-ESR ceramic capacitors. The IN pin is the power supply for the ET84501. A 0.1μF ceramic bypass capacitor is recommended as close as possible to the IN pin of the ET84501. The VCC pin is the output of the internal LDO. A ceramic capacitor of more than 1.0μF is required at the VCC pin to get a stable operation of the LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 10μF input capacitance is sufficient for most applications.

Output Capacitor Selection

For small output voltage ripple, recommends a low-ESR output capacitor like a ceramic capacitor. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Take care when evaluating a capacitor's derating under DC bias. The bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the following Equation 9 and Equation 10 to calculate the minimum required effective capacitance C_O:

$$V_{ripple\_dis} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_O} \quad (9)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times R_{ESR} \quad (10)$$

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.

- f_{SW} is the converter switching frequency.
- R_{ESR} is the ESR of the output capacitors.

Loop Stability

The ET84501 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network comprised of resistor R5, ceramic capacitors C5 and C8 is connected to the COMP pin.

The power stage small signal loop response of constant off time (COT) with peak current control can be modeled by Equation 11.

$$G_{PS}(S) = \frac{R_O \times (1-D)}{2 \times R_{sense}} \times \frac{\left(1+\frac{S}{2 \times \pi \times f_{ESRZ}}\right)\left(1-\frac{S}{2 \times \pi \times f_{RHPZ}}\right)}{1+\frac{S}{2 \times \pi \times f_P}} \quad (11)$$

- D is the switching duty cycle.
- R_O is the output load resistance.
- R_{sense} is the equivalent internal current sense resistor, which is 0.08Ω.
- f_P is the pole's frequency
- f_{ESRZ} is the zero's frequency
- f_{RHPZ} is the right-half-plane-zero's frequency

The D, f_P, f_{ESRZ}, and f_{RHPZ} can be calculated by following Equation 12:

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (12)$$

- η is the power conversion efficiency

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad (13)$$

- C_O is effective capacitance of the output capacitor

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (14)$$

- R_{ESR} is the equivalent series resistance of the output capacitor

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad (15)$$

The COMP pin is the output of the internal trans conductance amplifier. Equation 16 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{COMZ}}\right)}{\left(1 + \frac{S}{2 \times \pi \times f_{COMP1}}\right)\left(1 + \frac{S}{2 \times \pi \times f_{COMP2}}\right)} \quad (16)$$

where

- G_{EA} is the amplifier's trans conductance
- R_{EA} is the amplifier's output resistance
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C. The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

At the crossover frequency, the loop gain is 1. Thus the value of R5 can be calculated by Equation 17, then set the values of C5 and C6 (in ET84501 Single Cell Li-ion Battery to 9V/2A Output Converter) by Equation 18 and Equation 19.

$$R5 = \frac{2\pi \times V_{OUT} \times R_{sense} \times f_C \times C_O}{(1-D) \times V_{REF} \times G_{EA}} \quad (17)$$

- f_C is the selected crossover frequency

The value of C5 can be set by Equation 18.

$$C5 = \frac{R_O \times C_O}{2R5} \quad (18)$$

The value of C6 can be set by Equation 19.

$$C6 = \frac{R_{ESR} \times CO}{R5} \quad (19)$$

If the calculated value of C6 is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7V to 12V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47µF.

Layout

Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability andnoise problems. To maximize efficiency, switching rise time and fall time are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs to be close to the IN pin and GND pin to reduce the input supply current ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the OUT pin, but also to the GND pin to reduce the overshoot at the SW pin and OUT pin.

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, PD(max), and keep the actual power dissipation less than or equal to PD(max). The maximum-power-dissipation limit is determined using Equation 20.

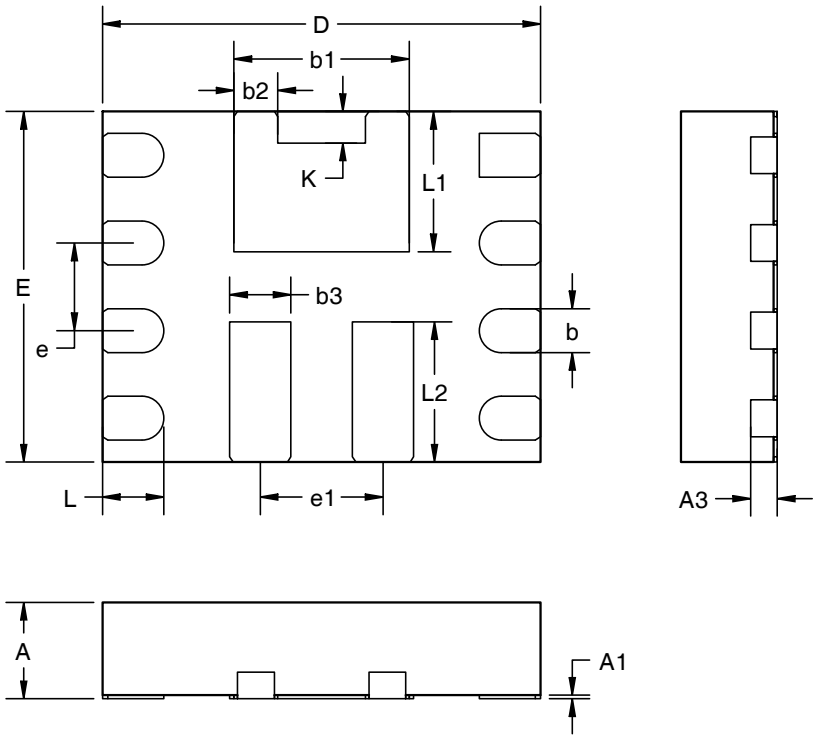
$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \quad (20)$$

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table

The ET84501 comes in a thermally-enhanced QFN package. The pads underneath the package improve the thermal capabilities of the package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connection. Using thick PCB copper and soldering the SW pin, OUT pin, and GND pin to large copper plate enhances the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

Package Dimension

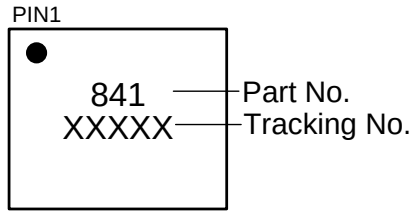
UQFN11



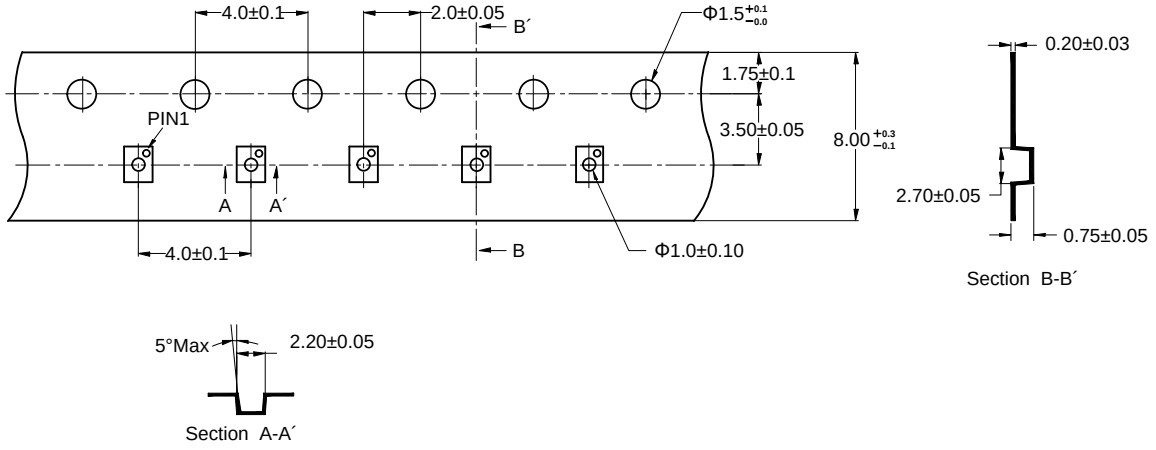
COMMON DIMENSIONS (Units:mm)

Symbol	Min	NOM	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF	
b	0.20	0.25	0.30
b1	0.90	1.00	1.10
b2		0.25REF	
b3	0.30	0.35	0.40
D	2.40	2.50	2.60
E	1.90	2.00	2.10
e	0.45	0.50	0.55
e1	0.60	0.70	0.80
K		0.18REF	
L	0.25	0.35	0.45
L1	0.70	0.80	0.90
L2	0.70	0.80	0.90

Marking



Reel Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-03-27	Preliminary Version	Caojc	Lugy	Liujy
0.1	2024-05-31	Preliminary Version	Caojc	Lugy	Liujy
0.2	2024-12-17	Update Electrical Characteristics and Package	LiuCong	Lugy	Liujy
0.3	2024-12-22	Add Marking & Tape rell	LiuCong	Lugy	Liujy
0.4	2025-02-28	EC Table Update	LiuCong	Lugy	Liujy
0.5	2025-03-05	Add Latch Up	LiuCong	Lugy	Liujy