2.5 MHz, Fixed-Output Synchronous Boost Regulator

General Description

The ET8210 is a low-power boost regulator. Even at minimum system battery voltage, the device maintains the output voltage regulation for a minimum output load current of 1A. The combination of built-in power transistors, synchronous rectification, and low supply current suit the ET8210 for battery-powered applications.

The ET8210 is available in a DFN8 (2mm ×2mm) .

Features

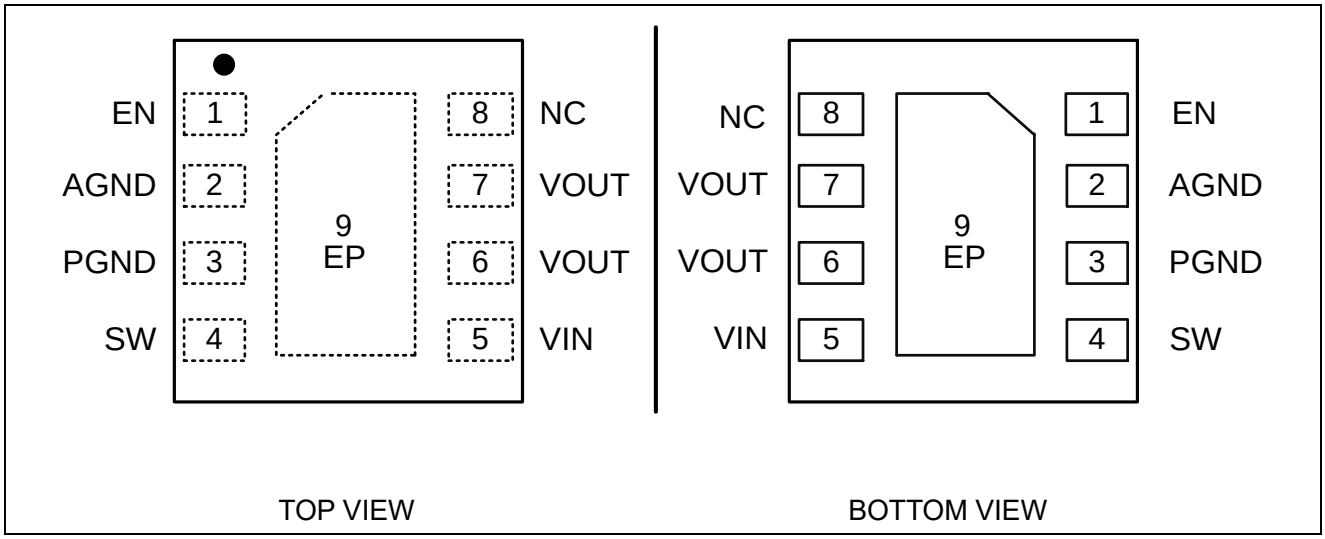
- Fixed Output Voltages: 5.4V
- I_{OUT}≥1A at V_{OUT}=5.4V, V_{IN}≥ 2.7V
- Automatic Pass-Through Operation when V_{IN}>V_{OUT}
- Internal Synchronous Rectification
- Soft-Start with True Load Disconnect
- Short-Circuit Protection
- Three External Components: 0.47uH Inductor / 10uF Input / 22uF Output Capacitors
- Part No. and package

Part No.	Package	MSL
ET8210	DFN8 (2mm x 2mm)	Level 1

Application

- Class-D Audio Amplifier and USB OTG Supply
- Boost for Low-Voltage Li-Ion Batteries
- Smart Phones, Tablets, Portable Devices

Pin Configuration

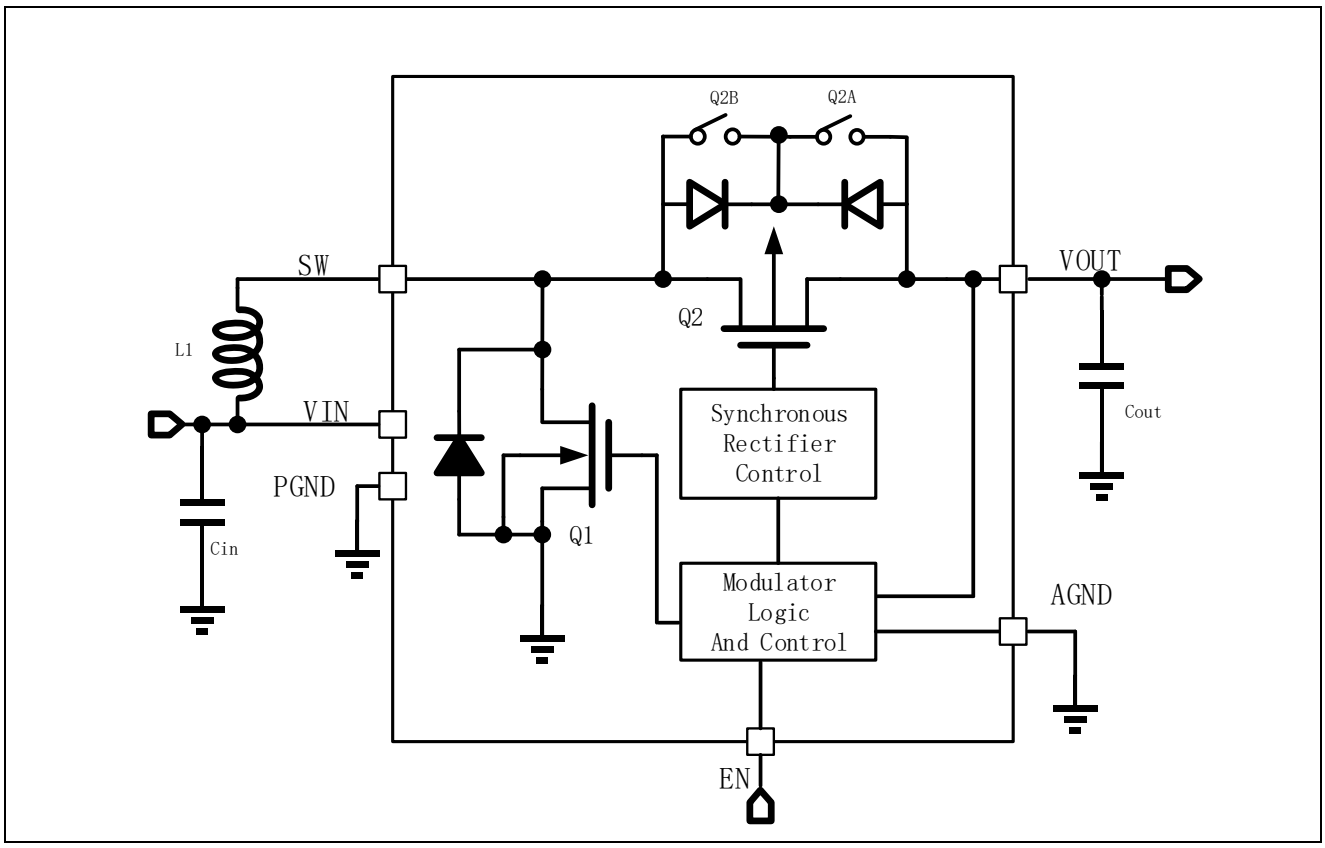


Note:EP is Exposed Pad

Pin Function

Pin No.	Pin Name	Description
1	EN	Enable. When this pin is HIGH, the circuit is enabled.
2	AGND	Analog Ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin-connect to PGND at a single point.
3	PGND	Power Ground. This is the power return for the IC. C_{OUT} capacitor should be returned with the shortest path possible to these pins.
4	SW	Switching Node. Connect to inductor.
5	VIN	Input Voltage. Connect to Li-Ion battery input power source; connect directly to C_{IN}.
6,7	OUT	Output Voltage. This pin is the output voltage terminal; connect directly to C_{OUT}.
8	NC	Not Connected.
9	Exposed Pad	Should be connected to AGND and PGND.

Block Diagram



Functional Description

Circuit Description

ET8210 is a synchronous boost regulator, typically operating at 2.5MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low V_{IN} voltages. The regulator's pass-Through Mode automatically activates when V_{IN} is above the boost regulator's set point.

Operating Modes

Mode	Description	Invoked When:
LIN	Linear Startup	$V_{IN}>V_{OUT}$
SS	Boost Soft-Start	$V_{IN}<V_{OUT}<V_{OUT(TARGET)}$
BST	Boost Operating Mode	$V_{OUT}=V_{OUT(TARGET)}$
PT	Pass-Through Mode	$V_{IN}>V_{OUT(TARGET)}$

Boost Mode Regulation

The ET8210 uses a current-mode modulator to achieve excellent transient response and smooth transitions between CCM and DCM operation. During CCM operation, the device maintains a switching frequency of about 2.5MHz. In light-load operation (DCM), frequency is naturally reduced to maintain high efficiency.

Shutdown and Startup

When V_{IN}>V_{UVLO}, EN voltage drop below V_{IL}, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, Current flow is prevented from VIN to VOUT, as well as reverse flow from VOUT to VIN. When V_{IN}>V_{UVLO},EN voltage rise above V_{IH},the IC will Re-start .It is recommended to keep load current draw below 500mA until the devices successfully executes startup. The following table describes the startup sequence.

Boost Startup Sequence

Start Mode	Entry	Exit	End Mode	Timeout(us)
LIN1	V_{IN}>V_{UVLO}, V_{IH}<V_{EN}≤V_{IN}	V_{OUT}>V_{IN}-300 mV	SS	
		TIMEOUT	LIN2	512
LIN2	LIN1 Exit	V_{OUT}>V_{IN}-300 mV	SS	
		TIMEOUT	FAULT	1024
SS	LIN1 or LIN2 Exit	V_{OUT} =$V_{OUT(TARGET)}$	BST	
		OVERLOAD TIMEOUT	FAULT	64

LIN Mode

When V_{IN}>V_{UVLO},EN voltage rise above V_{IH}, the regulator first attempts to bring V_{OUT} within 300mV of V_{IN} by using the internal fixed-current source from VIN(Q2).The current is limited to the LIN1 set point.

If V_{OUT} reaches VIN-300mV during LIN1 Mode, the SS Mode is initiated. Otherwise, LIN1 times out after 512us and LIN2 Mode are entered.

In LIN2 Mode, the current source is incremented to about 1.7A. If V_{OUT} fails to reach V_{IN}-300mV after 1024us, a fault condition is declared and the device waits 20ms to attempt an automatic restart.

Soft-Start (SS) Mode

Upon the successful completion of LIN Mode (V_{OUT}≥V_{IN}-300mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if V_{OUT} fails to reach regulation during the SS ramp sequence for more than 64us, a fault is declared. If large C_{OUT} is used, the reference is automatically stepped slower to avoid excessive input current draw.

Boost (BST) Mode

This is a normal operating mode of the regulator.

Pass-Through (PT) Mode

In normal operation, the device automatically transitions from Boost Mode to Pass-Through Mode if V_{IN} goes above the target V_{OUT}. In Pass-Through Mode, the device fully enhances Q2 to provide a very low impedance path from V_{IN} to V_{OUT}. Entry to the Pass-Through Mode is triggered by condition where V_{IN}>V_{OUT} and no switching has occurred during the past 5us. To soften the entry into Pass-Through Mode, Q2 is driven as a linear current source for the first 5us.Pass-Through Mode exit is triggered when V_{OUT} reaches the target V_{OUT} voltage. During Automatic Pass-Through Mode, the device is short circuit protected by a voltage comparator tracking the voltage drop from V_{IN} to V_{OUT}, if the drop exceeds 300mV, a fault is declared.

Fault State

The regulator enters Fault State under any of the following conditions:

- V_{OUT} fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- V_{OUT} fails to achieve the voltage required to advance from SS Mode to BST Mode.
- Boost current limit triggers for 2ms during BST Mode.
- V_{IN} - V_{OUT} > 300mV, this fault can occur only after successful completion of the soft-start sequence.
- V_{IN} < V_{UVLO}.

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between VIN and VOUT. After waiting 20ms, an automatic restart is attempted.

Over-Temperature

The regulator shuts down if the die temperature exceeds 150°C.Restart occurs when the IC has cooled by approximately 30°C.

Application Information

Output Capacitance (C_{OUT})

The effective capacitance (CEFF [(1)]) of small, high-value ceramic capacitors decreases as their bias voltage increases. ET8210 is guaranteed for stable operation with the minimum value of C_{EFF} ($C_{EFF(MIN)}$) outlined in below table.

Minimum C_{EFF} Required for Stability

Operating Conditions			$C_{EFF(MIN)}$ (uF)
V_{OUT}(V)	V_{IN}(V)	I_{LOAD} (mA)	
5.0	2.7 to 4.8	0 to 1000	3

Note:

1. C_{EFF} varies by manufacturer, capacitor material, and case size.

Startup

Input current limiting is in effect during soft-start, which limits the current available to charge C_{OUT} and any additional capacitance on the V_{OUT} line. If the output fails to achieve regulation within the limits described in the Soft-Start section above, a fault occurs, causing the circuit to shut down. It waits about 20ms before attempting a restart. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high current load and high capacitance are both present during Soft-Start, the circuit may fail to achieve regulation and continually attempt Soft-Start, only to have the output capacitance discharged by the load when in Fault State.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}.

$$V_{ripple(p\text{-}p)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}} \qquad \text{EQ1}$$

And

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{EQ2}$$

Therefore

$$V_{ripple(p-p)} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{C_{OUT}} \quad \text{EQ3}$$

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{EQ4}$$

The maximum V_{RIPPLE} occurs when V_{IN} is minimum and I_{LOAD} is maximum. For better ripple performance, more output capacitance can be added.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min	Max	Unit
V_{IN}	Voltage on VIN Pin		-0.3	6.0	V
V_{OUT}	Voltage on VOUT Pin			6.0	V
SW	SW Node	DC	-0.3	6.0	V
		Transient:10ns,3MHz	-0.3	8.0	
V_{EN}	Voltage on EN Pin		-0.3	V_{IN}+0.3	V
ESD	Electrostatic Discharge Protection Level	Human Body Model (JEDEC JS-001-2017)	±4		kV
		Charged Device Model(JEDEC JS-002-2018)	±1.5		
T_J	Junction Temperature Range		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. ETEK does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	2.7	4.8	V
I_{OUT}	Maximum Output Current	1000		mA
T_A	Ambient Temperature Range	-40	+85	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. Special attention must be paid not to exceed junction temperature, $T_{J\,(max)}$, at a given ambient temperature, T_A.

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance (DFN8)	75	°C/W

Electrical Characteristics

Recommended operating conditions, unless otherwise noted, circuit per typical application, V_{OUT}= 5.4V, V_{IN} = 2.7 V to 4.8V,T_A=-40°C to 85°C.Typical values are given V_{IN}=3.6V and T_A=25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Input Voltage Range(1)		2.7		4.8	V
I_Q	V_{IN} Quiescent Current	V_{IN}=3.6V,I_{OUT}=0,EN=V_{IN}		75	125	uA
		Shutdown: EN=0,V_{IN}=3.6V			5	
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising		2.1	2.3	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			150		mV
Inputs						
V_{IH}	Enable HIGH Voltage		1.05			V
V_{IL}	Enable LOW Voltage				0.4	V
I_{PD}	Current Sink Pull-Down	EN Pin, Logic HIGH		100		nA
R_{LOW}	Low-State Active Pull-Down	EN Pin, Logic LOW	300	400	500	kΩ
Outputs						
V_{REG}	Output Voltage Accurac DC(2)	Referred to V_{OUT}	-2		3	%
I_{LK_OUT}	VIN-to-VOUT Leakage Current	V_{OUT}=0,EN=0,V_{IN}=4.2V			1	uA
I_{LK}	VOUT-to-VIN Reverse Leakage Current	V_{OUT}=5.0V,EN=0,V_{IN}=2.5V			3.5	uA
V_{TRST}	Output Voltage Accuracy Transient(3)	Referred to V_{OUT}, 50-500mA Load Step	-5		5	%
Timing						
f_{SW}	Switching Frequency	V_{IN}=3.6V,V_{OUT}=5.0V, Load=1000mA	2	2.5	3	MHz
t_{SS}	Soft-Start EN HIGH to Regulation(3)	50ΩLoad,V_{OUT}=5.0V		600		us
t_{RST}	FAULT Restart Timer(3)			20		ms
Power Stage						
$R_{DS(ON)N}$	N-Channel Boost O-Switch $R_{DS(ON)}$	V_{IN}=3.6V,V_{OUT}=5.0V		80	130	mΩ
$R_{DS(ON)P}$	P-Channel Sync. Q-Rectifier $R_{DS(ON)}$	V_{IN}=3.6V,V_{OUT}=5.0V		90	115	mΩ
I_{V_LIM}	Boost Peak Current Limit	V_{OUT}=5.0V		3		A
$I_{V\_LIM\_SS}$	Boost Soft-Start Valley Current Limit	V_{IN}<V_{OUT}<V_{OUT_TARGET}, SS Mode		1.7		A
V_{MIN_1A}	Min V_{IN} for 1000mA Load(3)	V_{OUT}=5.0V		2.7		V
T_{SHDN}	Over-Temperature Protection(OTP) (3)			150		°C
T_{HYS}	OTP Hysteresis(3)			30		°C

Note:

1. The device can be operable when V_{IN} above 2.5V, but its load capacity has been reduced.
2. DC I_{LOAD} from 0 to 1A. V_{OUT} measured from mid-point of output voltage ripple. Effective capacitance of C_{OUT} ≥ 3uF.
3. Guaranteed by design and characterization; not a FT item.

Typical Characteristics

Unless otherwise specified; V_{IN}=3.6V,V_{OUT}=5.4V,unless otherwise noted T_A=25°C.

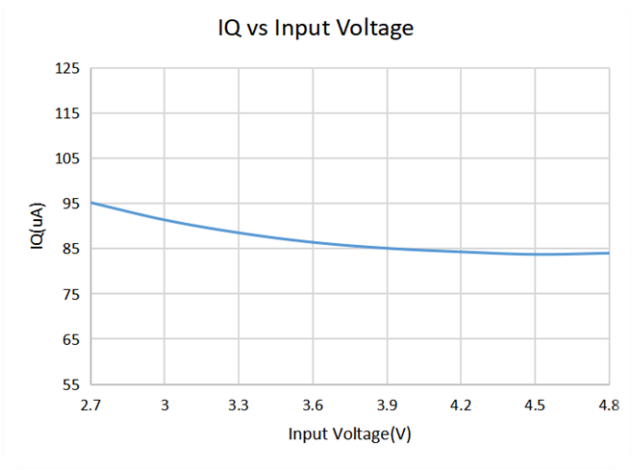


Figure1. I_Q vs Input Voltage

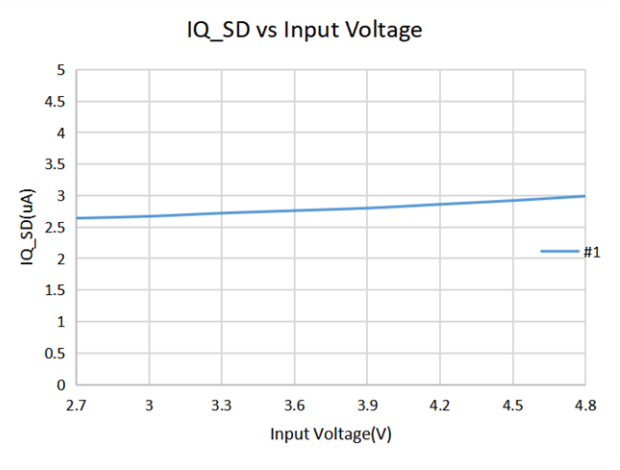


Figure2. I_{Q_SD} vs Input Voltage

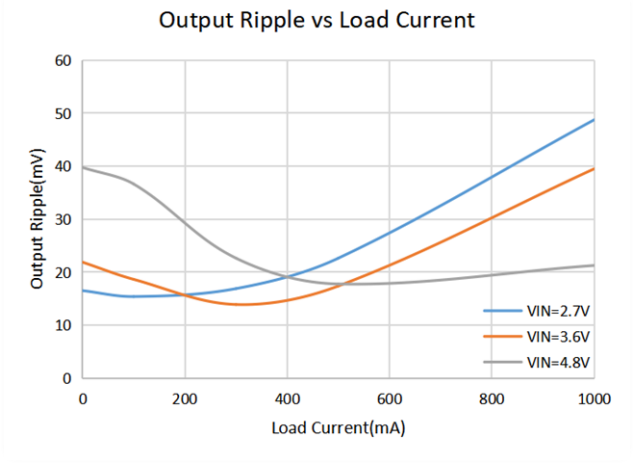


Figure3. Output Ripple vs Load Current and Input Voltage

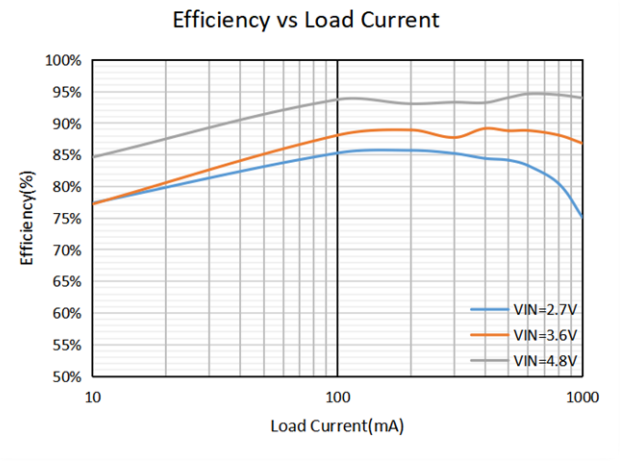


Figure4. Efficiency vs Load Current and Input Voltage

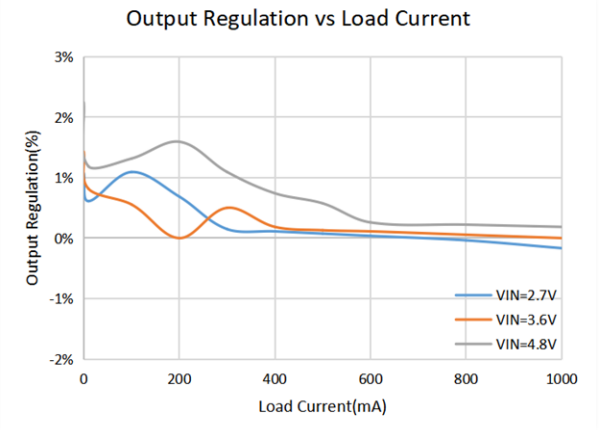


Figure5. Output Regulation vs Load Current and Input Voltage

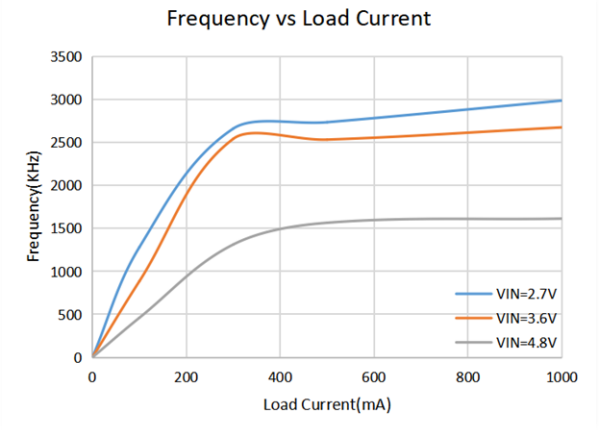


Figure6. Frequency vs Load Current and Input Voltage

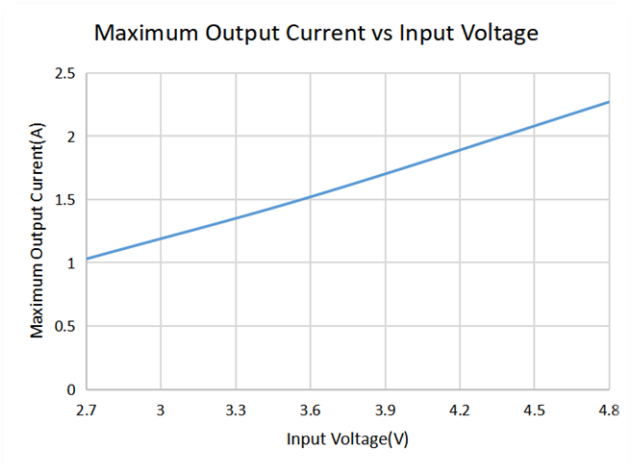


Figure7. Maximum Output Current vs Input Voltage

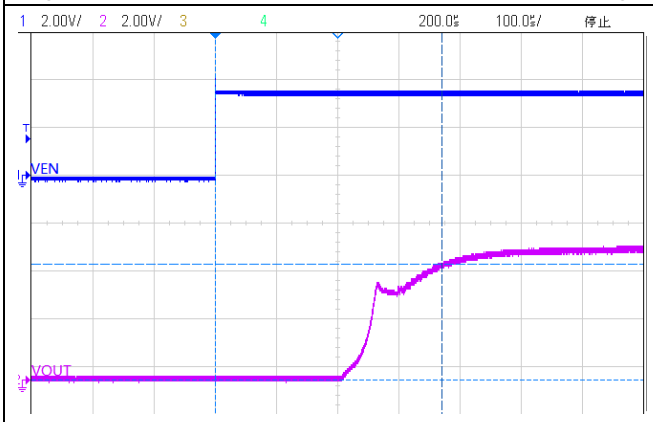


Figure8. Startup,Load=50Ω

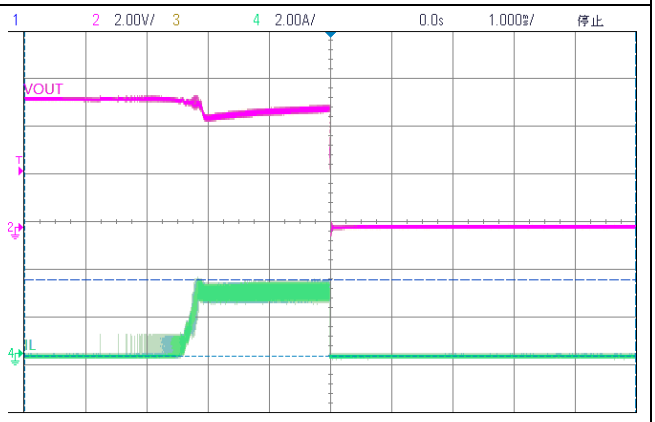


Figure9. Overload Protection

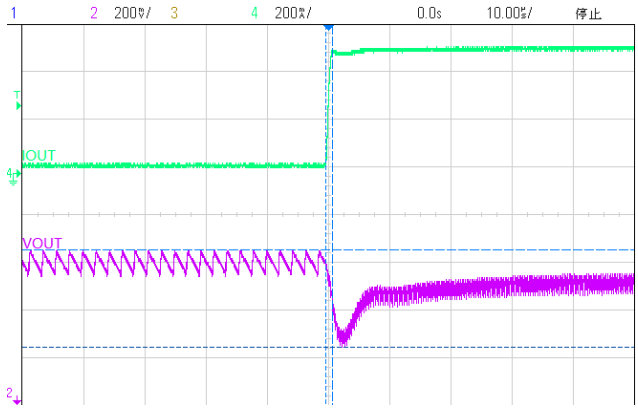


Figure10. Load Transient,50~500mA, Rise time is 1us

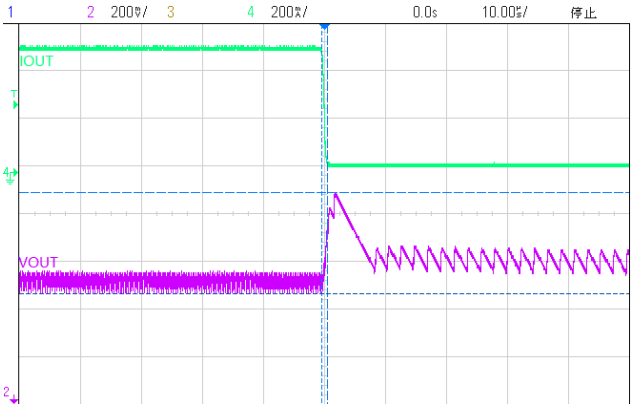


Figure11. Load Transient,500~50mA, Fall time is 1us

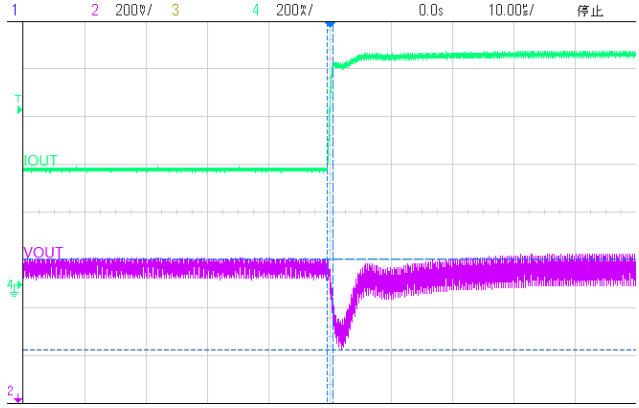


Figure12. Load Transient,500~1000mA, Rise time is 1us

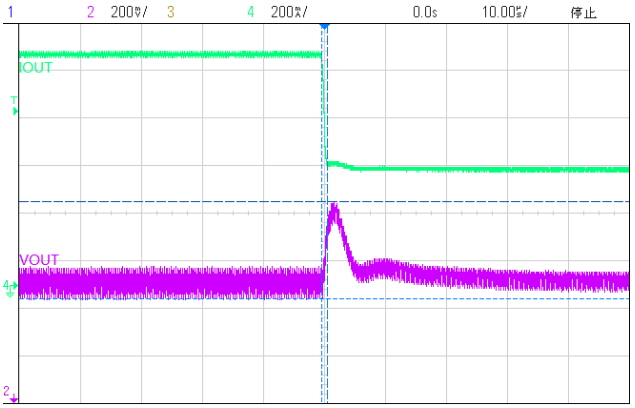


Figure13. Load Transient,1000~500mA, Fall time is 1us

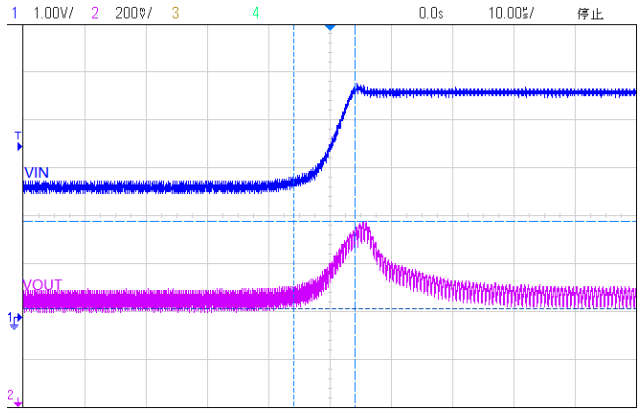


Figure14. Line Transient,2.7~4.8V,Load=500mA,Rise time is 10us

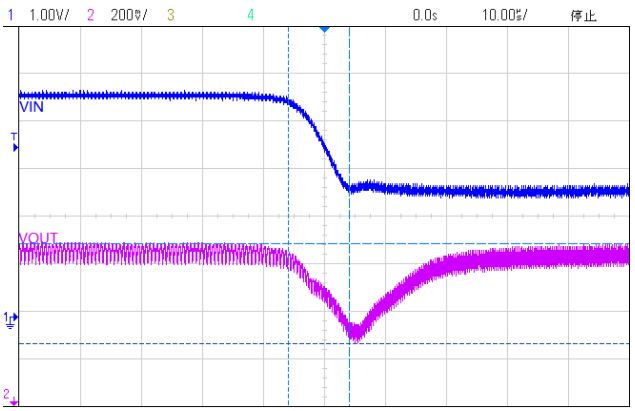
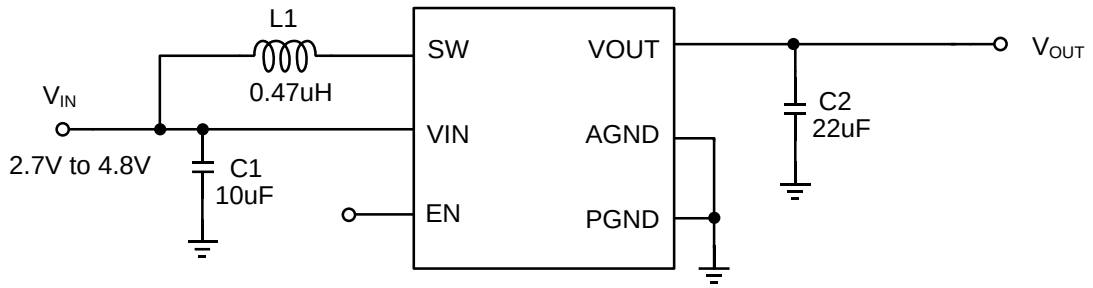


Figure15. Line Transient,2.7~4.8V,Load=500mA,Fall time is 10us

Application Circuits



Notes:

1.Unless EN connect to VIN,VIN should be powered on before EN.

2.This electric circuit only for reference.

Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.

2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.

3. Provide sufficient vias for the input capacitor and output capacitor.

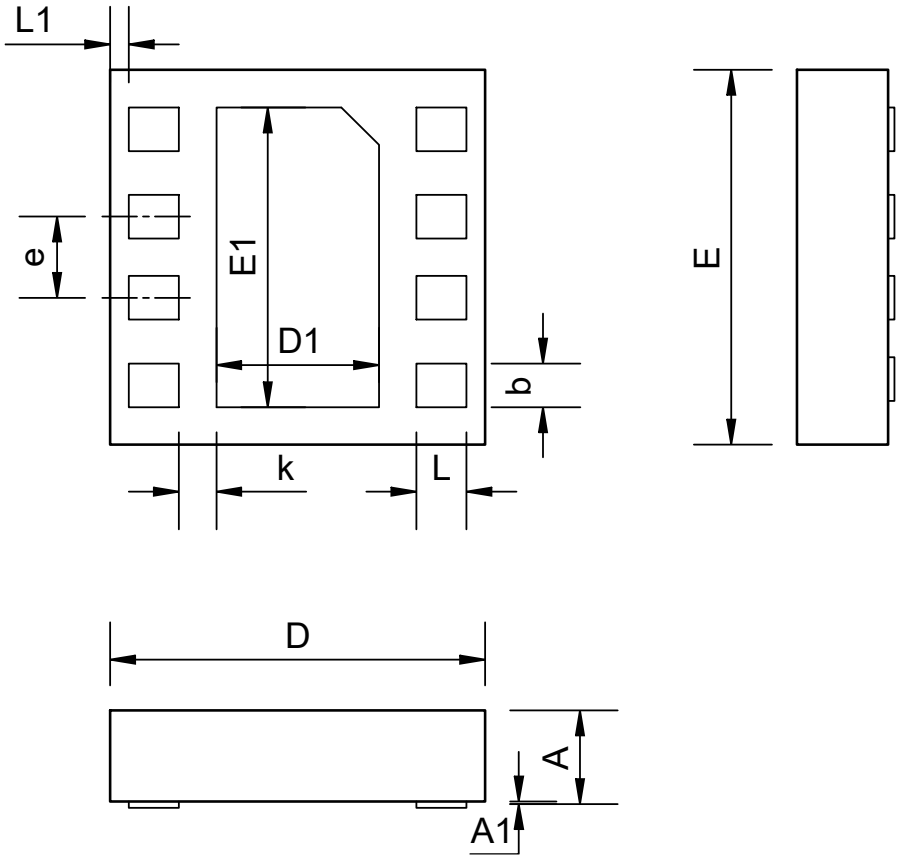
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.

5. Do not allow switching current to flow under the device.

6. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance

Package Dimension

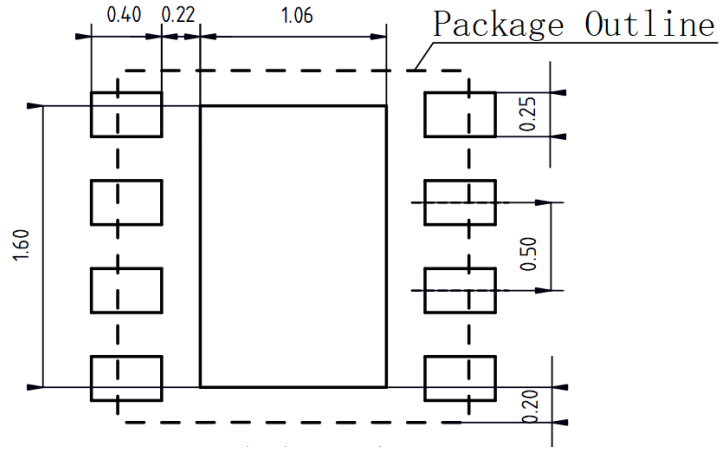
DFN8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

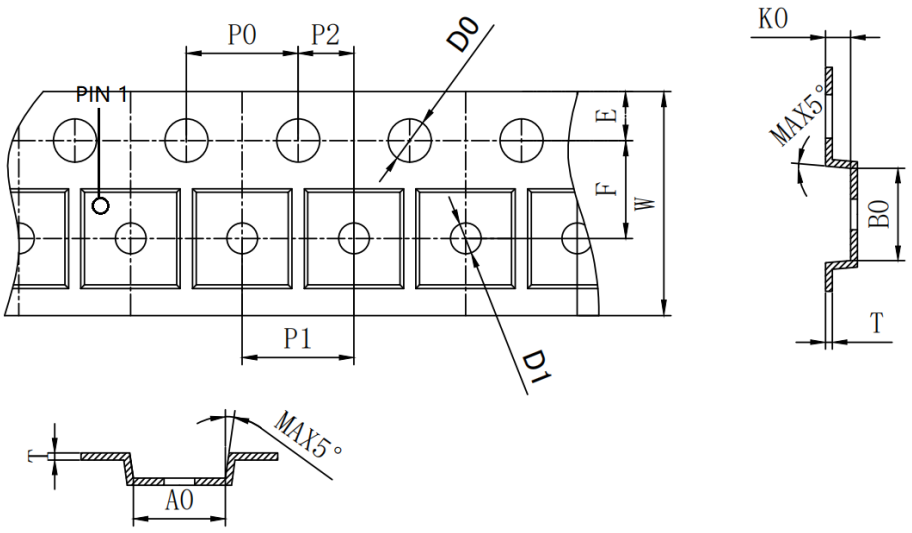
SYMBOL	MIN	NOM	MAX
A	0.700	--	0.800
A1	0.025	--	0.075
D	2.000	2.050	2.100
E	2.000	2.050	2.100
D1	0.750	0.850	0.950
E1	1.600	1.700	1.800
b	0.200	0.250	0.300
L	0.250	0.300	0.350
L1	0.010	0.050	0.090
K	0.250REF		
e	0.500BSC		

Recommended Land Pattern



Unit:mm

Tape



Symbol	A0	B0	K0	P0	P1	P2
Spec	2.25±0.10	2.25±0.10	0.70±0.10	4.00±0.10	4.00±0.10	2.00±0.05
Symbol	T	E	F	D0	D1	W
Spec	0.20±0.03	1.75±0.10	3.50±0.05	1.55±0.05	1.00 +0.10 -0.00	8.00 +0.10 -0.10

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2021-05-19	Initial Version	Huangxx	Huangxx	Liujy
1.1	2021-11-23	Update Graph and Tape Information	Huangxx	Huangxx	Liujy
1.2	2022-07-23	Update Document format	Shib	Huangxx	Liujy
1.3	2024-07-10	Update Soft-start Description	Liuc	Liuc	Liujy
1.4	2024-07-24	Update Layout Guidelines	Liuc	Liuc	Liujy