3A Synchronous Buck Converter with I²C Interface

General Description

The ET8330A is a synchronous BUCK converter with I²C interface. The output voltage and dynamic voltage scaling (DVS) slew rate can both be programmed by I²C.

When the load is moderate and heavy, the converter operates in PWM mode with 2.4MHz quasi fixed frequency. In light load condition, it can work in pulse frequency modulation (PFM) mode to achieve high efficiency by setting VSEL pin to low. In PFM mode, the typical quiescent current is only about 30uA. Even with such low quiescent current, the load transient performance is still excellent, due to adaptive constant on time (ACOT) structure has been adopted in ET8330A.

When VSEL PIN is set to high, it always works in PWM mode, no matter what the load is in Shutdown Mode, the supply current is typically about 0.2uA.

The ET8330A is available in a small WLCSP15 (1.15mm ×1.95mm).

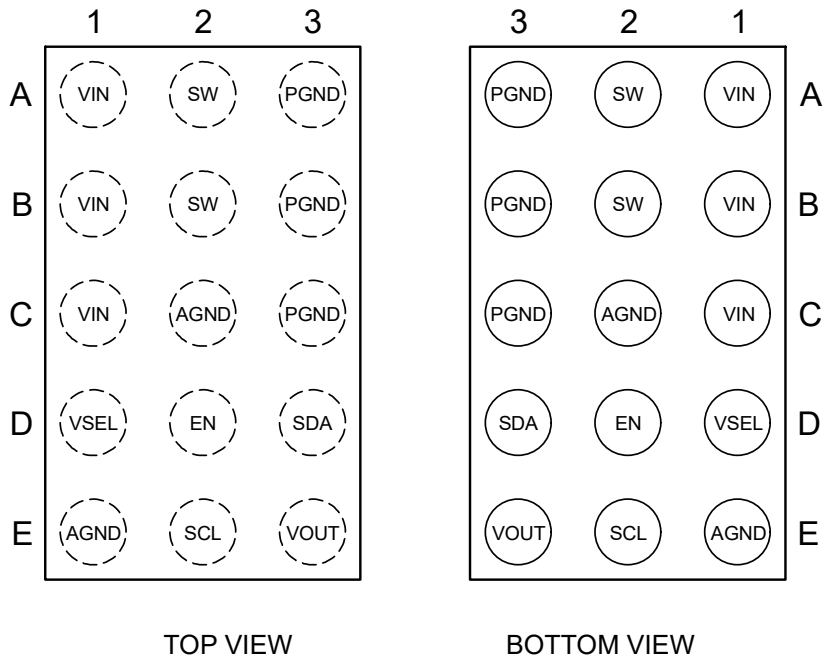
Features

- Programmable Output Voltage: 0.5V to 1.3V
- 2.5V to 5.5V Input Voltage Range
- Programmable Slew Rate for Dynamic Voltage Scaling (DVS)
- Quasi Fixed 2.4MHz Switching Frequency
- PFM Mode in Light Load Condition
- Excellent Load Transient Performance
- Capable of Delivering 3A Current
- 30uA Input Current with No Load in PFM Mode
- Thermal Shutdown and Over Current Protection
- WLCSP15 (1.15mm ×1.95mm ,0.4mm pitch) Package

Applications

- Application Processors
- Hard Disk Drives, LPDDR3, LPDDR4
- Tablets, Notebooks, Ultra-Mobile PCs
- Smart Phones
- Handheld Devices

Pin Configuration

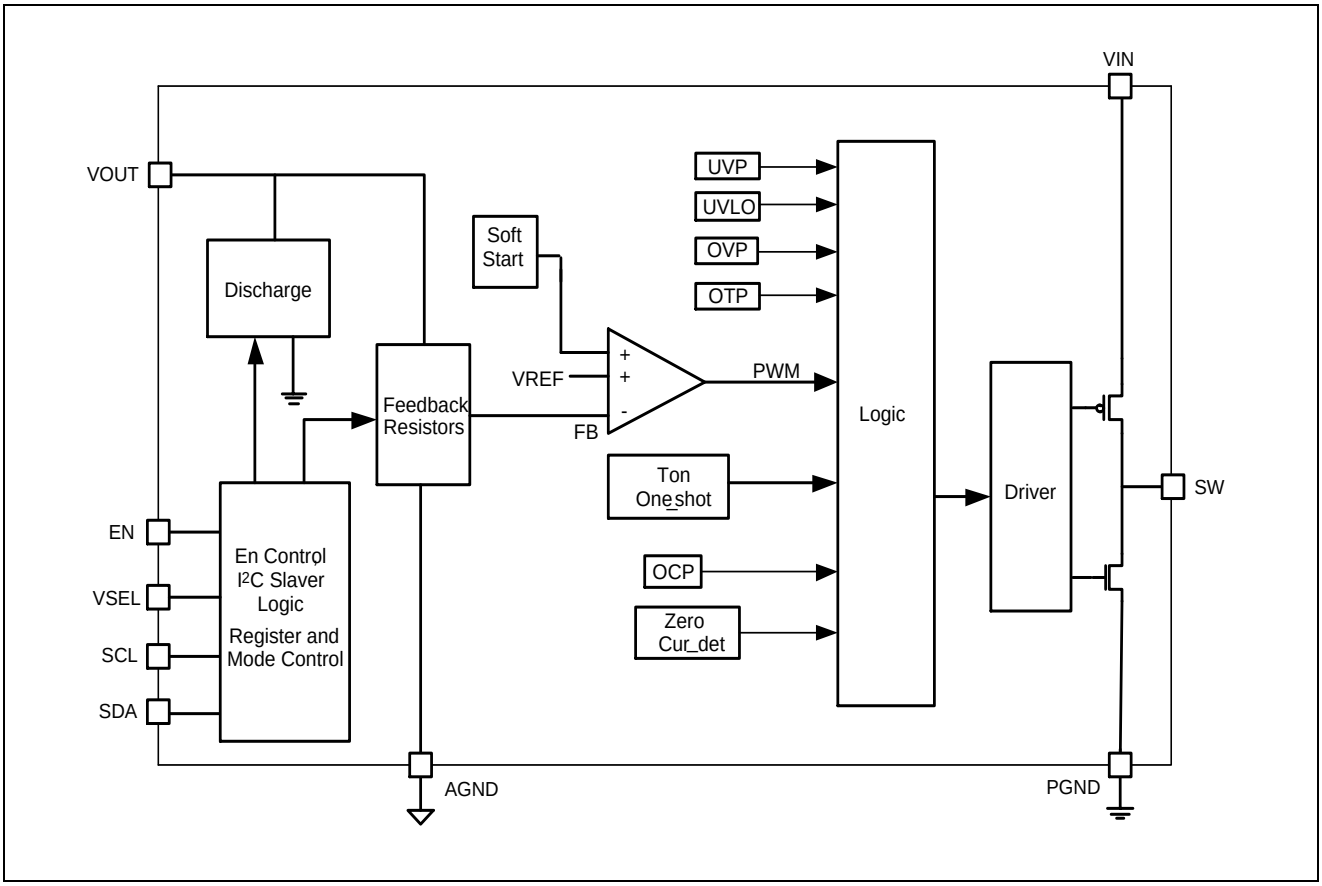


TOP VIEW BOTTOM VIEW

Pin Function

Pin No.	Pin Name	Pin Function
A1, B1, C1	VIN	Power supply pins. Connect to CIN capacitor as close as possible.
A2, B2	SW	Switching pins. Connect to the inductor.
A3, B3, C3	PGND	Power ground pins. The low-side MOSFET is referenced to these pins. CIN and COUT should be returned with a minimum path to these pins.
C2, E1	AGND	Analog ground pins. All signals are referenced to this pin.
D1	VSEL	FPWM or auto PFM/PWM select pin. When this pin is low, the converter works in auto PFM/PWM mode. When this pin is high, it works in forced PWM mode.
D2	EN	Enable pin. The device is shutdown Mode when this pin is low.
D3	SDA	I^2C serial data pin.
E2	SCL	I^2C serial clock pin.
E3	VOUT	VOUT sense pin. Output voltage sense through this pin. Connect to output capacitor.

Block Diagram



Operation

General Descriptions

The ET8330A is a synchronous step-down converter with 2.5V to 5.5V input voltage range. It's capable of delivering 3A current for output continuously. The output voltage ranges from 0.5V to 1.3V, which can be dynamically programmed by I^2C. To achieve excellent transient performance, ACOT structure has been adopted. By using this structure it can easily keep loop stable even with low-ESR ceramic output capacitors.

In steady-state PWM operation, the feedback voltage is compared to voltage reference. When the feedback voltage is less than the reference voltage, the on-time one-shot is triggered and high side power FET is turned on. When the on-time is over, the high side power MOSFET is turned off and the low side power MOSFET is turned on, until feedback voltage is lower than voltage reference.

In auto PFM mode, the on-time of high side MOSFET is same as that in PWM mode. However, because of low load, it takes much longer time discharge the output voltage. So after on-time is over, the off-time of high side power MOSFET is much longer accordingly. Then the frequency decreases automatically.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly calculated by the below Equation 1:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \quad (1)$$

Where **f** is nominal 2.4MHz.

Zero Current Detector

The zero current detector circuit senses the SW voltage during low side power MOSFET is on. When the SW voltage decreases to near zero, the low-side MOSFET is turned off to prevent the current flowing from output to GND.

Under-Voltage Protection (UVLO)

The UVLO module continuously monitors input voltage to make sure the converter works properly. When the input voltage is higher than threshold voltage of UVLO, the converter begins soft start to its regulated output voltage. When the input voltage decreases to its low threshold (350mV hysteresis), the converter shuts down.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 70% reference voltage after soft-start, the UVP is triggered.

Over-Current Protection (OCP)

When the low side power MOSFET is on, the ET8330A senses the inductor current. Only when the current is smaller than limit value, the high side power MOSFET is possibly turned on, even though the feedback voltage is lower than voltage reference. If the OCP last for about soft start time, it enters into hiccup mode. In hiccup mode, the shut time is about 1.7ms.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft start time can be programming by I^2C.

Over-Temperature Protection (OTP)

The ET8330A has over-temperature protection. When the junction temperature rises up to 150°C, it triggers OTP, and the device will be shut down, until junction temperature falls to 120°C.

Absolute Maximum Ratings

Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Symbol	Parameter		Rating	Unit
V_{IN}	Supply Input Voltage		-0.3 to 7.0	V
V_{SW}	SW Pin Switch Voltage		-1.0 to 7.3	V
V_{SW_MAX}	Switch Voltage<50ns		-5.0 to 8.5	V
V_{IO}	Other I/O Pin Voltages		-0.3 to 7.3	V
P_D	Power Dissipation@ T_A = 25°C	WLCSP15	2.38	W
θ_{JA} (1)	Package Thermal Resistance	WLCSP15	42	°C/W
T_{JMAX}	Max Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C
ESD	HBM (ESDA/JEDEC JS-001-2017) (2)		±2000	V

Note 1: θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 2: Devices are ESD sensitive. Handling precaution recommended.

Recommended Operating Range

The device is not guaranteed to function outside its operating conditions.

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Input Voltage	2.5 to 5.5	V
I_{OUT}	Output Current	0 to 3.0	A
T_J	Junction Temperature	-40 to 125	ºC
T_A	Ambient Temperature	-40 to 85	ºC

Electrical Characteristics

V_{IN}= 3.6V, L = 0.47μH, C_{OUT} = 22μF × 2 , T_A= -40°C to 85°C, unless otherwise specified.

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Operating Quiescent Current PWM[3]		I_{Q_PWM}	I_{LOAD} = 0, mode Bit = 1 (Forced PWM)		11		mA
Operating Quiescent Current PFM		I_{Q_PFM}	I_{LOAD} = 0		30		μA
H/W Shutdown Supply Current		$I_{SHDN\_H/W}$	V_{EN} = GND		0.2	3	μA
S/W Shutdown Supply Current		$I_{SHDN\_S/W}$	V_{EN} = V_{IN}, BUCK_ENx = 0, 2.5 V ≤ V_{IN} ≤ 5.0 V		2	12	μA
Under-Voltage Lockout Threshold		V_{UVLO}	V_{IN} rising		2.32	2.45	V
Under-Voltage Lockout Hysteresis		$\triangle V_{UVLO}$			350		mV
$R_{DS(ON)}$ of P-MOSFET		$R_{DS(ON)\_P}$	V_{IN} = 5.0V		27		mΩ
$R_{DS(ON)}$ of N-MOSFET		$R_{DS(ON)\_L}$	V_{IN} = 5.0V		16		mΩ
Input Voltage	Logic-High	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.0 V	0.9			V
	Logic-Low	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.0 V			0.4	
EN Input Bias Current		I_{EN}	EN input tied to GND or V_{IN}		0.01	1	uA
V_{OUT} DC Accuracy[3]		$\triangle V_{OUT1}$	2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} > 0.6V, Auto PFM/PWM	-2		2.5	%
		$\triangle V_{OUT2}$	2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} ≤ 0.6V, Auto PFM/PWM	-18		18	mV
		$\triangle V_{OUT3}$	2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} > 0.6V, Force PWM	-2		2	%
		$\triangle V_{OUT4}$	2.8V ≤V_{IN}≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} ≤ 0.6V, Force PWM	-12		12	mV
Load Regulation[3]		$\triangle V_{LOAD}$	$I_{OUT(DC)}$ = 1 to 3A		0.10		%/A
Line Regulation[3]		$\triangle V_{LINE}$	2.5V ≤ V_{IN} ≤ 5.0V， $I_{OUT(DC)}$ = 1.5A		0.10		%/V

Electrical Characteristics (Continued)

V_{IN}= 3.6V, L = 0.47μH, C_{OUT} = 22μF × 2 ,T_A= -40°C to 85°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transient Load Response[3]	AC_{LOAD1}	I_{LOAD} step 0.01A to 1.5A, t_R = t_F = 500ns, V_{OUT} = 1.125V		±45		mV
	AC_{LOAD2}	I_{LOAD} step 0.1A to 1.8A, t_R = t_F = 1us, V_{IN} = 3.8V, V_{OUT} = 0.9V		±56		mV
	AC_{LOAD3}	I_{LOAD} step 0.01A to 0.8A, t_R = t_F = 1μs		45		mV
Line Transient	V_{LINE}	V_{IN} = 3V to 3.6V, t_R = t_F = 10us, I_{OUT} = 100mA, Forced PWM mode		±40		mV
Valley Current Limit			3.5	4	4.5	A
Thermal Shutdown	T_{SD}			150		ºC
Thermal Shutdown Hysteresis	T_{SD_HYS}			30		ºC
Switching Frequency	f_{SW}	V_{OUT} = 0.6V		2400		kHz
Minimum Off-Time	t_{OFF_MIN}			170		ns
DAC Resolution[3]				8		Bits
DAC Differential Nonlinearity[3]					0.5	LSB

Note 3: Guaranteed by design，Not FT items.

Typical Operating Characteristics

Unless otherwise specified, Auto PFM/PWM mode, V_{IN} = 3.6V, V_{EN} = V_{IN}, L = 0.47μH, C_{OUT} = 22μF × 2, T_A = 25°C; Circuit and components according to typical application circuit.

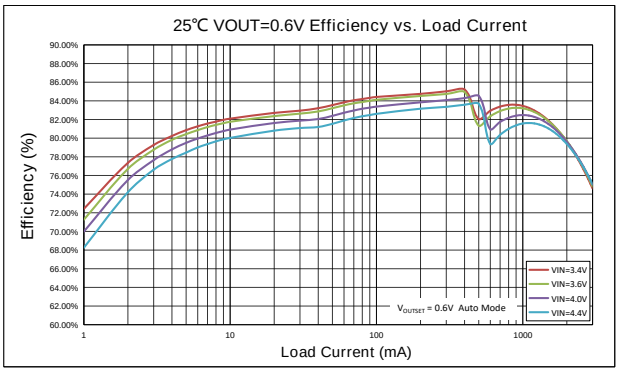


Figure 1. Efficiency vs. Load Current and Input Voltage, VOUT=0.600V

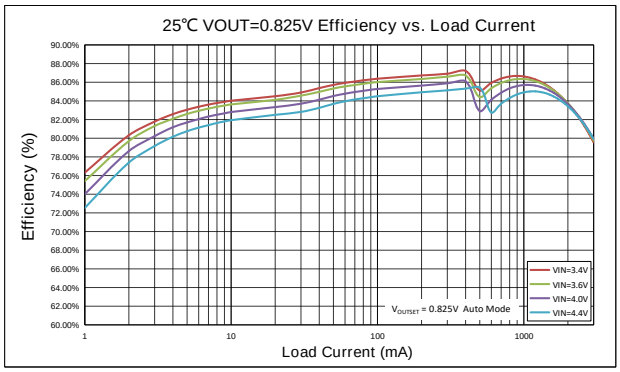


Figure 2. Efficiency vs. Load Current and Input Voltage, VOUT=0.825V

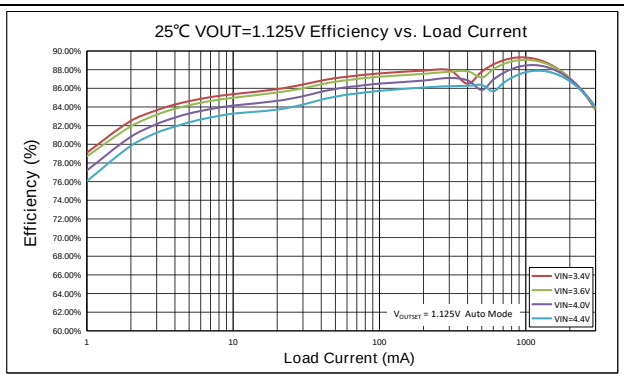


Figure 3. Efficiency vs. Load Current and Input Voltage, VOUT=1.125V

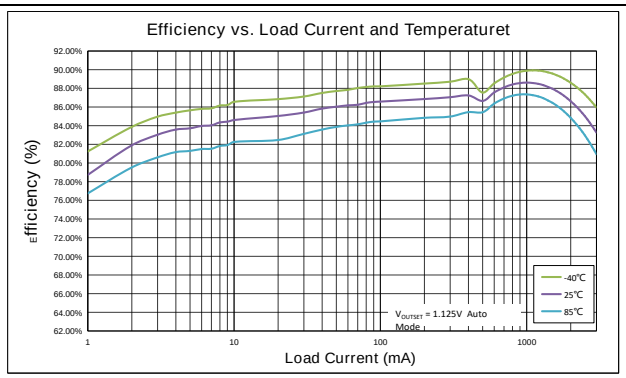


Figure 4. Efficiency vs. Load Current and Temperature, VIN=3.6V, 1.125V

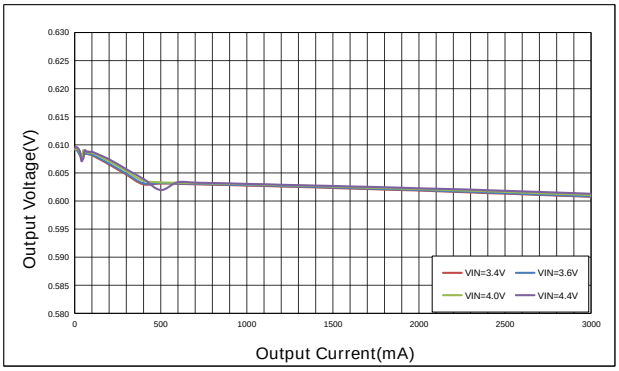


Figure 5. Output Voltage vs. Load Current , VOUT=0.6V

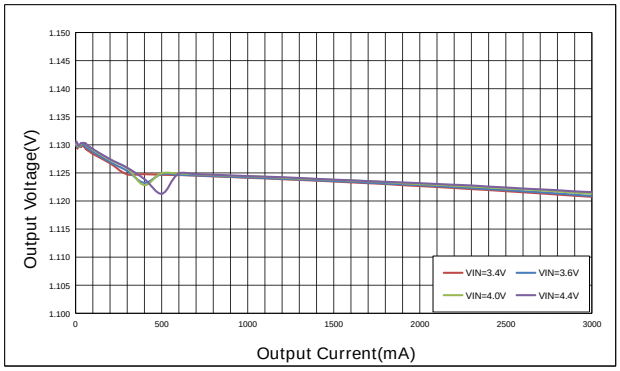


Figure 6. Output Voltage vs. Load Current , VOUT=1.125V

Typical Operating Characteristics(Continued)

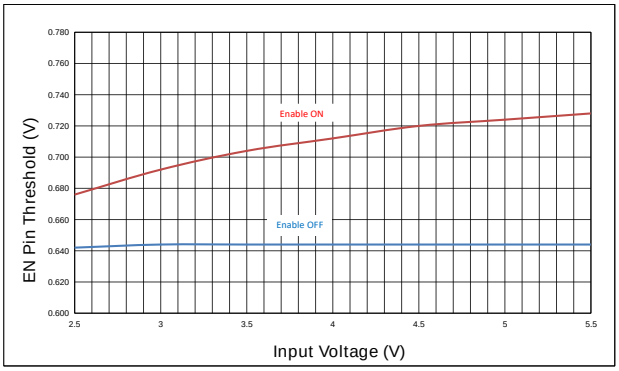


Figure 7. EN Pin Threshold vs. Input Voltage

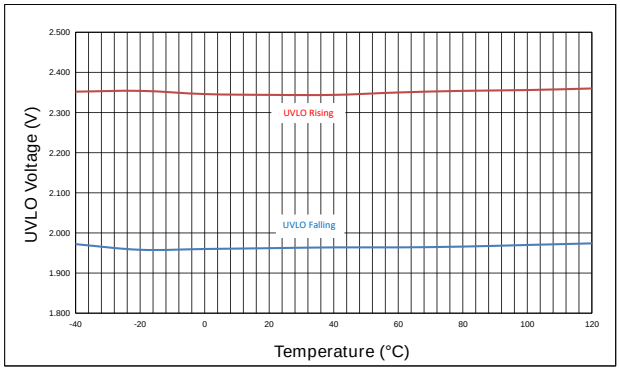


Figure 8. UVLO Voltage vs. Temperature

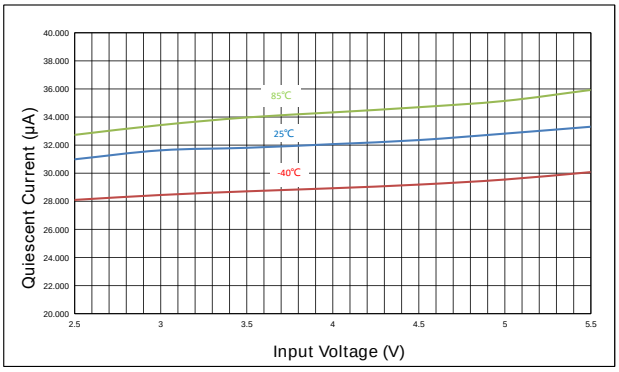


Figure 9. Quiescent Current vs. Input Voltage

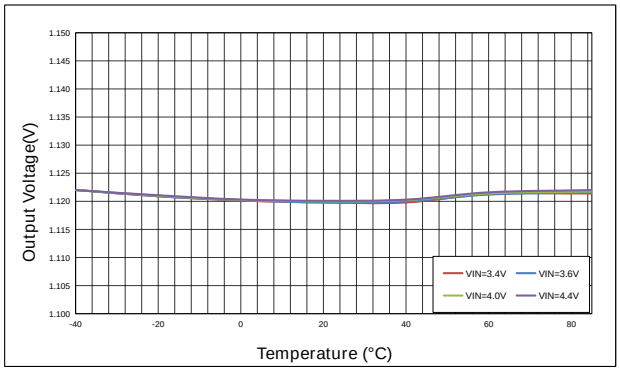


Figure 10. Output Voltage vs. Temperature

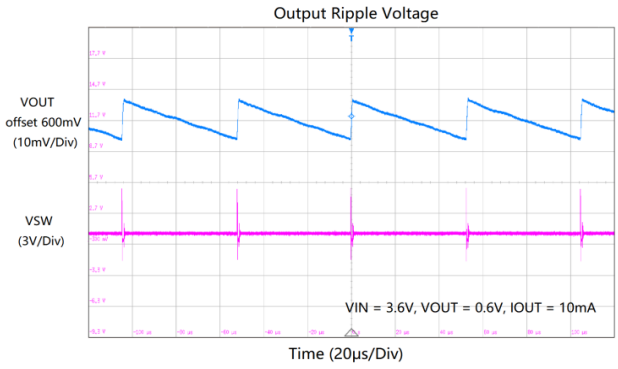


Figure 11. VOUT=0.6V, PFM Output Ripple

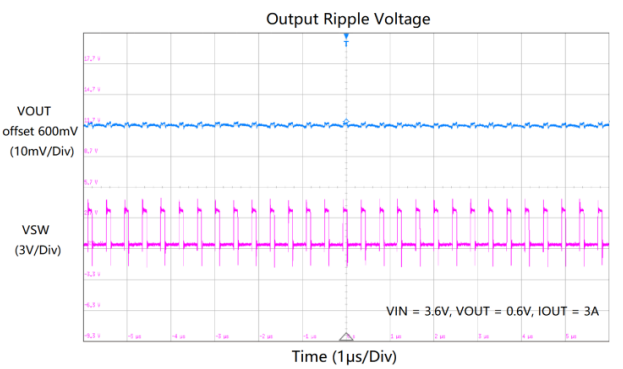


Figure 12. VOUT=0.6V, PWM Output Ripple

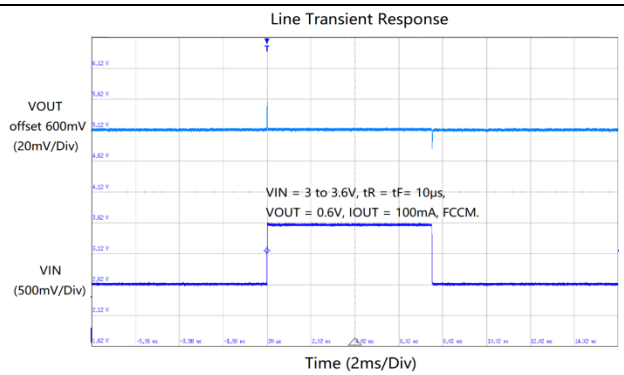


Figure 13. VOUT=0.6V, Line Transient Test

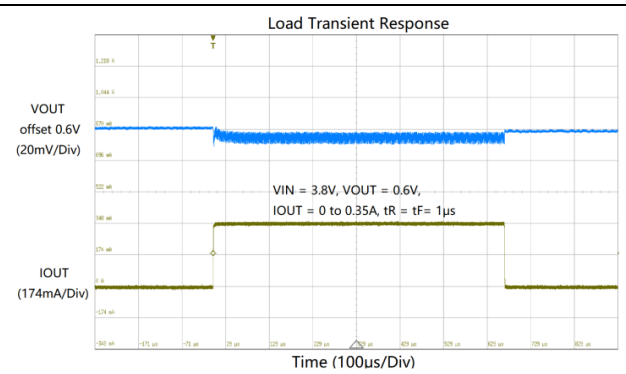


Figure 14. VOUT=0.6V, Load Transient Test

Typical Operating Characteristics(Continued)

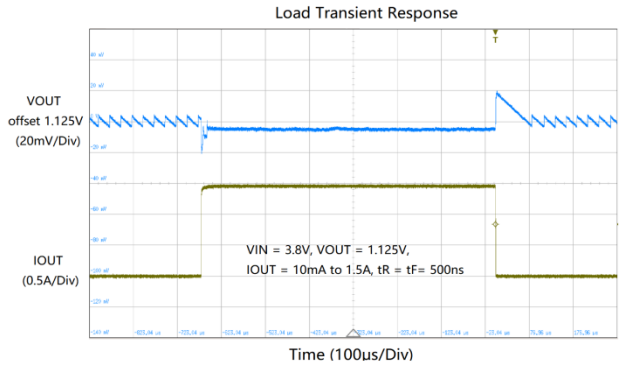


Figure 15. VOUT=1.125V, Load Transient Test

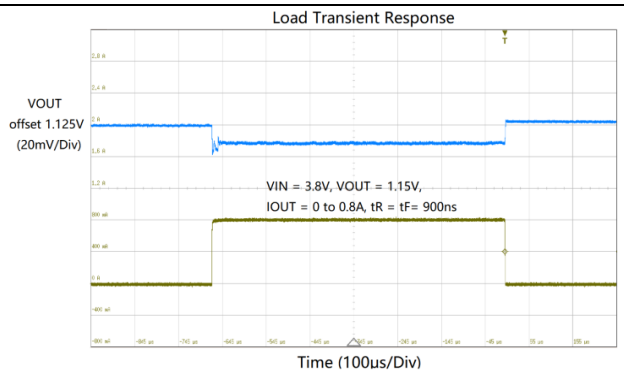


Figure 16. VOUT=1.15V, Load Transient Test

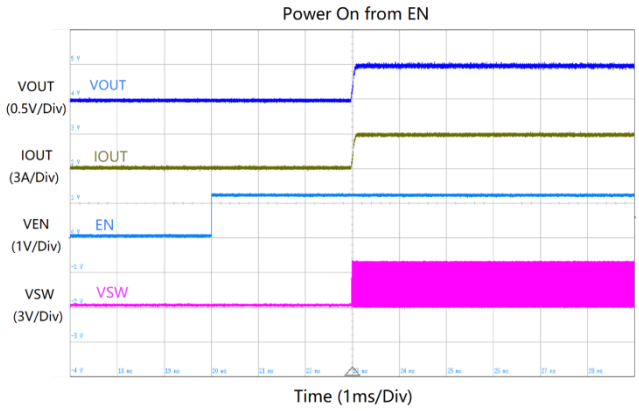


Figure 17. VOUT=0.5V, Power ON Test

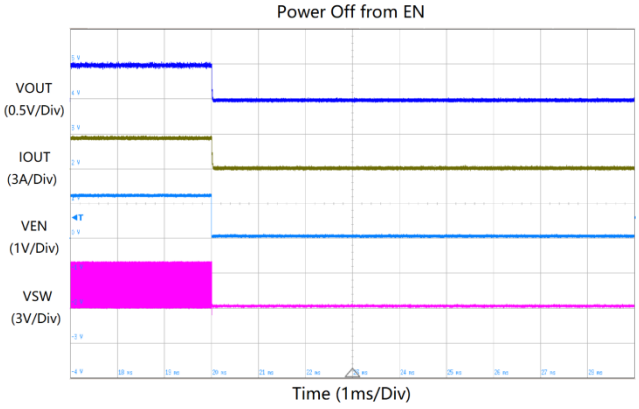


Figure 18. VOUT=0.5V, Power OFF Test

Application Circuit

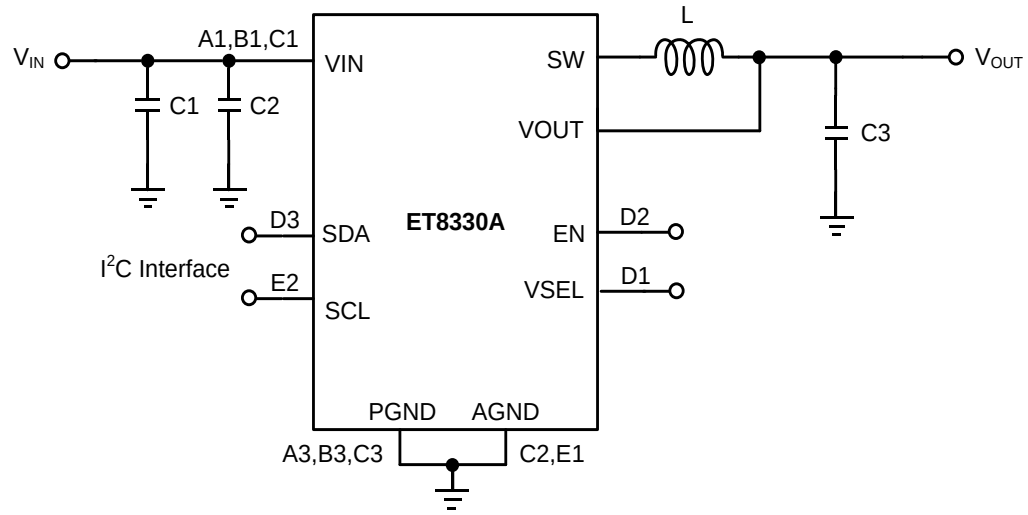


Figure 19. Reference Application Circuit

Component	Value	Size	Vendor
L	470nH	2016	DFE201612E-R47M (muRata)
C_1	10uF / 10V	0603	CL10A106KP8NNNC (SAMSUNG)
C_2	100nF / 10V	0402	CL05B104KO5NNNC (SAMSUNG)
C_3	3*22uF / 6.3V	0603	CL10A226MQ8NRNC (SAMSUNG)

Table 1. Recommended External Components

Application Information

General Descriptions

The typical application circuit is shown in the figure of Application Circuit. External components are recommended in table 1. The external components should be properly chosen in order to achieve desired performance.

Inductor Selection

The current ripple of inductor is determined by input voltage, output voltage, operating frequency and the value of inductor, as shown in below Equation 2:

$$\Delta I_L = \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{f * L} \quad (2)$$

In above equation, f is the operating frequency and L is the inductance. In order to reduce current ripple, the inductor value should be increased.

According to above equation, when VIN is the biggest, the current ripple is the biggest correspondingly. In general, the ripple current ranges from 0.3×I_{MAX} to 0.4×I_{MAX}. To make sure the current ripple is smaller than a specified maximum, the inductor value shouldn't be smaller than below value, Equation 3 :

$$L = \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{f * \Delta I_L} \qquad (3)$$

Input and Output Capacitor Selection

In order to reduce voltage ripple of VIN pin when high side power MOSFET is turned on and off, low ESR input capacitor C_{IN}, is needed to bypass VIN pin.

To meet size or height requirements, several capacitors may also be put in parallel at VIN and VOUT pin. Ceramic capacitors with high voltage rating and low ESR are suitable for switching regulator applications. However, they can also have a high voltage coefficient and audible piezoelectric effects. So the capacitors for VIN pin should be 10V rate, and for V_{OUT} should be 6.3V rate. In order to reduce V_{OUT} ripple and get better load transient performance, 3×22uF or larger capacitors can be used for VOUT pin.

I²C Interface Function

By using I²C interface, the V_{OUT} voltage, Dynamic Voltage Scaling (DVS) slew rate, Auto PFM/PSM or FCCM mode all can be set according to customer's requirement.

The register of each function can be found from the following register map and it also explains how to use these function.

VOUT Selection

The VOUT can be set from 0.5V to 1300mV with 5mV resolution.

The output voltage can be set by NSELx register bit and the output voltage is given by following Equation 4:

$$V_{OUT} = 0.5V + VSELx \times 5mV \qquad (4)$$

For example :

if VSELx = 00111100 (60 decimal), then

V_{OUT} = 0.5 + 60 × 5mV = 0.5 + 0.3 = 0.8V.

The ET8330A also has external VSEL pin to select VSEL1(0x01) or VSEL0(0x00).

Pull VSEL to high is for VSEL1 and pull VSEL to low is for VSEL0. Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

Enable and Soft-Start

When the EN pin is LOW, almost all internal circuits are turned off, and the device consumes very little current. However, if V_{IN} is higher than threshold of Power On Reset (POR), I^2C can also be written to or read from I^2C interface. The registers will be reset when V_{IN} is lower than POR threshold.

When EN pin is high, V_{OUT} will ramp up at the chosen soft-start slew rate which is programmed in the CONTROL2 register ss_sr[1:0] bit.

Raising EN while the vseln_en(n=0,1) bit is HIGH activates the part and begins the soft-start cycle. For the ET8330A, there is 3ms and 2ms delay time from EN HIGH to V_{OUT} start soft-start separately.

Discharge Function

In the CONTROL1 register outdischg bit is set to 1 can let V_{OUT} discharge by internal resistor when converter shuts down. If setting to 0 V_{OUT} will decrease depending on the loading. When EN pin set to low, the ET8330A will default turn on internal 11Ω discharge resistor.

Slew Rate Setting

The slew rate of V_{OUT} can be set, when V_{OUT} changes between two voltage levels. In the CONTROL1 register up_sr[2:0] bits can control up-speed when in the CONTROL2 register dn_sr[1:0] can control down-speed. The default up_sr[2:0] slew rate is 20mV/us and dn_sr[1:0] slew rate is 5mV/us.

Force PWM Mode

In the CONTROL1 register mode_vsel0 and mode_vsel1 can decide converter is always at PWM mode or enters power saving mode at light load condition.

The default operation mode of mode_vsel0 is auto PWM/PFM mode and mode_vsel1 is Continuous PWM mode.

During output voltage is changed from high to low, the ET8330A will make transition operate at PWM mode and output voltage will decrease quickly.

I^2C Interface

Bus Interface

Baseband Processor can transmit data with ET8330A each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is high, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte Format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET8330A will send a low level response signal with one period width to the SDA port. During the reading mode, ET8330A will not send response signal and the host will send a high response signal one period width to the SDA.

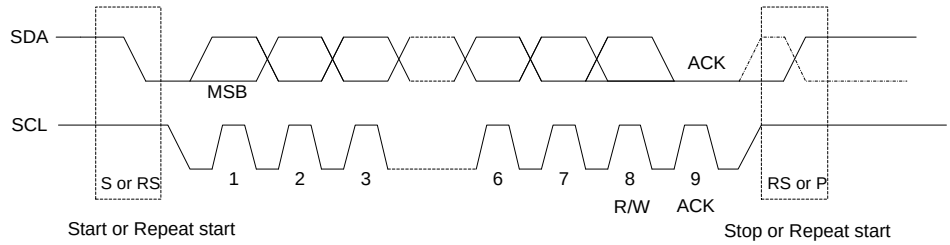


Figure 20. I²C write mode

- ACK = Acknowledge
- MSB = Most Significant Bit
- S = Start Conditions
- RS = Restart Conditions
- P = Stop Conditions
- Restart: SDA-level turnover as expressed by the dashed line waveform

7bit Address for chips

Chip Name	7bit Address
ET8330A	1010000b

I²C Writing Command Register Interface Protocol (continuous)：

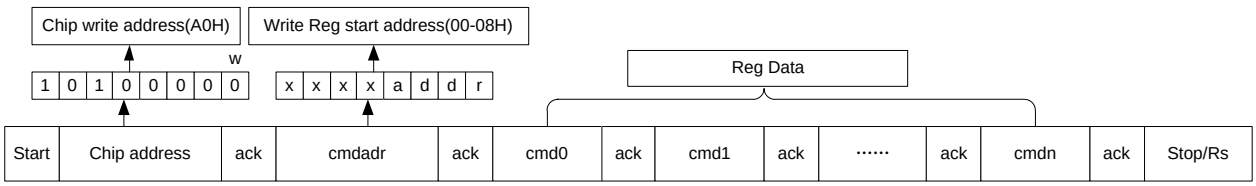


Figure 21. I²C Writing Command Register (continuous)

- Start = Start Conditions
- Chip address = Write register address =1010000+0(w)b
- Ack = Acknowledge
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- Ack = Acknowledge
- Reg data 0 = cmd0(Command data0)
- Ack = Acknowledge
- ……
- Reg data n = cmdn(Command datan)
- Ack = Acknowledge
- Stop/Rs = Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：

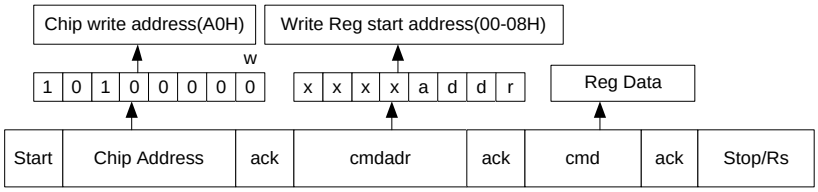


Figure 22. I²C Writing Command Register(single)

- Start = Start Conditions
- Chip address =Write register address=1010000+0(w)b
- Ack = Acknowledge
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- Ack = Acknowledge
- Reg data = cmd(Command data)
- Ack = Acknowledge
- Stop/Rs = Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(continuous):

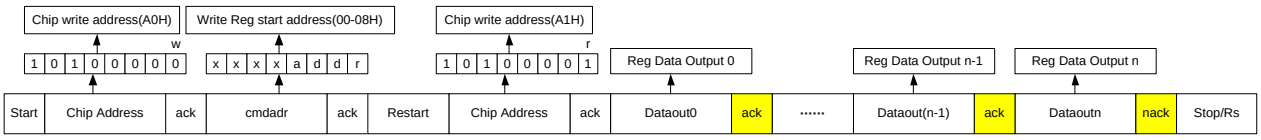


Figure 23. I²C Reading Command Register(continuous)

- Start = Start Conditions
- Chip address = Write register address =1010000+0(w)b
- Ack = Acknowledge from ET8330A
- Write Reg start address byte = cmdadr (xxxx + REG's 4bit addr)
- Ack = Acknowledge from ET8330A
- Restart = Restart condition
- Chip address Read register address =1010000+1(r)b
- Ack = Acknowledge from ET8330A
- Dataout0 = Register data output 0
- Ack = Acknowledge from Host
- ……
- Dataoutn = Register data output n
- Nack = No Acknowledge from Host
- Stop/Rs = Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol:

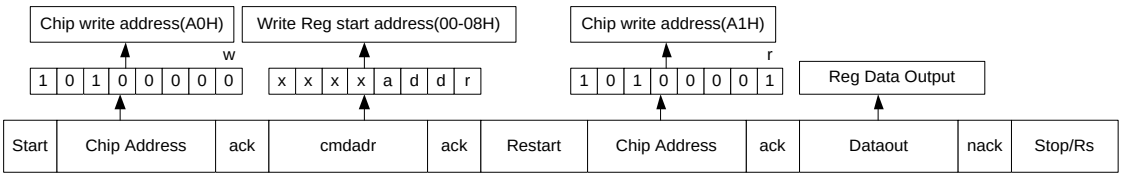


Figure 24. I²C Reading Command Register

- Start = Start Conditions
- Chip address = Write register address = 1010000+0(w)b
- Ack = Acknowledge from ET8330A
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- Ack = Acknowledge from ET8330A
- Restart = Restart condition
- Chip address Read register address = 1010000+1(r)b
- Ack = Acknowledge from ET8330A
- Dataout = Register data output
- Nack = No Acknowledge from Host
- Stop/Rs = Stop Condition/Restart Condition

Register Map

Addr	Name	Descirption							
0x00	VSEL0	vsel0[7:0]							
0x01	VSEL1	vsel1[7:0]							
0x02	CONTRL1	dischg	up_sr[2:0]			0	sw_reset	vsel1_mode	vsel0_mode
0x03	CHIPID	100000						chipid[1:0](01b)	
0x04	VERID	000000						verid[1:0](00b)	
0x05	MONITER	power_ good	uvlo_ sta	ovp_ sta	buck_ vpos	buck_ vneg	reset_ stat	chip_ ovt	buck_ status
0x06	CONTRL2	dn_sr[2:0]			0	ss_sr[1:0]		vsel1_en	vsel0_en
0x07	CONTRL3	00			buck_en_dly[5:0]				
0x08	CONTRL4	00			buck_dis_dly[5:0]				

Table 2: Register Map

Register description

- **0x00 VSEL0 Register---- Output Voltage Setting Register When VSEL Pin Connect Low Level. Default = 0x14**

  Output voltage range is from 0.5V to 1.3V, each step=5mV.

  The register VSEL0 sets the voltage when VSEL=0, it has 161 steps,

  shown as below table 3, the formula is VOUT =0.500V + [d*5mV];

Output Voltage Set by vsel0[7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	0.500
1	00000001	0.505
2	00000010	0.510
3	00000011	0.515
4	00000100	0.520
5	00000101	0.525
……	……	……
20	**00010100(default for ET8330A)**	**0.600**
……	……	……
50	00110010	0.750
……	……	……
125	01111101	1.125
……	……	……
145	10010001	1.225
……	……	……
160	10100000	1.300
161~255	10100001~11111111	Reserved

- **0x01 VSEL1 Register---- Output Voltage Setting Register When VSEL Pin Connect High Level. Default = 0x14**

  Output voltage range is from 0.5V to 1.3V, each step=5mV.
  The register VSEL1 sets the voltage when VSEL=1, it has 161 steps,
  shown as below table 4, the formula is VOUT =0.500V + [d*5mV];

Output Voltage Set by vsel1[7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	0.500
1	00000001	0.505
2	00000010	0.510
3	00000011	0.515
4	00000100	0.520
5	00000101	0.525
……	……	……
20	**00010100(default for ET8330A)**	**0.600**
……	……	……
50	00110010	0.750
……	……	……
125	01111101	1.125
……	……	……
145	10010001	1.225
……	……	……
160	10100000	1.300
161~255	10100001~11111111	Reserved

- **0x02 CONTROL1 Register---- Control Register Default = 0x92 ,** shown as below table 5.

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7</td><td>outdischg</td><td>1</td><td>R/W</td><td>Output Discharge Enabled/Disabled Control:
0b: Disabled
1b: Enabled</td></tr>
<tr><td>6:4</td><td>up_sr[2:0]</td><td>001</td><td>R/W</td><td>Output Voltage rising DVS step setting control:
<table>
<tr><th>Register Value</th><th>DVS step</th></tr>
<tr><td>000</td><td>40mv/us</td></tr>
<tr><td>001</td><td>20mv/us</td></tr>
<tr><td>010</td><td>10mv/us</td></tr>
<tr><td>011</td><td>5mv/us</td></tr>
<tr><td>100</td><td>2.5mv/us</td></tr>
<tr><td>101</td><td>1.25mv/us</td></tr>
<tr><td>110</td><td>0.625mv/us</td></tr>
<tr><td>111</td><td>0.3125mv/us</td></tr>
</table></td></tr>
<tr><td>3</td><td>Rev.</td><td>0</td><td>R</td><td>Reserved</td></tr>
</table>

2	sw_reset	0	R/W	Register Software Reset Control 1b:Reset 0b:auto clear after reset
1	mode_vsel1	1	R/W	Buck Mode Setting Control When VSEL Pin Connect High Level: 0b:Auto PWM/PFM conversion mode 1b:Continuous PWM mode
0	mode_vsel0	0	R/W	Buck Mode Setting Control When VSEL Pin Connect Low Level: 0b:Auto PWM/PFM conversion mode 1b:Continuous PWM mode

- **0x03 CHIPID Register---- Indicates the Product ID. Default = 0x81**

  die_id[1:0] Indicates the die ID. Read only. shown as below table 6.

Bit	Name	Default	Type	Description
7:2	default	100000	R	Default
1:0	chipid	01	R	Chip Identity

- **0x04 VERID Register---- Indicates the Die version ID. Default = 0x00**

  ver_id[1:0] Indicates the die version ID. Read only. shown as below table 7.

Bit	Name	Default	Type	Description
7:2	default	000000	R	Default
1:0	verid	00	R	Version Identity

- **0x05 MONITER Register ----Buck Status Register. Default = 0x00 ,** shown as below table 8.

Bit	Name	Default	Type	Description
7	power_good	0	R	Buck Enabled and Soft-start Completed Status: 0b:not start 1b:start
6	uvlo_sta	0	R	VIN Under Voltage Status: 0b:not under voltage 1b:under voltage
5	ovp_sta	0	R	VIN Over Voltage Status: 0b:not over voltage 1b:over voltage
4	buck_vpos	0	R	Voltage Posedge Progress Status: 0b:not in progress 1b:in progress
3	buck_vneg	0	R	Voltage Negedge Progress Status: 0b:not in progress 1b:in progress
2	reset_stat	0	R	Software Restart Occurrence Status, Auto Clear: 0b:not occur 1b:occured

1	chip_ovt	0	R	Over Temperature Status: 0b:not over temperature 1b:over temperature
0	buck_status	0	R	Buck Enabled/Disabled Status: 0b:Disabled 1b:Enabled

- **0x06 CONTROL2 Register---- Control register Default = 0x63.** shown as below table 9.

Bit	Name	Default	Type	Description
7:5	dn_sr[2:0]	011	R/W	Output Voltage Falling DVS Step Setting Control: Register Value / DVS step 000 / 40mv/us 001 / 20mv/us 010 / 10mv/us 011 / 5mv/us 100 / 2.5mv/us 101 / 1.25mv/us 110 / 0.625mv/us 111 / 0.3125mv/us
4	Rev.	0	R	Reserved
3:2	ss_sr[1:0]	00	R/W	Soft-start Time Setting Control: Register Value / Soft-start time 00 / 100us 01 / 200us 10 / 400us 11 / 800us
1	en_vsel1	1	R/W	Buck Enabled/Disabled Control When VSEL Pin Connect High Level: 0b:Disabled 1b:Enabled
0	en_vsel0	1	R/W	Buck Enabled/Disabled Control When VSEL Pin Connect Low Level: 0b:Disabled 1b:Enabled

- **0x07 CONTROL3 Register----Buck Enable Delay Time Set Register**

  buck_en_dly[5:0] set the delay time of starting Buck after EN or en_vseln sets(n=0,1)

  Delay time ranging from 0 to 63ms, step=1ms

  The register CONTROL3 set the delay time of starting BUCK after EN or en_vseln sets(n=0,1), it has 64steps, shown as below table 10, the formula is delay time = d*1ms;

BUCK Enable Delay Time Set by buck_en_dly[5:0]		
Dec	**Binary**	**Delay Time(ms)**
0	000000	0
1	000001	1
2	000010	2
3	**000011(default for ET8330A)**	**3**
4	000100	4
5	000101	5
……	……	……
62	111110	62
63	111111	63

- **0x08 CONTROL4 Register---- Buck Disable Delay Time Set Register**

  buck_dis_dly[5:0] set the delay time of stopping Buck after EN or en_vseln sets(n=0,1)

  Delay time ranging from 0 to 63ms, step=1ms

  The register CONTROL3 set the delay time of starting Buck after EN or en_vseln sets(n=0,1), it has 64steps, shown as below table 11, the formula is delay time = d*1ms;

Buck Disable Delay Time Set by buck_dis_dly[5:0]		
Dec	**Binary**	**Delay Time(ms)**
0	**000000(default for ET8330A)**	**0**
1	000001	1
2	000010	2
3	000011	3
4	000100	4
5	000101	5
……	……	……
62	111110	62
63	111111	63

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following Equation 5:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \quad (5)$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WLCSP15 1.15mm×1.95mm package, the thermal resistance, θ_{JA}, is 42°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$= (125°C-25°C) / (42°C/W) = 2.38W for a WLCSP15 1.15mm×1.95mm package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in below Figure allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

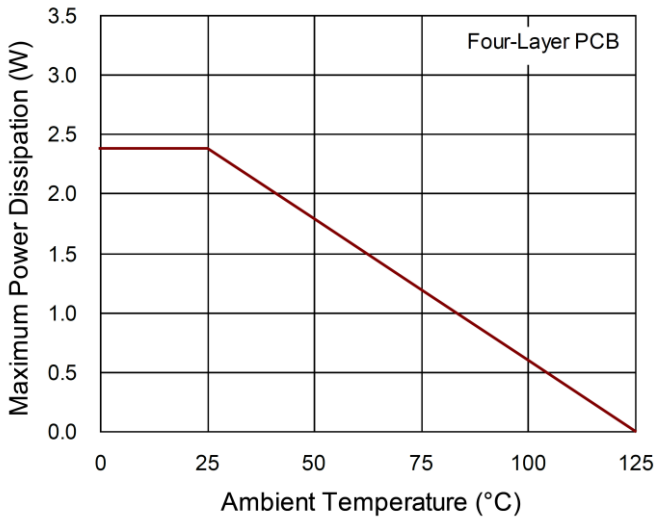


Figure 25. Derating curve of maximum power dissipation

Layout Considerations

For best performance of the ET8330A, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to IC to minimize the power loop area. A typical 0.1uF decouple capacitor is recommended to reduce power loop area and any high frequency component on V_{IN}.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- The AGND pin is suggested to connect to 2nd GND plate through top to 2nd via.

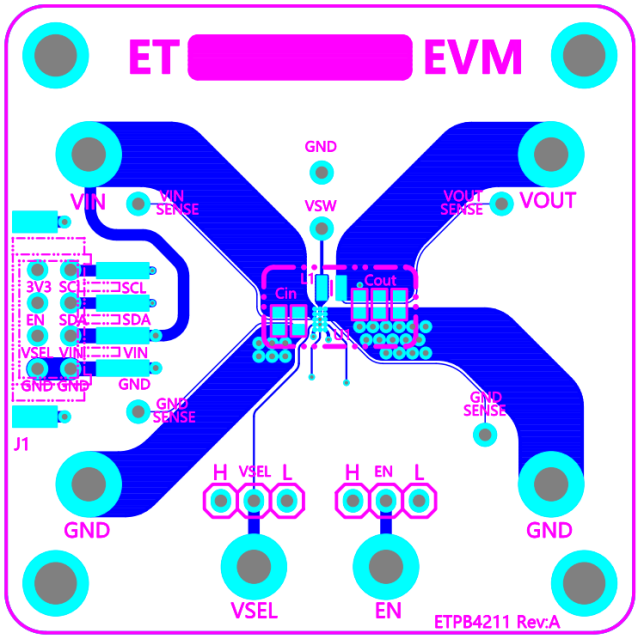
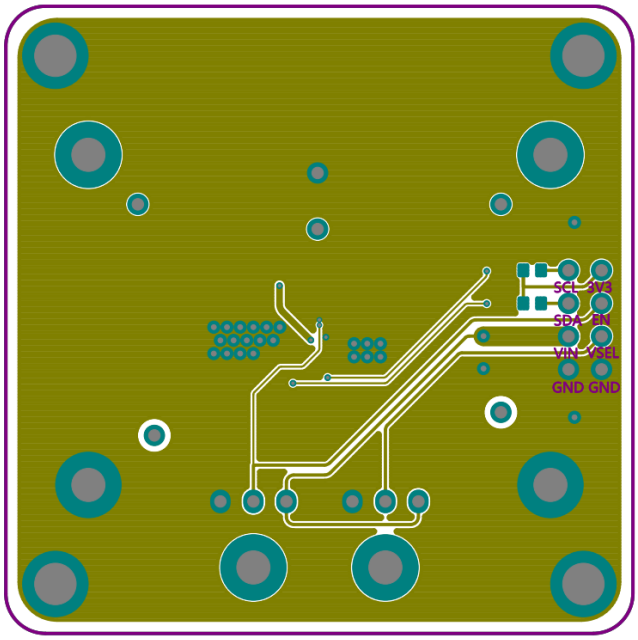
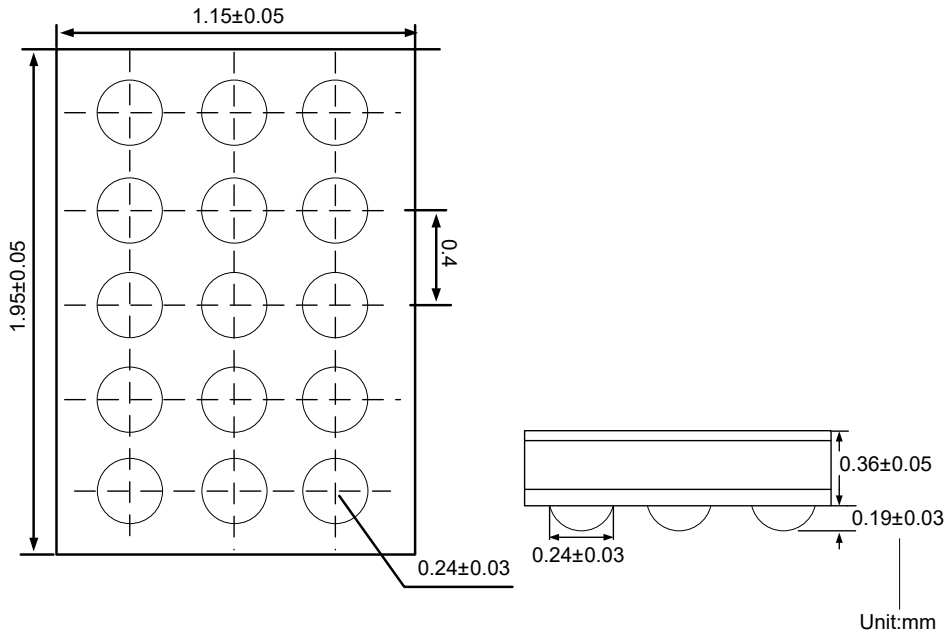
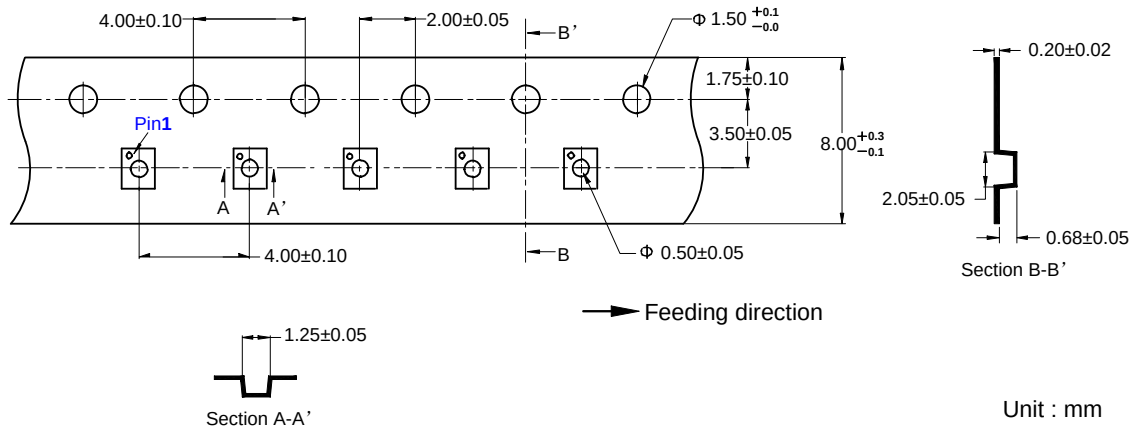
ET8330A PCB Layout Guide	
Top Layer	**Bottom Layer**
	

Figure 26. PCB layout guide

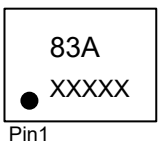
Package Dimension



Tape Information



Marking



83A- Part Number

XXXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2021-6-7	Initial Version	Xielh	Xielh	Zhujl
1.1	2021-10-12	Update Package Dimension	Xielh	Xielh	Zhujl
1.2	2021-11-8	Update V_{OUT} vs Temperature graph	Xielh	Xielh	Zhujl
1.3	2023-1-31	Update Typeset	Shibo	Xielh	Liujy
1.4	2023-3-22	VIH to 0.9V	Shibo	Xielh	Liujy
1.5	2023-6-22	Update Typical Operating Characteristics	Shibo	Xielh	Liujy
1.6	2023-7-14	Inductance determined to 470nH	Shibo	Xielh	Liujy