4.5V to 17V Input, 2A Synchronous Step-Down Regulator

General Description

The ET8123 is a highly integrated, wide input voltage, 2A output synchronous buck converter.

The device is optimized to operate with minimum external component counts and also optimized to achieve low standby current.

This converter adopts adaptive constant-on-time (ACOT) structure, and provides a fast transient response. It also supports both low-equivalent series resistance (ESR) output capacitors and ultra-low ESR ceramic capacitors with no external compensation components.

During light load operation, ET8123 operates in pulse frequency modulation (PFM) mode, which maintains high efficiency.

ET8123 is available in a small SOT-563 package.

Features

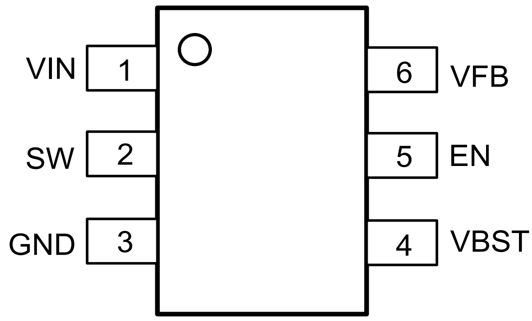
- 2A Converters Integrated 100mΩ and 55mΩ FET
- ACOT mode control with fast transient response
- Input Voltage Range: 4.5V to 17V
- Output Voltage Range: 0.8V to 7V
- PFM mode during light load operation
- 800KHz Switching Frequency
- Low Shutdown Current Less than 5μA
- Start-up from Pre-Biased Output Voltage
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.2ms
- Part No. and Package

Part No.	Package
ET8123	SOT-563

Application

- Digital TV Power Supply and Surveillance
- Disc Players
- Networking Home Terminal
- Digital Set Top Box

Pin Configuration

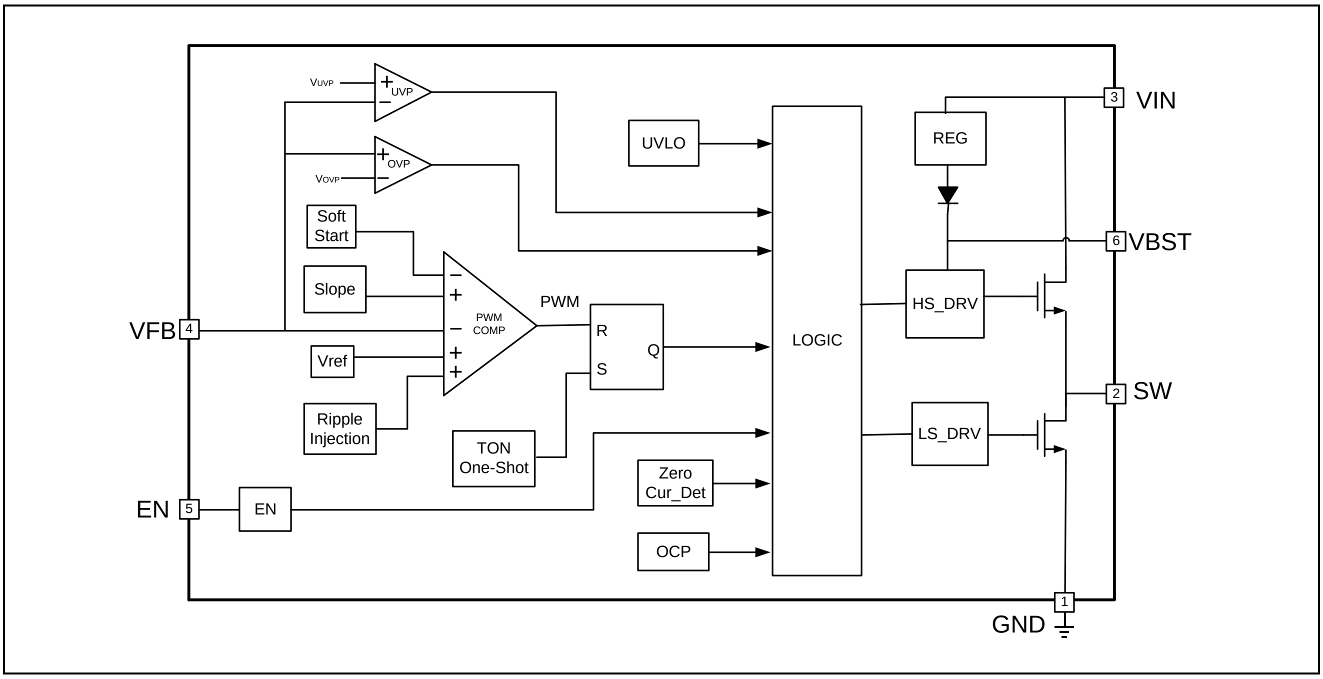


Top View

Pin Function

Pin Name	Pin No.	I/O	Description
VIN	1	I	Input voltage supply pin, also the drain terminal of high-side power NFET.
SW	2	O	Switch node connection between low-side NFET and high-side NFET.
GND	3		Ground pin of controller circuit, as well as source terminal of low-side power NFET. Connect sensitive VFB to this GND at a single point.
VBST	4	O	Power supply of high-side NFET control circuit. Connect 0.1μF capacitor between VBST and SW pins.
EN	5	I	Enable pin. Must be pulled up to enable the device.
VFB	6	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.

Block Diagram



Functional Description

Overview

The ET8123 is highly integrated, 2A synchronous buck converter. It employs adaptive constant on time (ACOT) mode, and supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of this device can reduce the output capacitance.

Adaptive On-Time Control and PWM Operation

The main control mode of ET8123 is pulse width modulation (PWM) with ACOT structure. This control mode control can achieve pseudo-fixed frequency and stable operation with both low-ESR and ceramic output capacitors.

The high-side MOSFET is turned on at the beginning of each cycle. When one shot timer expires, the high-side power FET is turned off. This one shot duration is set proportional to input voltage (VIN) and inversely proportional to the output voltage (VO) to achieve pseudo-fixed frequency over the input voltage range, hence it is called adaptive constant on-time control. The one-shot timer is reset and the high-side power FET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is generated to emulate output ripple, eliminating the need for ESR of output capacitor.

Pulse Frequency modulation

The ET8123 is designed with pulse frequency modulation mode to achieve high efficiency during light load condition. As the output current decreases from heavy load condition, the inductor current also deceases and eventually comes to zero, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side power FET is turned off when the zero inductor current is detected. As the load current further decreases the convertor enters into discontinuous conduction mode. The on-time is almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps efficiency high in light load condition. The transition point to the light load operation IOUT(LL) current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{sw}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \qquad (1)$$

In PFM mode, each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the threshold voltage. As the output current decreases, the sleep time between switching pulses increases.

Soft Start and Pre-Biased Soft Start

The ET8123 is designed with an internal 1.2ms soft-start. When the VIN is plugged in and the EN pin becomes high, the reference voltage of PWM comparator begins to rise from zero.

If the output capacitor is pre-biased at start-up, the device begins to switch and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

Current Protection

The over-current limit (OCL) is implemented by using cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET drain to source voltage during its on-state. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-state of high-side FET, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, and the inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter keeps low-side FET on and prevents the creation of a new set pulse, even the voltage feedback loop requires one, until the current level decreases to OCL level or lower. In next switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the load current is higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time and re-start after the hiccup time (typically 12ms).When the over current condition is removed, the output voltage returns to the regulated value.

Under-voltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Thermal Shutdown

The device monitors the temperature of itself. If temperature exceeds the threshold value (typically 170° C), the device is shut off. When the temperature falls to about 140°C or below, the converter begins to switch.

Standby Operation

When the ET8123 is operating in either normal CCM or PFM, they may be placed in standby by pulling the EN pin to low.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters		Min	Max	Unit
V_{IN}	Input Port Voltage	VIN, EN	-0.3	19	V
		VBST	-0.3	24	V
		VBST (10ns transient)	-0.3	25	V
		VBST (VS SW)	-0.3	6.5	V
		VFB	-0.3	6.5	V
		SW	-2	19	V
		SW (10ns transient)	-3.5	20	V
V_{ESD}	Human Body Model (JEDEC JS-001)			±2000	V
	Charged Device Model (JESD22-C101)			±1000	V
$R_{\theta JA}$	Junction-to-ambient thermal resistance			150	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			75	°C/W
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters		Min	Max	Unit
V_{IN}	Supply Input Voltage Range		4.5	17	V
V_I	Input Voltage Range	VBST	-0.1	22	
		VBST (10ns transient)	-0.1	25	
		VBST (VS SW)	-0.1	6	
		EN	-0.1	17	
		VFB	-0.1	5.5	
		SW	-1.8	18	
		SW (10ns transient)	-3.5	20	
T_J	Operating Junction Temperature		-40	125	°C
T_A	Ambient Temperature		-40	85	°C

Electrical Characteristics

V_{IN} = 12V, T_A = -40°C to 85°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{VIN}	Operating–non-switching Supply Current	V_{IN} current, V_{EN} = 5V, V_{FB} = 0.9V		200	280	μA
I_{VINSDN}	Shutdown supply current	V_{IN} current, V_{EN} = 0V		1.6	5	μA
Logic Threshold						
V_{ENH}	EN High-level Input Voltage	To make sure the device is enabled	1.14	1.2	1.26	V
V_{ENL}	EN Low-level Input Voltage	To make sure the device is disabled	1.04	1.1	1.16	V
V_{EN_HYS}	EN Hysteresis Voltage	V_{ENH} - V_{ENL}		100		mV
I_{EN}	EN Input Current	V_{IN} = 12V, V_{EN} = 12V	2	3.5	5	uA
V_{FB} Voltage and Discharge Resistance						
V_{FBTH}	V_{FB} Threshold Voltage	V_{OUT} = 1.0V, I_{OUT} = 10mA, PFM operation		808		mV
V_{FBTH}	V_{FB} Threshold Voltage	V_{OUT} = 1.0V, Continuous mode operation	784	800	816	mV
I_{VFB}	VFB pin Input Current	V_{FB} = 0.8V			0.1	μA
MOSFET						
$R_{DS(ON)H}$	High-side Switch Resistance	T_A = 25°C, V_{BST} – V_{SW} = 5V		100		mΩ
$R_{DS(ON)L}$	Low-side Switch Resistance	T_A = 25°C		55		mΩ
Current Limit						
I_{OCL}	Current Limit	DC current, V_{OUT} = 1.0V, L_1 = 2.2μH	2.5	3.5	4.5	A
Thermal Shutdown						
T_{SDN}	Thermal Shutdown Threshold (1)	Shutdown temperature		170		°C
T_{SDN}	Thermal Shutdown Threshold (1)	Hysteresis		30		°C
ON-Time Timer Control						
$t_{OFF(MIN)}$	Minimum off Time	V_{FB} = 0.5V		110		ns
Soft Start						
t_{SS}	Soft Start Time	Internal soft-start time		1.2		ms
Frequency						
F_{SW}	Switching Frequency	V_{IN} = 12V, V_O = 1.0V, CCM mode	600	800	1000	KHz

Electrical Characteristics(Continued)

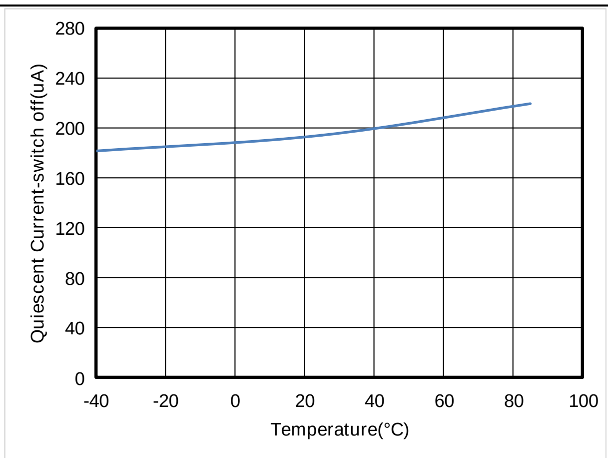
V_{IN} = 12V, T_A = -40°C to 85°C, (unless otherwise noted)

Output Under-voltage and Over-voltage Protection						
V_{UVP}	Output UVP Threshold	Hiccup detect (H > L)		64		%
t_{HICCUP_WAIT}	Hiccup on Time			1.4		ms
t_{HICCUP_RE}	Hiccup Time Before Restart			12		ms
UVLO						
V_{UVLO}	UVLO Threshold	Wake up V_{IN} voltage	3.8	4.1	4.3	V
		Shutdown V_{IN} voltage	3.3	3.6	3.8	
		Hysteresis V_{IN} voltage		0.5		

Note(1). Not production tested, design assurance.

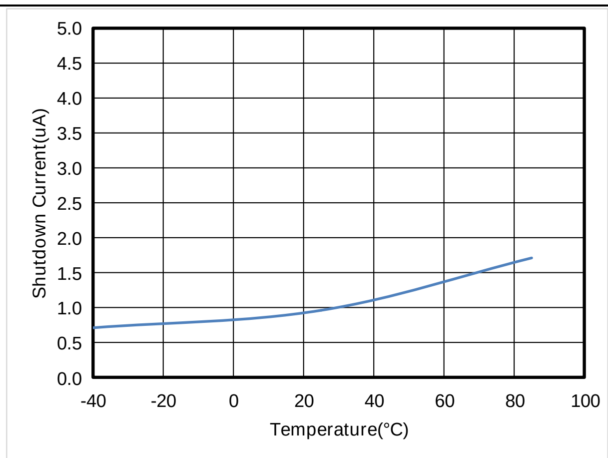
Typical Characteristics

V_{IN} = 12V (unless otherwise noted)



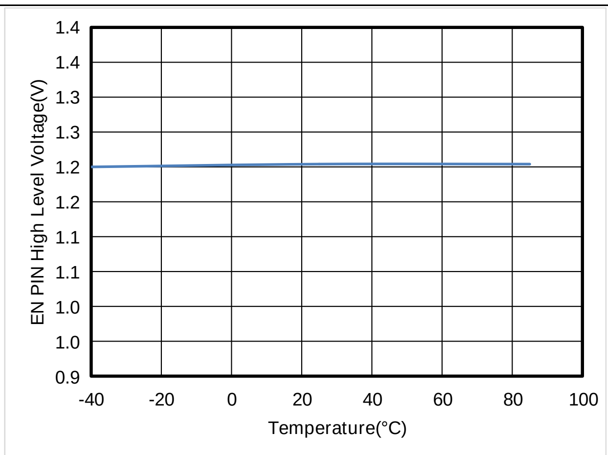
I_{OUT}=0mA

Figure1. ET8123 Quiescent current vs Temperature



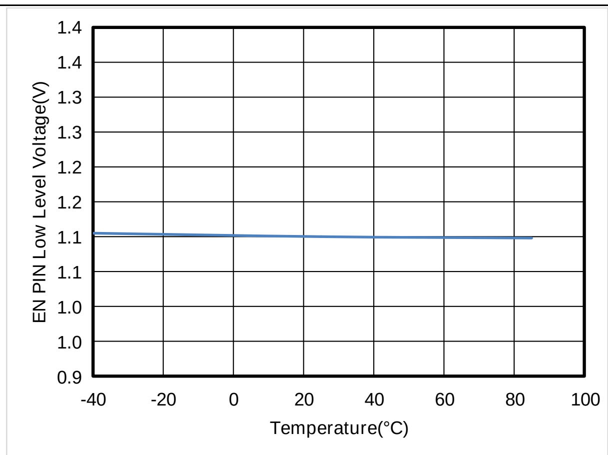
EN=L

Figure2. ET8123 Shutdown current vs Temperature



I_{OUT}=0mA

Figure3. ET8123 EN_H vs Temperature

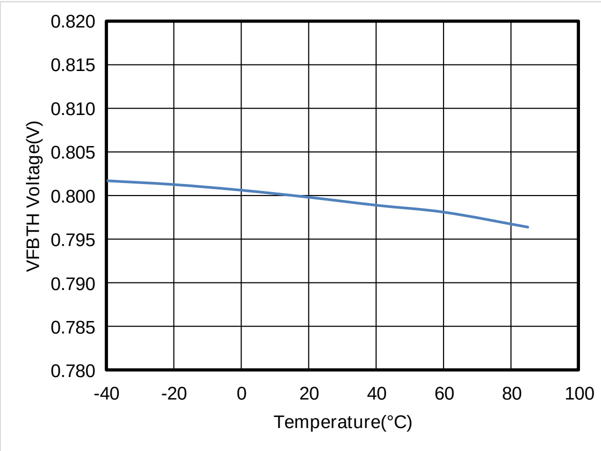


I_{OUT}=0mA

Figure4. ET8123 EN_L vs Temperature

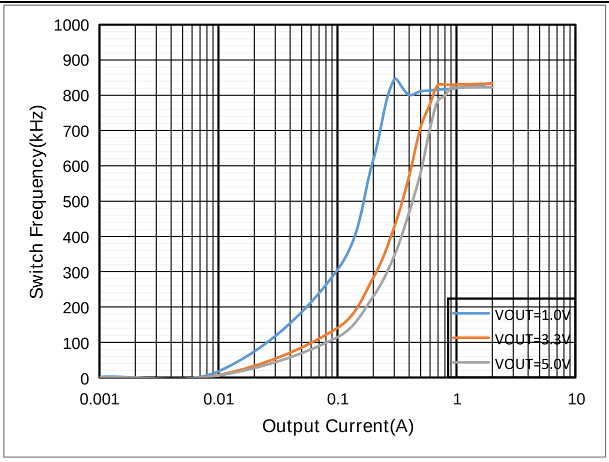
Typical Characteristics(Continued)

V_{IN} = 12V (unless otherwise noted)



I_{OUT}=1000mA

Figure5. ET8123 VFB Voltage vs Temperature



I_{OUT}=2000mA

Figure6. ET8123 Switch Frequency vs input Voltage

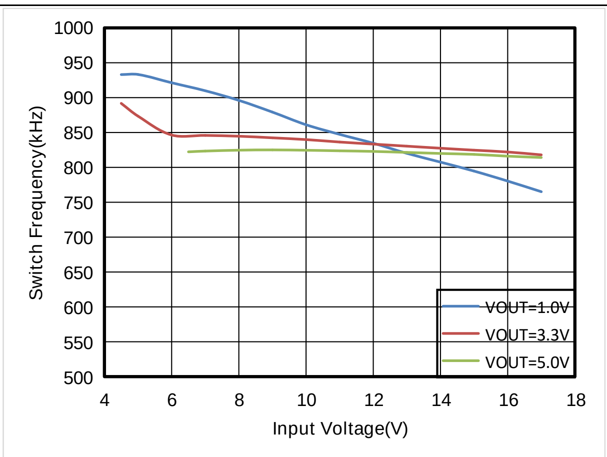
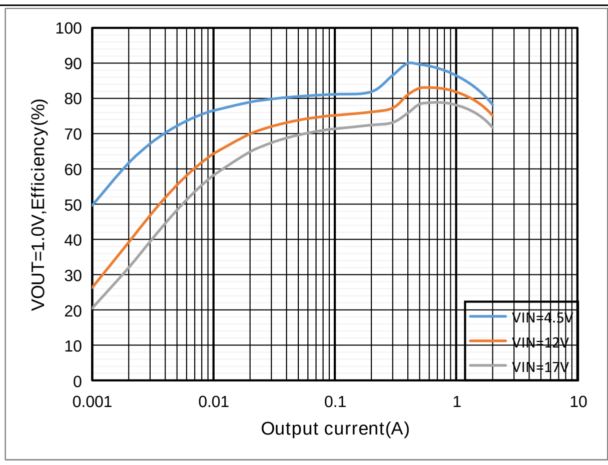
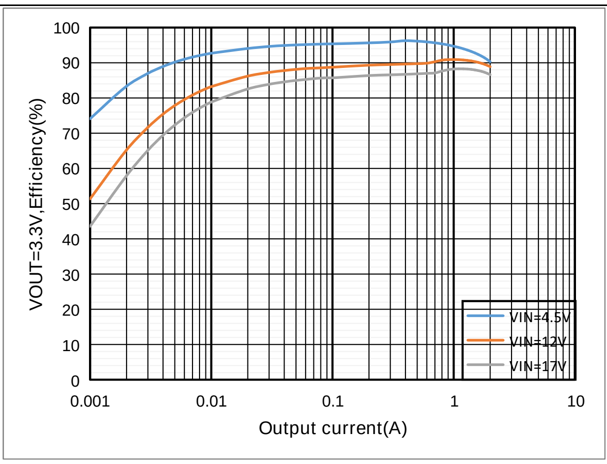


Figure7. ET8123 Switch Frequency vs Output Current



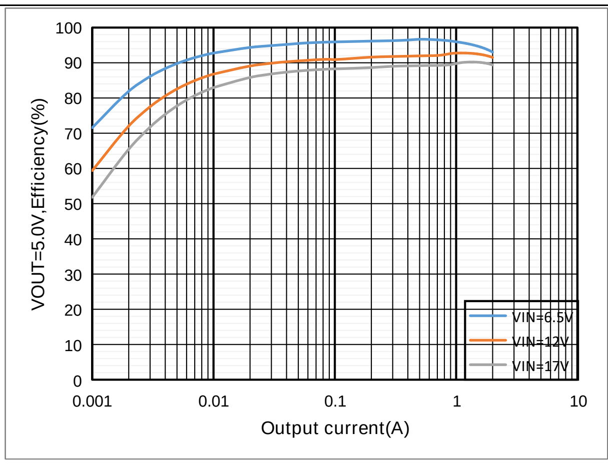
V_{OUT}=1.0V L=2.2uH

Figure8. ET8123 Efficiency vs Output Current



V_{OUT}=3.3V L=2.2uH

Figure9. ET8123 Efficiency vs Output Current



V_{OUT}=5.0V L=2.2uH

Figure10. ET8123 Efficiency vs Output Current

Application and Implementation

Note

ETEK don't warrant its accuracy or completeness and Information in the following applications sections is not part of the ETEK component specification. Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

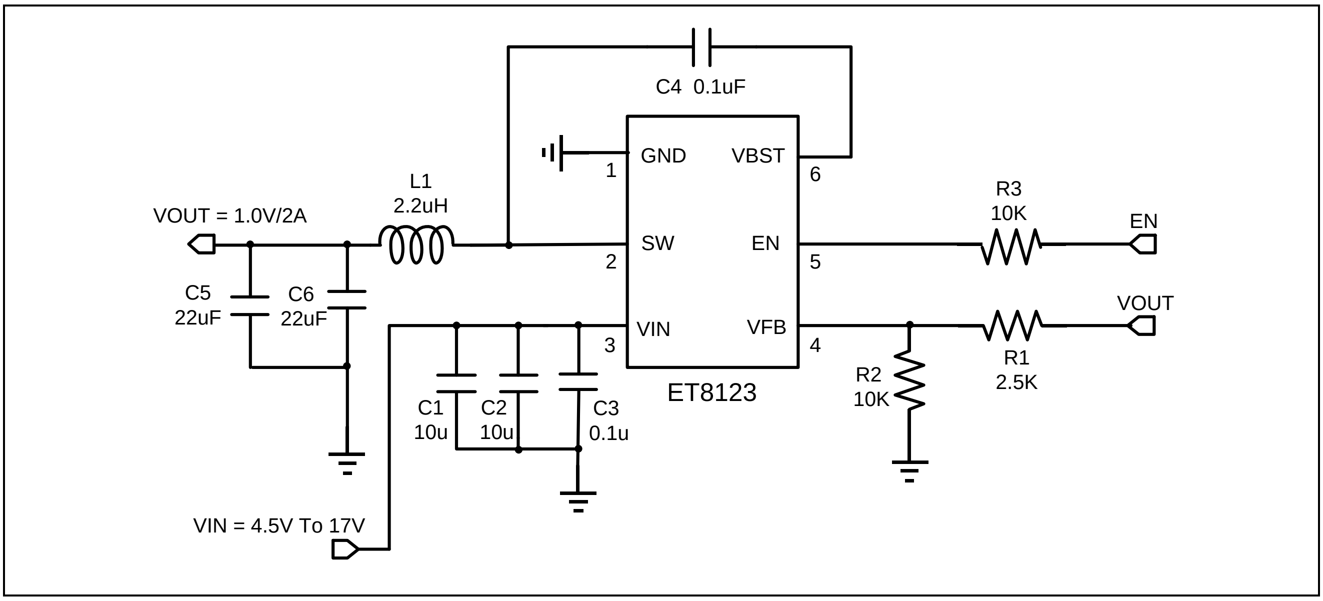
Application Information

ET8123 is typical step-down DC-DC converter. It's typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 2A. The following design procedure can be used to select component values for the ET8123.

Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The figure shows ET8123 4.5V to 17V input, 1.0V output converter schematics.



VOUT = 1.0V / 2 A Reference Design

Design Requirements

This table below shows the design parameters for this application.Table1.

Parameter	Example Value
Input voltage range	4.5 to 17V
Output voltage	1.0V
Transient response, 1.5A load step	ΔV_{OUT} = ±2.5 %
Input ripple voltage	400mV
Output ripple voltage	30mV
Output current rating	2A
Operating frequency	800KHz

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. ETEK recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate VOUT.

If customers want to improve efficiency at very light loads， we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.8 \times (1 + \frac{R1}{R2}) \quad (2)$$

Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

The overall loop gain is set by the output set-point resistor divider network and the internal gain of the device at low frequencies. The low frequency phase is 180° . At the output filter pole frequency, the gain rolls off at a -40dB per decade rate and the phase drops rapidly. The inductor and capacitor for the output filter should be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C5 + C6 (μF)
			Min	Typ	Max	
1.0	2.5	10.0	1.5	2.2	4.7	20 to 68
1.2	5	10.0	1.5	2.2	4.7	20 to 68
1.5	8.75	10.0	1.5	2.2	4.7	20 to 68
1.8	12.5	10.0	1.5	2.2	4.7	20 to 68
2.5	21.25	10.0	2.2	2.2	4.7	20 to 68
3.3	31.25	10.0	2.2	2.2	4.7	20 to 68
5.0	52.5	10.0	3.3	3.3	4.7	20 to 68
6.5	71.25	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4,Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$Il_{p\text{-}p} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{sw}} \quad (4)$$

$$II_{peak} = I_O + \frac{II_{p\text{-}p}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O{}^2 + \frac{1}{12} II_{P-P}{}^2} \quad (6)$$

For this design example, the calculated peak current is 2.4A and the calculated RMS current is 2.01A.

The capacitor value and ESR determines the amount of output voltage ripple. The ET8123 is intended for use with ceramic or other low ESR capacitors. We recommend using values range from 20uF to 68uF. Equation 7 determines the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{sw}} \quad (7)$$

Two 22μF output capacitors are used for this design. The typical ESR is 2mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 3A.

Input Capacitor Selection

The ET8123 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. We recommend a ceramic capacitor over 10uF for the decoupling capacitor. An additional 0.1uF capacitor (C3) from VIN pin to GND is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1uF ceramic capacitor must be connected between the VBST to SW pin for proper operation. We recommend using a ceramic capacitor.

Power Supply Recommendations

ET8123 is designed to operate from input supply voltage in the range of 4.5V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_{OUT}/0.75.

Application Curves

V_{IN} = 12V (unless otherwise noted)

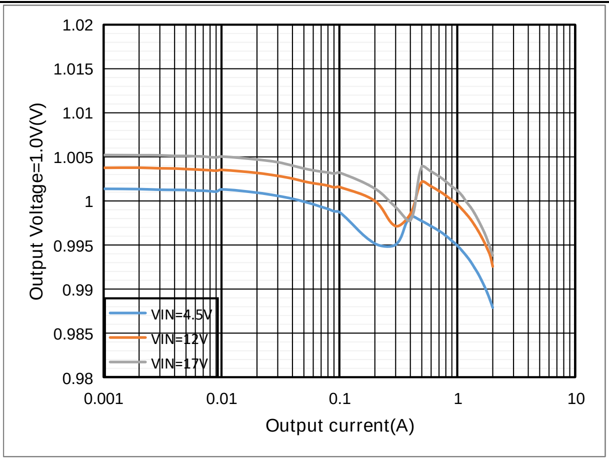


Figure11. ET8123 Load Regulation,V_{OUT}=1.0V

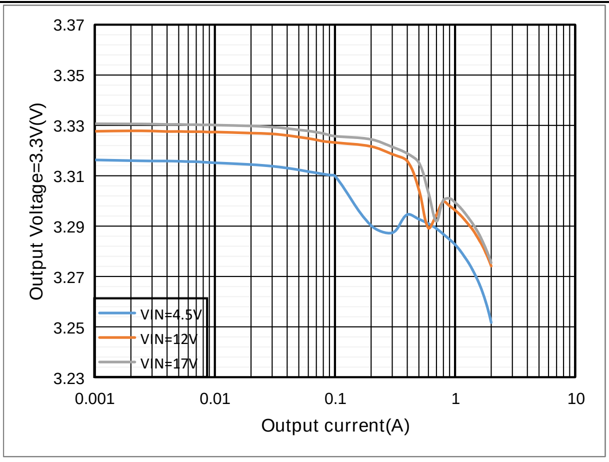


Figure12. ET8123 Load Regulation,V_{OUT}=3.3V

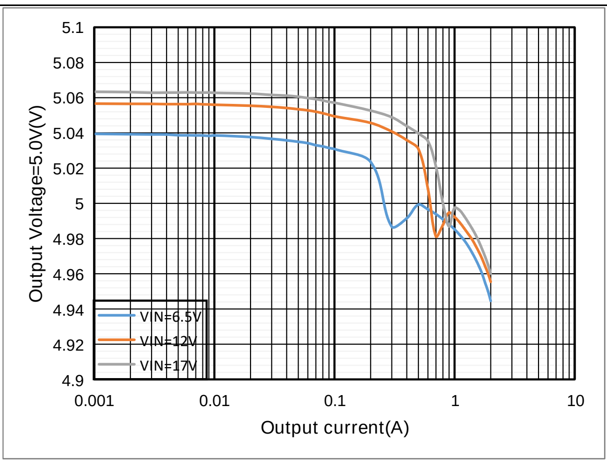


Figure13. ET8123 Load Regulation, V_{OUT}=5.0V

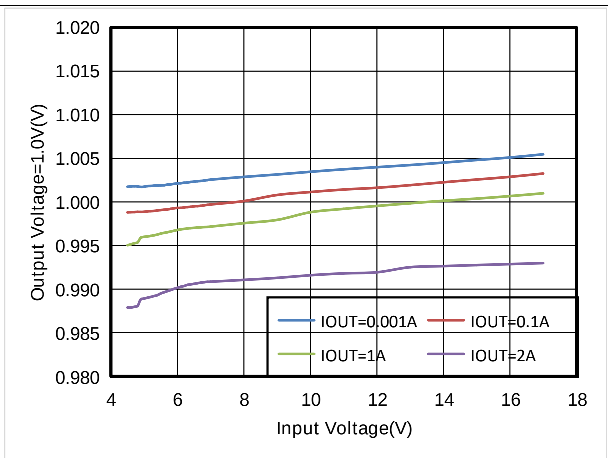


Figure14. ET8123 Line Regulation,V_{OUT}=1.0V

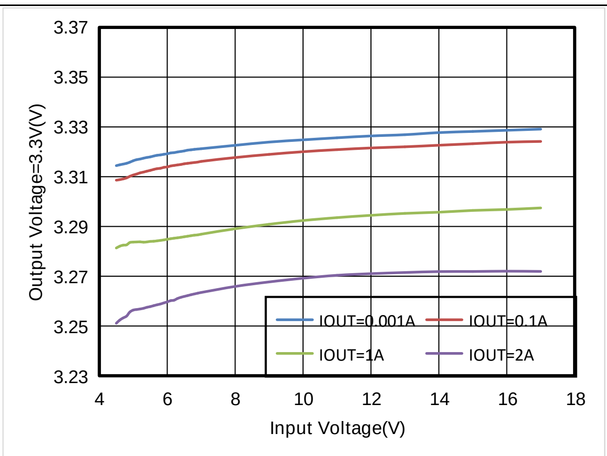


Figure15. ET8123 Line Regulation,V_{OUT}=3.3V

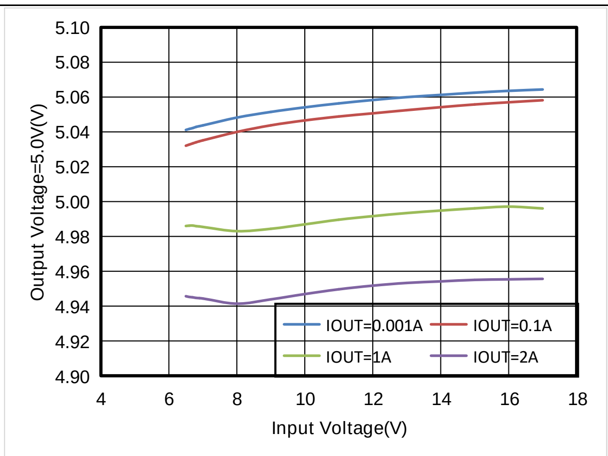
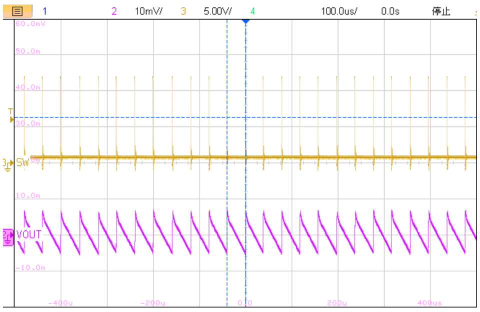


Figure16. ET8123 Line Regulation,V_{OUT}=5.0V

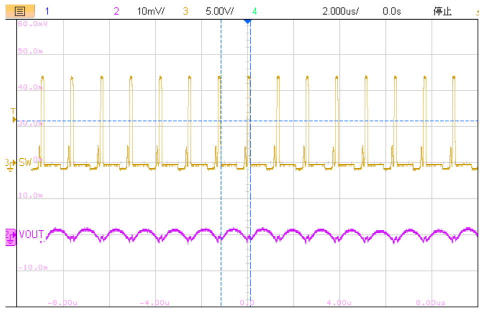
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



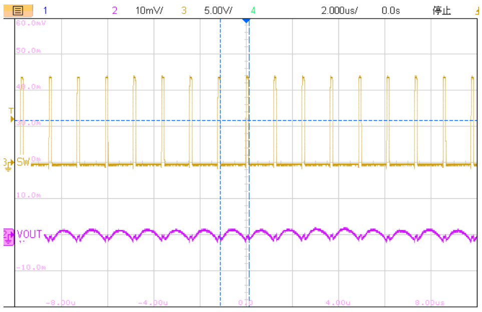
100us/div, V_{OUT}=1.0V I_{OUT}=10mA

Figure17. ET8123 Output Ripple



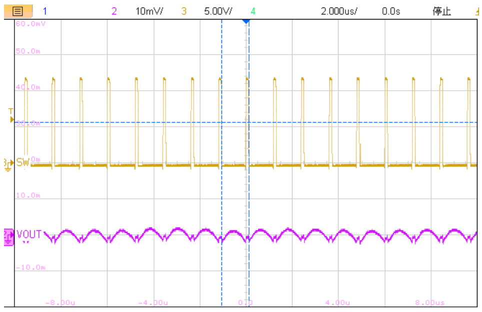
2us/div, V_{OUT}=1.0V I_{OUT}=250mA

Figure18. ET8123 Output Ripple



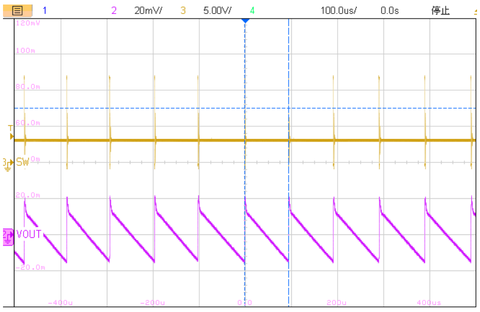
2us/div, V_{OUT}=1.0V I_{OUT}=1A

Figure19. ET8123 Output Ripple



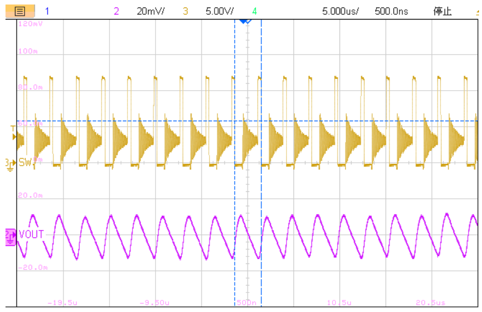
2us/div, V_{OUT}=1.0V I_{OUT}=2A

Figure20. ET8123 Output Ripple



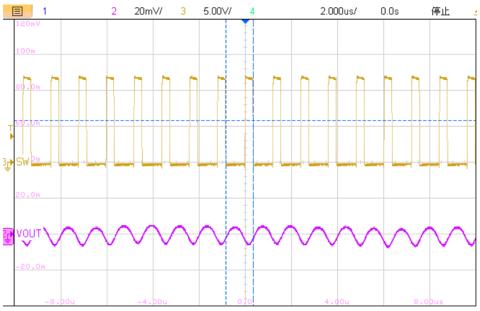
100us/div, V_{OUT}=3.3V I_{OUT}=10mA

Figure21. ET8123 Output Ripple



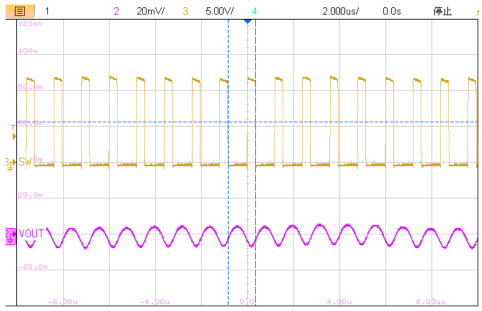
5us/div, V_{OUT}=3.3V I_{OUT}=250mA

Figure22. ET8123 Output Ripple



2us/div, V_{OUT}=3.3V I_{OUT}=1A

Figure23. ET8123 Output Ripple

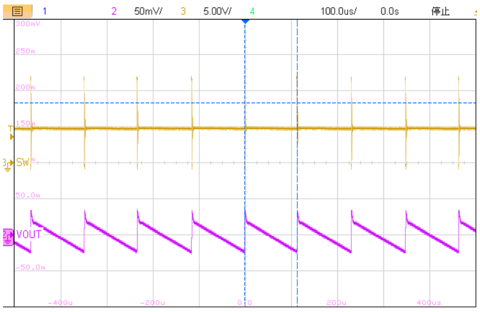


2us/div, V_{OUT}=3.3V I_{OUT}=2A

Figure24. ET8123 Output Ripple

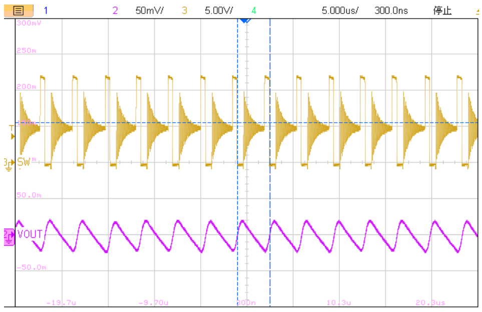
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



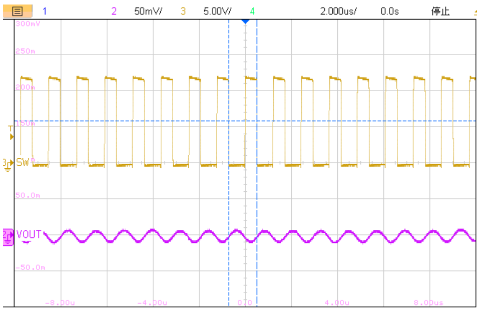
100us/div, V_{OUT}=5.0V I_{OUT}=10mA

Figure25. ET8123 Output Ripple



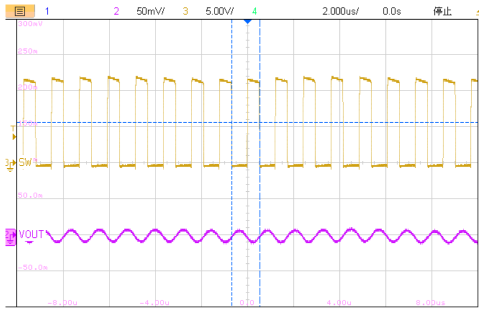
5us/div, V_{OUT}=5.0V I_{OUT}=250mA

Figure26. ET8123 Output Ripple



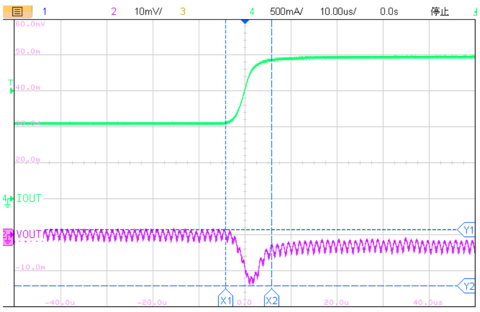
2us/div, V_{OUT}=5.0V, I_{OUT}=1A

Figure27. ET8123 Output Ripple



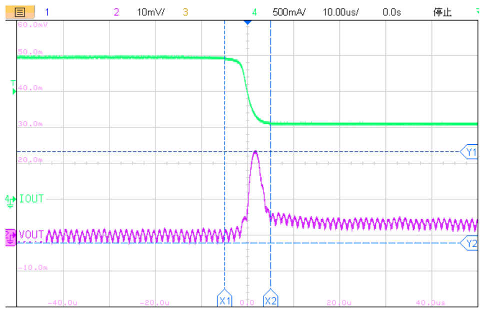
2us/div, V_{OUT}=5.0V I_{OUT}=2A

Figure28. ET8123 Output Ripple



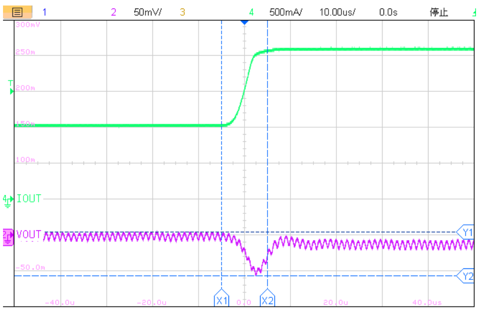
10us/div, V_{OUT}=1.0V I_{OUT} =1A to 2A

Figure29. ET8123 Load Transient



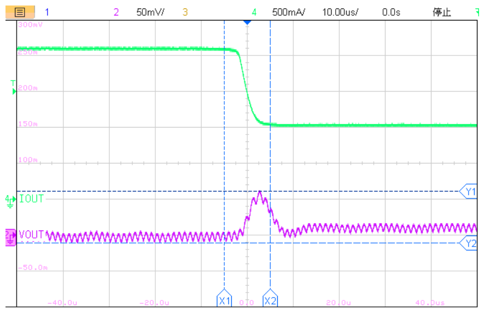
10us/div, V_{OUT}=1.0V I_{OUT} =2A to 1A

Figure30. ET8123 Load Transient



10us/div, V_{OUT}=3.3V I_{OUT} =1A to 2A

Figure31. ET8123 Load Transient

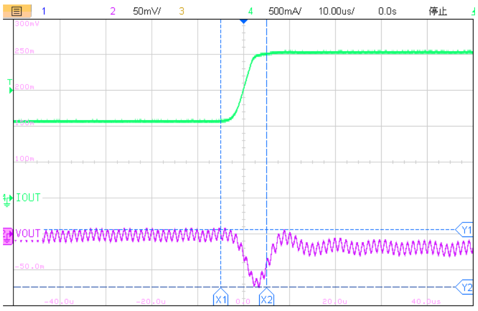


10us/div, V_{OUT}=3.3V I_{OUT} =2A to 1A

Figure32. ET8123 Load Transient

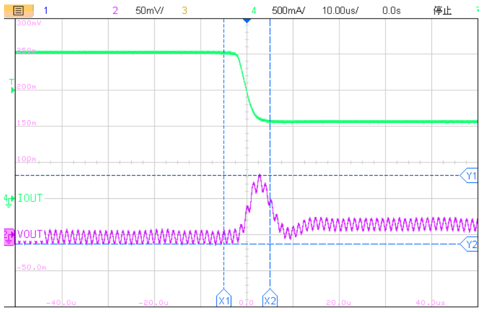
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



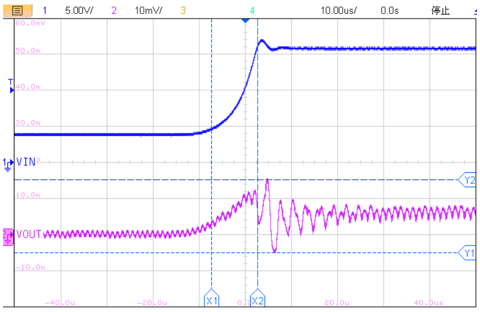
10us/div, V_{OUT}=5.0V I_{OUT} =1A to 2A

Figure33. ET8123 Load Transient



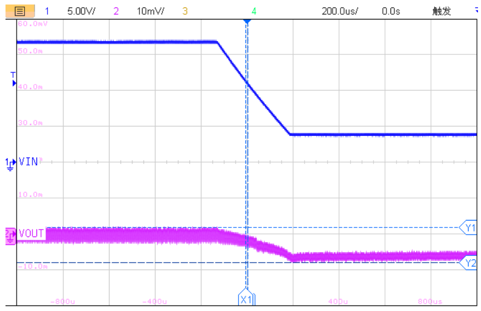
10us/div, V_{OUT}=5.0V I_{OUT} =2A to 1A

Figure34. ET8123 Load Transient



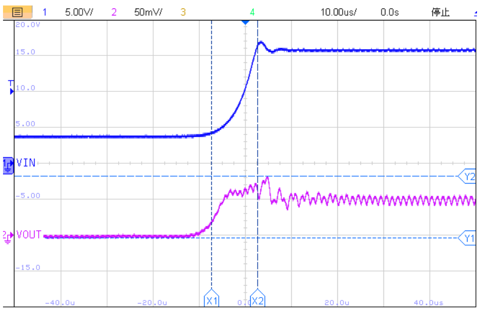
5us/div, V_{OUT}=1.0V I_{OUT} =1A V_{IN}=4.5V to 17V

Figure35. ET8123 Line Transient



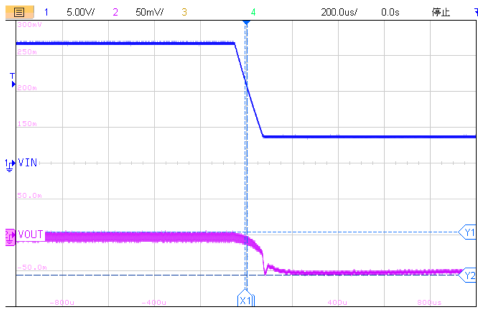
200us/div, V_{OUT}=1.0V I_{OUT} =1A V_{IN}=17V to 4.5V

Figure36. ET8123 Line Transient



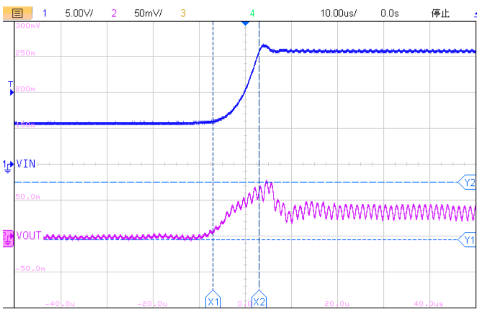
10us/div, V_{OUT}=3.3V I_{OUT} =1A V_{IN}=4.5V to 17V

Figure37. ET8123 Line Transient



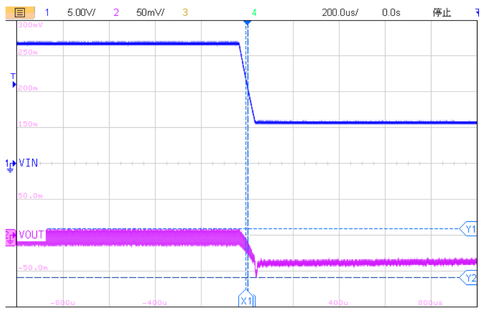
200us/div, V_{OUT}=3.3V I_{OUT} =1A V_{IN}=17V to 4.5V

Figure38. ET8123 Line Transient



10us/div, V_{OUT}=5.0V I_{OUT} =1A V_{IN}=6.5V to 17V

Figure39. ET8123 Line Transient

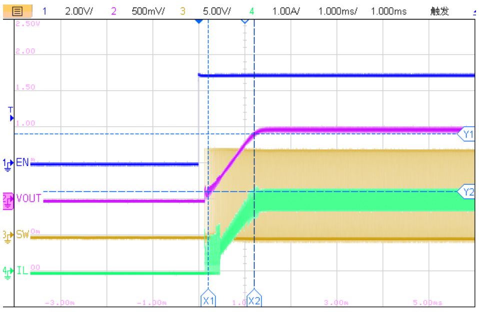


200us/div, V_{OUT}=5.0V I_{OUT} =1A V_{IN}=17V to 6.5V

Figure40. ET8123 Line Transient

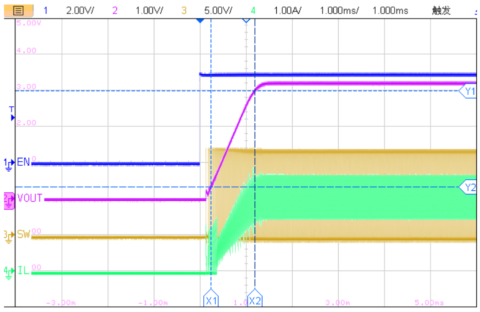
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



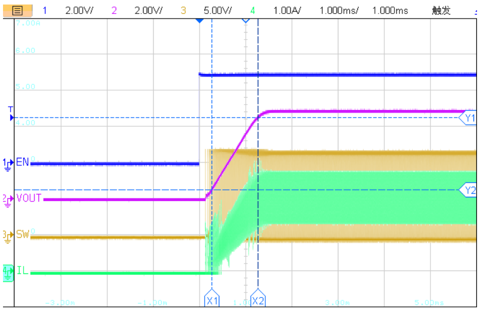
1ms/div,V_{IN}=12V V_{OUT}=1.0V I_{OUT}=2A

Figure41. ET8123 Start-Up Relative to EN



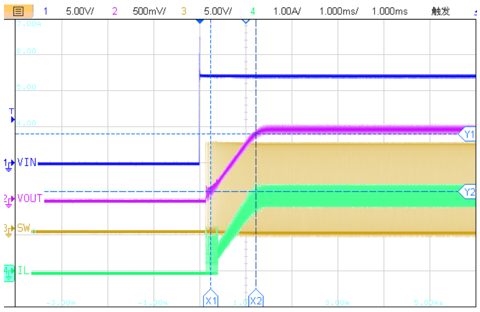
1ms/div,V_{IN}=12V V_{OUT}=3.3V I_{OUT}=2A

Figure42. ET8123 Start-Up Relative to EN



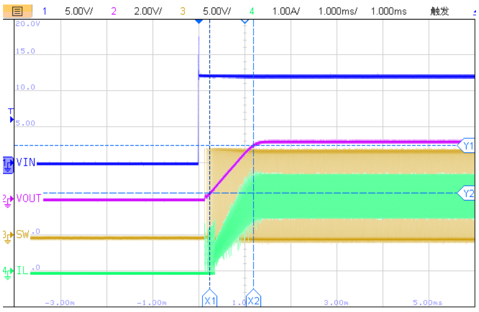
1ms/div,V_{IN}=12V V_{OUT}=5.0V I_{OUT}=2A

Figure43. ET8123 Start-Up Relative to EN



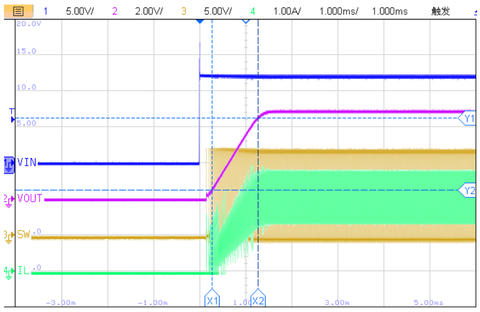
1ms/div,V_{EN}=5V V_{OUT}=1.0V I_{OUT}=2A

Figure44. ET8123 Start-Up Relative to VIN



1ms/div,V_{EN}=5V V_{OUT}=3.3V I_{OUT}=2A

Figure45. ET8123 Start-Up Relative to VIN



1ms/div,V_{EN}=5V V_{OUT}=5.0V I_{OUT}=2A

Figure46. ET8123 Start-Up Relative to VIN

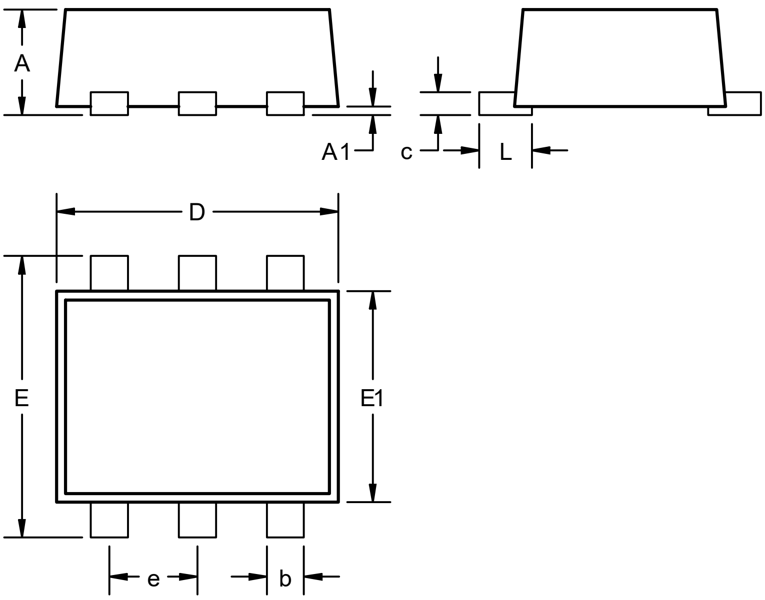
Layout

Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance and better heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize-trace impedance.
3. Provide sufficient Vias for the input capacitor and output capacitor.
4. Keep the SW trace physically short and wide to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its-trace impedance.

Package Dimension

SOT-563



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.525	—	0.6
A1	0.00	—	0.05
b	0.17	0.22	0.27
c	0.09	—	0.16
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	1.20	1.30
e	0.50BSC		
L	0.20	0.30	0.40

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0	2019-05-21	Preliminary Version	Xielh	Xielh	Zhujl
1.0	2022-06-23	Initial Version	Shib	Xielh	Liujy
1.1	2022-09-15	Update Electrical Characteristics	LiuCong	Xielh	LiuCong
1.2	2024-1-24	Update Electrical Characteristics	LiuCong	Xielh	Xielh
1.3	2024-03-08	Update Electrical Characteristics	LiuCong	Xielh	Xielh