4 Channel LDO PMIC with I²C Control

General Description

The ET5904 is CMOS-based low dropout, low power linear regulator. It's a 4 channels integrated LDOs with I²C control. 2 channels offering 800mA with NMOS pass transistor, 2 channels offering 300mA with PMOS pass transistor. ET5904 include 400kHz high speed I²C interface, the function setting is flexible such as power sequence, output voltage, output discharge, current limit per channel. The chip enable control support EN pin control and I²C control.

Features

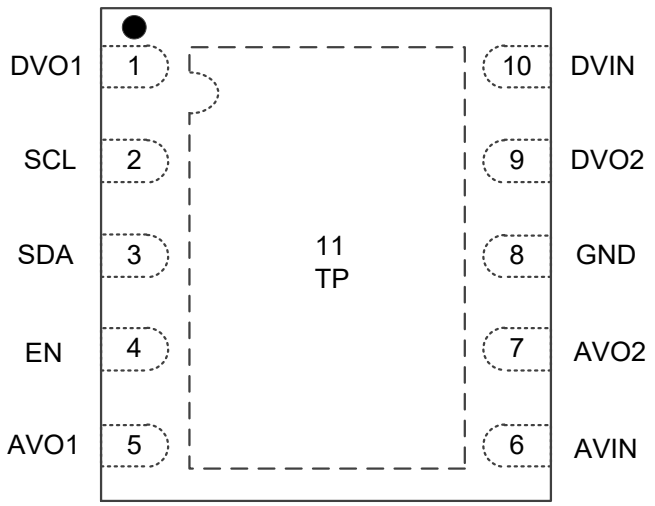
- DVIN input voltage range from 0.6V to 2.0V
- AVIN input voltage range from 3.0 V to 5.5V
- LDO1/2 output voltage range from 0.6V to 1.8V with step 6mV.
- LDO1/2 output current are 800mA Min.
- LDO1/2 ultra-low dropout are typical 105mV at 800mA, 1.2V output.
- LDO3/4 output voltage range from 1.2V to 4.3V with step 12.5mV
- LDO3/4 output current range are 300mA Min.
- LDO3/4 ultra-low dropout are typical 90mV at 300mA, 2.8V output.
- LDO3/4 built-in inrush current limit at Typ. 250 mA for appr.700 us period after start-up
- Very low input quiescent current of 85μA typical
- Built-in over-current protection and thermal shutdown circuit
- Built-in auto-discharging circuit (optional)
- Built-in under voltage lock-out
- Package Information:

Part No.	Package	MSL
ET5904	DFN10 (2mm × 2mm)	Level 1

Applications

- Constant-Voltage Power Supply for Battery-powered Device
- Constant-Voltage Power Supply for Smartphones, Tablets
- Constant-Voltage Power Supply for Cameras, DVRs, STB and Camcorders

Pin Configuration

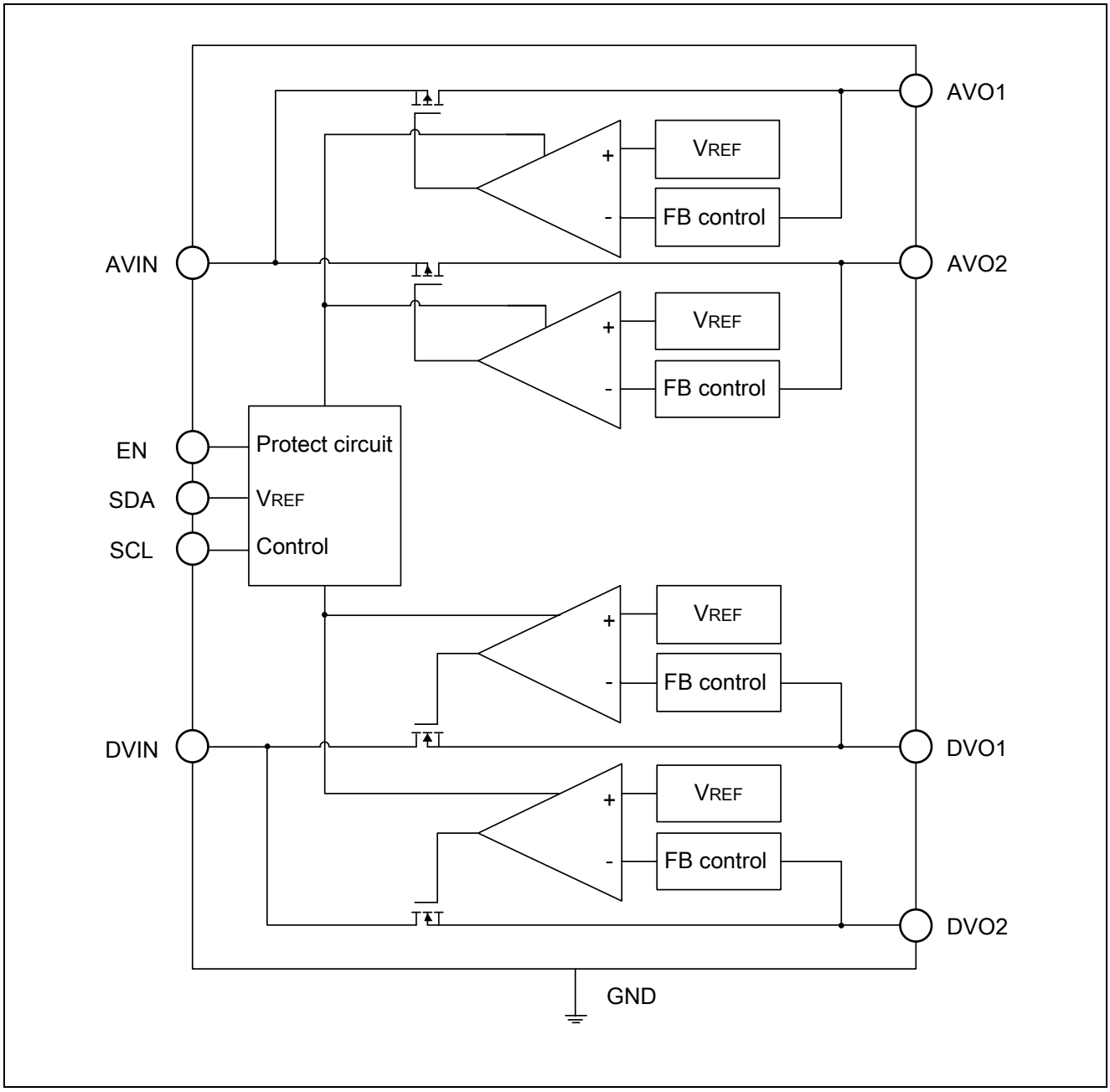


Top view

Pin Function

Pin No.	Pin Name	Pin Function
1	DVO1	LDO1 regulate output
2	SCL	I^2C interface Clock
3	SDA	I^2C interface Data
4	EN	Global enable control, active high. Maintain to low with 0.3uA pull down current source
5	AVO1	LDO3 regulator output
6	AVIN	LDO3~4 supply input and LDO1~2 bias input
7	AVO2	LDO4 regulator output
8	GND	Ground
9	DVO2	LDO2 regulator output
10	DVIN	LDO1~2 supply input
11	TP	Thermal Pad, only be connect to GND or floating, can't be connected to other pins

Block Diagram



Functional Description

Power Up and Power Down Control

ET5904 has 4 LDO regulators. LDO1/2 are using NMOS pass transistor for output voltage regulation from DVIN. LDO3/4 are using PMOS pass transistor for output voltage regulation from AVIN. The ET5904 offers smooth start-up. Power up/down of each regulator can be controlled by the following three ways. It can be set at the registers LDOx_SEQ[3:0] (x=1 to 4) respectively.

1. External EN pin control.

External EN pin toggles from low to high, it will force all 4 LDO regulators powered up, output voltage of each

LDO is default voltage. LDO1/2 output default voltage 1.2V, LDO3/4 output default voltage 2.8V. When external EN pin is low, LDO output can be controlled by an I²C register.

2. Individual on/off control.

Power-up and shut down of each regulator can be controlled by an I²C register. LDOx_EN is an internal signal to enable one of regulators, If LDOx_SEQ[3:0] set to '0000', that LDOx channel can be controlled directly by a bit specified in register LDOx_EN[3:0]. LDOx_VSET[3:0] can set output voltage of each channel.

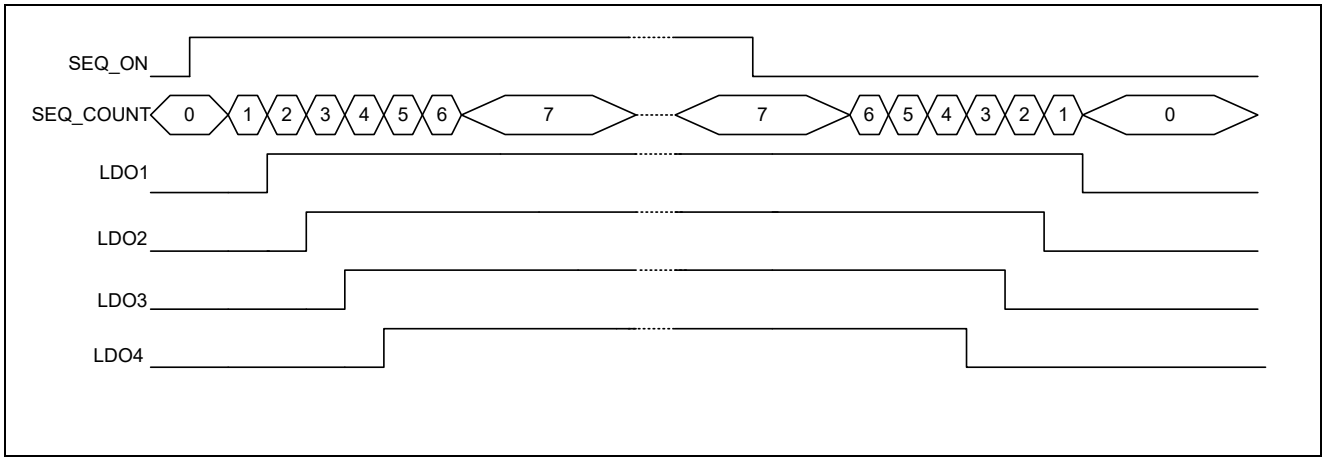
3. Automatic power up/down sequence control.

ET5904 has 7 SLOTs to which each regulator can be assigned.

They are started by SEQ_ON signal. when SEQ_ON is high. Internal counter SEQ_COUNT [2:0] starts increments from 0 ("000") to 7 ("111"). When SEQ_ON is low, SEQ_COUNT [2:0] decrements from 7 ("111") to 0 ("000"). Regulators assigned to one of SLOTs starts power-up or power-down.

When SEQ_COUNT [2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I²C, write '00' to SEQ_CTRL [1:0] will set SEQ_ON to'0', while write '01' to SEQ_CTRL[1:0] will set SEQ_ON to '1'.



* Example of Power-up in the case of LDO1/2/3/4 are assigned to SLOT1/2/3/4 respectively

* Example of Shutdown in the case of LDO1/2/3/4 are assigned to SLOT1/2/3/4 respectively.

Input and Output Capacitor

The LDO1/2 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2μF to 22μF. The LDO3~LDO4 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 0.47μF to 10μF. The recommended CDVO1/2 =4.7μF and CAVO3/4= 1μF.

The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available (PCB inductance in DVIN and/or AVIN inputs as example), the recommended CAVIN =4.7μF and CDVIN= 4.7μF or greater.

Current Limit Protection

For each channel, when output current of LDO output pin is higher than current limit threshold or the output pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a

predesigned level to prevent over-current and thermal damage. Set related bits to select Current limit threshold register.

Thermal Shutdown Protection

Thermal protection disables all the output when the junction temperature rises to approximately +150°C, allowing the device to cool down. When the junction temperature reduces to approximately +120°C all the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

For each channel, when shut down the output, the Auto-discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of output pin in very short time.

The Auto-discharging function is optional. Set related bits to select output discharge function for discharge resistor (RDIS Register) : “0” is Disable. “1” is Enable.

Note : When use the discharge function by register control , should set Bit7 =1 .
When set Bit7 =”0”, EN=”0”, discharge resistor selection[3:0]=0x00, discharge function enable.
When set Bit7 =”1”, EN=”0”, discharge resistor selection[3:0]=0x00, discharge function disable.

Serial Port Interface (I^2C)

- **Bus Interface**

Baseband Processor can transmit data with ET5904 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

- **Data Validity**

When the SCL signal is high, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

- **Start (Re-start) and Stop Working Conditions**

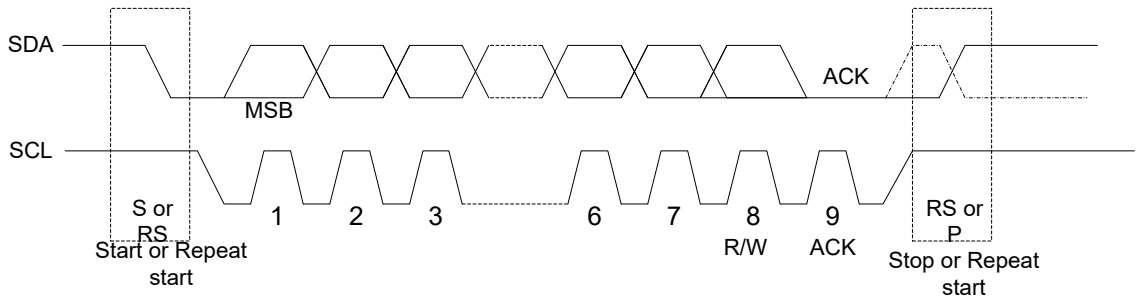
When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

- **Byte format**

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

- **Acknowledge**

During the writing mode, ET5904 will send a low level response signal with one period width to the SDA port. During the reading mode, ET5904 will not send response signal and the host will send a high response signal one period width to the SDA.



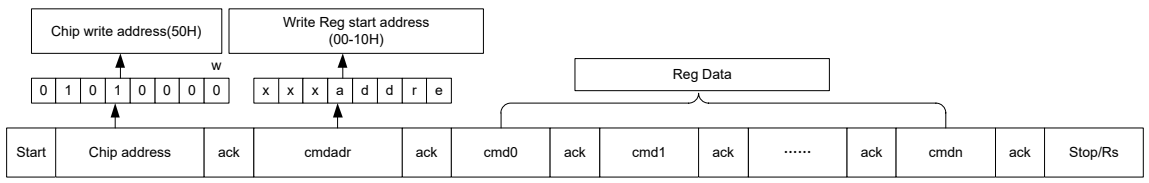
I²C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =400kHz
- Restart: SDA-level turnover as expressed by the dashed line wavefor

- **Chip Address**

Chip address is 01010000(Writing Register mode)/01010001(Reading Register Mode)

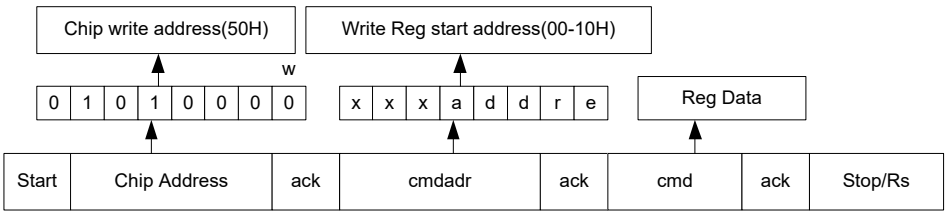
- **I²C Writing Command Register Interface Protocol (continuous):**



I²C Writing Command Register(continuous)

- Start=Start Conditions
- Chip address=Write register address =0101000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addr)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge
- ……
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

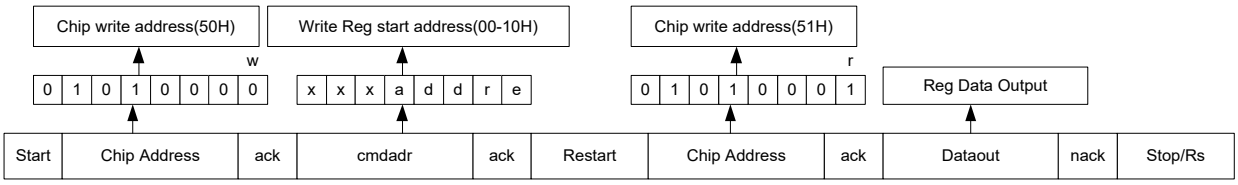
- **I²C Writing Command Register Interface Protocol (single):**



I²C Writing Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=0101000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr (xxx + REG's 5bit addr)
- ack=Acknowledge
- Reg data= cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

- **I²C Reading Command Register Interface Protocol(continuous)**



I²C Reading Command Register

- Start=Start Conditions
- Chip address =Write register address=0101000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addr)
- ack=Acknowledge
- Restart=Restart condition
- Chip address Read register address=0101000+1(r)b
- ack=Acknowledge
- Dataout=Register data output
- nack=No Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

Register Map

Addr	Name	Type	Rst	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	CHIPID	R/W	0x00	Chip_REV[7:0]							
0x01	ILIMIT	R/W	0x00	Rev.				LDO3/4_IL [1:0]		LDO1/2_IL [1:0]	
0x02	RDIS	R/W	0x00	RDIS_EN	Rev.			Discharge Resistor Selection [3:0]			
0x03	DVO1	R/W	0x64	LDO1_VSET [7:0]							
0x04	DVO2	R/W	0x64	LDO2_VSET [7:0]							
0x05	AVO1	R/W	0x80	LDO3_VSET [7:0]							
0x06	AVO2	R/W	0x80	LDO4_VSET [7:0]							
0x0A	SEQ1	R/W	0x00	LDO2_SEQ [3:0]				LDO1_SEQ [3:0]			
0x0B	SEQ2	R/W	0x00	LDO4_SEQ [3:0]				LDO3_SEQ [3:0]			
0x0E	LDO_EN	R/W	0x00	REG_RST	Rev.			LDOx_EN [3:0]			
0x0F	SEQ_C	R/W	0x00	SEQ_SPEED [1:0]		SEQ_CTRL [1:0]		SEQ_ON	SEQ_COUNT [2:0]		
0x10	ILIMT_ COAR	R/W	0x00	LDO4_COA_IL[1:0]		LDO3_COA_IL[1:0]		LDO2_COA_IL[1:0]		LDO1_COA_IL[1:0]	

Note: Rev.—Reserve, keep “0”.

- **0x00 CHIPID Register---- Indicates the device ID with revision.**

  Chip_REV[7:0] Indicates the device ID with revision. Read only

- **0x01 ILIMIT Register ----LDO Current Limit Selection**

  Defined the typical value of current limit threshold value for LDOs.

  The detail current limit value are shown in the table as below:

  LDO1/LDO2 Current Limit Table:

LDO1/2_COA_IL[1:0]	LDO1/2_IL[1:0]	Current Limit(mA)
00 Default	00	1300
	01	1250
	10	1400
	11	1450
01	00	1070
	01	1010
	10	1130
	11	1190
10	00	1720
	01	1680
	10	1800
	11	1880
11	00	1520
	01	1460
	10	1600
	11	1660

LDO3/LDO4 Current Limit Table:

LDO3/4_COA_IL[1:0]	LDO3/4_IL[1:0]	Current Limit(mA)	Short Current Limit(mA)
00 Default	00	450	45
	01	380	38
	10	590	59
	11	520	52
01	00	230	23
	01	170	17
	10	380	38
	11	310	31
10	00	860	88
	01	820	81
	10	1010	102
	11	940	95
11	00	650	67
	01	600	60
	10	790	81
	11	740	74

- **0x02 RDIS Register ----Discharge Resistor Selection**

Each LDO regulators output discharge resistor enable control.
Bit0 for LDO1, Bit1 for LDO2, Bit2 for LDO3, Bit3 for LDO4
1=Enable, 0=Disable.

Note: When use the Discharge Function by Register Control, should set Bit7 =”1”.
When set Bit7 =”0”, EN=”0”, Discharge Resistor Selection [3:0]=0x00, Discharge Function Enable.
When set Bit7 =”1”, EN=”0”, Discharge Resistor Selection [3:0]=0x00, Discharge Function Disable.

- **0x03 DVO1 Register ---- DVO1 output voltage setting register**
- **0x04 DVO2 Register ---- DVO2 output voltage setting register**

The register LDO1/2_VSET [7:0] set the voltage of DVO1/ DVO2, it have 256 steps, shown as below table, the formula is VDVO =0.6V+ LDO1/2_VSET *0.006V.

DVO1/DVO2 Output Voltage set by LDO1/2_VSET [7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	0.600
1	00000001	0.606
2	00000010	0.612
3	00000011	0.618
4	00000100	0.624
5	00000101	0.630

……	……	……
100	**01100100(default)**	**1.200**
101	01100101	1.206
102	01100110	1.212
~255	……	……

- **0x05~0x06 AVO1~2 Register ---- AVO1~2output voltage setting register**

The registers LDO3/4_VSET [7:0] set the voltage of AVO1/AVO2, each voltage have 256 steps, shown as below table, the formula is VAVO1~AVO2=1.2V+ LDO3/4_VSET [7:0] *0.0125V.

AVO1~2 Output Voltage set by LDO3/4_VSET [7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	1.2000
1	00000001	1.2125
2	00000010	1.2250
3	00000011	1.2375
4	00000100	1.2500
5	00000101	1.2625
……	……	……
128	**10000000(default)**	**2.8000**
129	10000001	2.8125
130	10000010	2.8250
……	……	……
250	11111010	4.3250
251	11111011	4.3375
252	11111100	4.3500
253	11111101	4.3625
254	11111110	4.3750
255	11111111	4.3875

- **0x0A~0x0B SEQ1~2 Register ---- Power sequence setting register**

Power sequence setting register. there are 4 time slots defined as following table. The power-up sequence is start from slot1 to slot7 and shut down start from slo7 to slot1. Power-up and shut down of each LDO regulator can be set at any one of the slots.

Register Value	**VOUTX**
0000	Controlled by I^2C register LDOx_EN[3:0]
x001	Slot1
x010	Slot2
x011	Slot3
x100	Slot4
x101	Slot5

x110	Slot6
x111	Slot7

- **0x0E LDO_EN Register ----LDOs Chip enable control register**

Chip enable control register by I²C while the register value of LDOx_SEQ[3:0] are set to be default “0000”. This register can be written to enable or disable the corresponding LDO regulator. Bit0 for LDO1, Bit1 for LDO2, Bit2 for LDO3,Bit3 for LDO4,REG_RST bit is a software reset bit, all the register will be reset to default value if this bit is set to “1”.

- **0x0F SEQ_C Register ---- Power sequence setting and status register**

SEQ_SPEED[1:0] define the slot period as following: (Read/Write)

Register Value	Slot period(ms)
00	2.00
01	1.00
10	0.50
11	0.25

SEQ_CTRL[1:0] enables power-up or shut down of SEQ .(Read/Write)

Register Value	SEQ Status
x0	Shutdown
x1	Power-up

SEQ_ON indicates the activation signal of SEQ. (Read only)

Register Value	SEQ Status
0	Shutdown
1	Power-up

SEQ_COUNT[2:0] indicates the slot number of SEQ at the moment. (Read only)

Register Value	SEQ Counter
000	No LDO starts.
001	Slot1 starts
010	Slot2 starts
011	Slot3 starts
100	Slot4 starts
101	Slot5 starts
110	Slot6 starts
111	Slot7 starts and stop counting

- **0x10 ILIMIT Register ----LDO Current Limit Selection**

Provide more step current limit selection for each LDO if customer need.

Absolute Maximum Ratings

Item		Rating	Unit
IN Voltage (AVIN, DVIN)		-0.3 to 6.5	V
Other Pin Voltage		-0.3 to V_{IN}+0.3	V
LDO1/2 Maximum Load Current		800	mA
LDO3/4 Maximum Load Current		300	mA
Maximum Power Consumption		1800	mW
Operating Junction Temperature		-40 to 150	°C
Storage Temperature		-65 to 150	°C
Lead Temperature (Soldering, 10 sec)		300	°C
ESD	HBM	±6000	V
	CDM	±1500	V

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{AVIN}	Input Voltage	3 to 5.5	V
V_{DVIN}	Input Voltage	0.6 to 2.0	V
I_{AVOx}	Output Current (300mA LDOs)	0 to 300	mA
I_{DVOx}	Output Current (800mA LDOs)	0 to 800	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{AVIN}	AVIN Effective Input Ceramic Capacitor Value	2.2 to 10	µF
C_{DVIN}	DVIN Effective Input Ceramic Capacitor Value	2.2 to 10	µF
C_{DVOx}	Effective Output Ceramic Capacitor Value (800mA LDO)	2.2 to 22	µF
C_{AVOx}	Effective Output Ceramic Capacitor Value (300mA LDO)	0.47 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{AVIN}=V_{AVOx}+1V,V_{DVIN}=V_{DVOx}+0.3V, V_{AVIN}=(V_{DVOx}+1.6V) or 3.0V whichever greater, I_{OUT}=1mA, C_{DVIN}=4.7μF, C_{AVIN}=4.7μF, C_{DVOx}=4.7μF, C_{AVOx}=1μF, Ta = -40°C~85°C. Typical values are at. T_A=25 ºC)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{DVIN}	V_{DVIN}>V_{DVOx}	V_{DVOx} + V_{DROP_DVOx}		5.5	V
V_{AVIN} Voltage Range	V_{AVIN} (1)	V_{DVO}+1.6V, V_{AVIN}>3.0	3.0		5.5	V
Under-voltage lock-out	V_{UVLO}	V_{AVIN} falling	1.7	2	2.3	V
Hysteresis	V_{UVLO_HYS}	Under-voltage Lock-out Hysteresis	0.1	0.2	0.3	V
V_{AVIN} Current	I_{Q_ON}	Active mode: V_{EN}=V_{AVIN} or Enable chip by I^2C, no load	60	85	150	μA
	I_{Q_OFF}	V_{EN}=0V or Shut down by I^2C		0.4	1	μA
EN Pull-down Current	I_{EN}	V_{EN}=5.5V, V_{AVIN}=5.5 V		0.3	1	μA
EN Input Voltage High	V_{ENH}		0.9			V
EN Input Voltage Low	V_{ENL}				0.4	V
SCL/SDA Input Voltage High	V_{I2CH}		1.4			V
SCL/SDA Input Voltage Low	V_{I2CL}				0.3	V
SDA Logic Low Output	V_{OL}	3mA Sink			0.4	V
SCL Clock Frequency	F_{SCL}				400	kHz
Thermal Shutdown Threshold	T_{TSD} (3)	T_J rising		150		°C
Thermal Shutdown Hysteresis	T_{HYS} (3)	T_J falling from shutdown		30		°C

800mA LDO1/2

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{DVOx}	I_{OUT}=1mA~800mA, Ta=25 ºC	-2		2	%
		I_{OUT}=1mA~800mA, Ta = -40°C ~85°C	-2.5		2.5	
Dropout Voltage	V_{DROP_DVOx}(2)	I_{OUT} = 500mA, V_{OUT}=1.2V		65	105	mV
		I_{OUT} = 800mA, V_{OUT}=1.2V		105	165	
Output Current	I_{OUT_DVOx}		800			mA
Current Limit	I_{LIM_DVOx}	Default Current Limit Register	1	1.3	1.6	A
Load Regulation	Reg_{LOAD_DVOx}	1mA≤I_{OUT}≤800mA		2	20	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{DVIN} Line Regulation	Reg_{LINE_DVOx}	V_{DVOx}+0.3V≤V_{DVIN}≤5.5 V (I_{OUT} =10mA)		0.02	0.2	%/V
V_{AVIN} Line Regulation		3.0V or (V_{DVOx}+ 1.6 V) whichever greater < V_{AVIN} < 5.5V, (V_{DVIN}=V_{DVOx}+0.3V, I_{OUT}=10mA)		0.02	0.2	%/V
Power Supply Rejection Ratio	$PSRR\_DVOx$(3)	V_{IN} to V_{OUT}, f=1kHz, V_{DVIN}=1.5V, V_{DVOx}=1.2V, Ripple 0.2V_{PP}, I_{OUT}=30mA		65		dB
		V_{AVIN} to V_{DVO}, f=1kHz, V_{DVIN}=1.5V, V_{DVOx}=1.2V, Ripple 0.2V_{PP}, I_{OUT}=30mA		75		
Output Noise	e_{N_DVOx}(3)	V_{DVIN}=1.5V, V_{OUT}=1.2V, f= 10 Hz to 100 kHz		50		μV_{RMS}
Output Resistance of Auto Discharge at Off State	R_{DIS_DVOx}	V_{EN}=0V, or Shut down by I^2C, V_{OUT} =0.5V V_{AVIN}=3.8V	250	350	450	Ω
Line Transient	V_{TRLN_DVOx}(3)	V_{DVIN}= V_{DVOx}+0.3V to V_{DVOx}+1.3V in 10us, I_{OUT}=1mA, T_A=25°C		5	30	mV
		V_{DVIN}= V_{DVOx}+1.3V to V_{DVOx}+0.3V in 10us, I_{OUT}=1mA, T_A=25°C		5	30	mV
Load Transient	V_{TRLD_DVOx}(3)	I_{OUT}=1mA to 800mA in 1us V_{DVIN}= V_{DVOx}+0.3V, T_A=25°C		160	240	mV
		I_{OUT}=800mA to 1mA in 1us V_{DVIN}= V_{DVOx}+0.3V, T_A=25°C		160	240	mV
Turn-On Time	T_{ON_DVOx}(3)	From assertion of V_{EN} to V_{OUT}=95%$V_{DVO(NOM)}$		300	450	μs

300mA LDO3/LDO4

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dropout Voltage	V_{DROP_AVOx}(2)	I_{OUT} = 300mA, V_{AVOx}=2.8V		90	130	mV
		I_{OUT} = 150mA, V_{AVOx}=2.8V		45	65	mV
Regulated Output Voltage	V_{AVOx}	I_{OUT}=1mA~300mA,T_A=25°C	-2		2	%
		I_{OUT}=1mA~300mA, T_A = -40°C~85°C	-2.5		2.5	
Output Voltage Line Regulation	Reg_{LINE_AVOx}	V_{AVOx} =2.8V, 3.8V≤V_{AVIN}≤5.5V, I_{OUT} = 10mA （$\Delta V_{AVOx}/\Delta V_{AVIN}/V_{AVOx}$）		0.01	0.2	%/V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Load Regulation	Reg_{LOAD_AVOx}	I_{OUT} from 1mA to 300mA		10	30	mV
Line Transient (The absolute value of the output change)	V_{TRLN_AVOx}(3)	V_{AVOx}=2.8V, I_{OUT} =1mA, V_{AVIN} =3.8V to 5.5V in 10us, T_A=25°C		5	20	mV
		V_{AVOx}=2.8V , I_{OUT} = 1mA, V_{AVIN} =5.5V to 3.8V in 10us, T_A=25°C		5	20	
Load Transient (The absolute value of the output change)	V_{TRLD_AVOx}(3)	V_{AVOx}=2.8V, V_{AVIN} =3.8V, I_{OUT} from 1mA to 300mA in 1us, T_A=25°C		40	80	mV
		V_{AVOx}=2.8V, V_{AVIN}=3.8V, I_{OUT} from 300mA to 1mA in 1us, T_A=25°C		40	80	
Output Current	I_{OUT_AVOx}		300			mA
Over Current Limit	I_{LMT_AVOx}	Default Current Limit Register, V_{AVIN}= V_{LDOx_VSET}+1V, T_A=25°C	350	450	600	mA
Short Current Limit	I_{SHORT_AVOx}	Default Current Limit Register,V_{AVOx}=0V, T_A=25°C	20	45	60	mA
Power Supply Rejection Ratio	$PSRR\_{AVO}$(3)	f=1kHz, I_{OUT}=20mA, V_{AVIN}= V_{LDOx_VSET}+1V, T_A=25°C		92		dB
Output Noise	e_N(3)	10Hz to 100kHz, I_{OUT} =30mA, V_{AVOx} =2.8V, V_{AVIN}= 3.8V, T_A=25°C		8		μV_{RMS}
Output resistance of auto discharge at off state	R_{LOW_AVOx}	V_{EN}=0V, or Shut down by I^2C, V_{AVIN}=3.8V,I_{OUT}=10mA	250	350	450	Ω
Output Turn-on Delay Time	T_{ON_AVOx}(3)	From V_{EN}> V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$		130	250	μs

Note1: Here V_{AVIN} means internal circuit can work normal.

If V_{AVIN} <V_{AVOx}, Output voltage follow V_{AVIN} (I_{OUT}=1mA), circuit is safety.

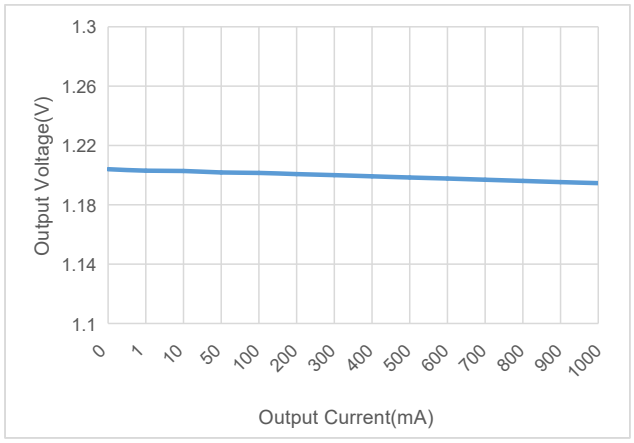
Note2: V_{DROP_DVO} and V_{DROP_AVOx} FT test method:

Test the V_{OUT} voltage at V_{LDOx}_vset +$V_{DROPMAX}$ with output current.

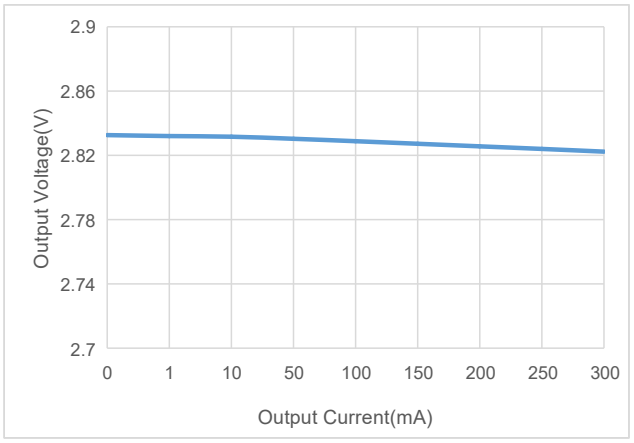
Note3: Guaranteed by design and characterization, not a FT item.

Typical Characteristics

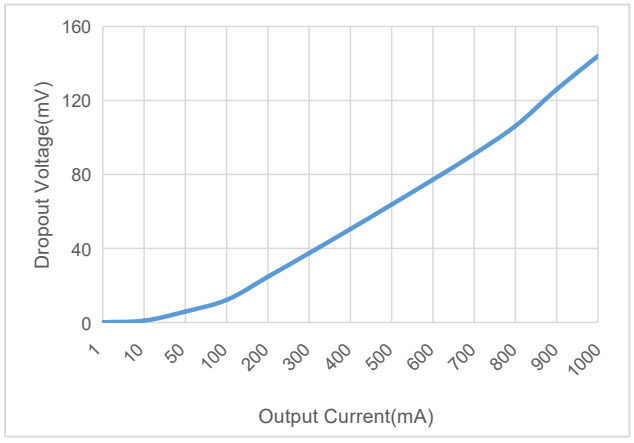
(Unless otherwise noted , V_{AVIN}=V_{AVOx}+1V,V_{DVIN}=V_{DVOx}+0.3V, V_{AVIN}=(V_{DVOx}+1.6V) or 3.0V whichever greater, I_{OUT}=1mA, C_{DVIN}=4.7μF, C_{AVIN}=4.7μF, C_{DVOx}=4.7μF, C_{AVOx}=1μF, T_A = -40°C~85°C. Typical values are at. T_A=25 ºC)



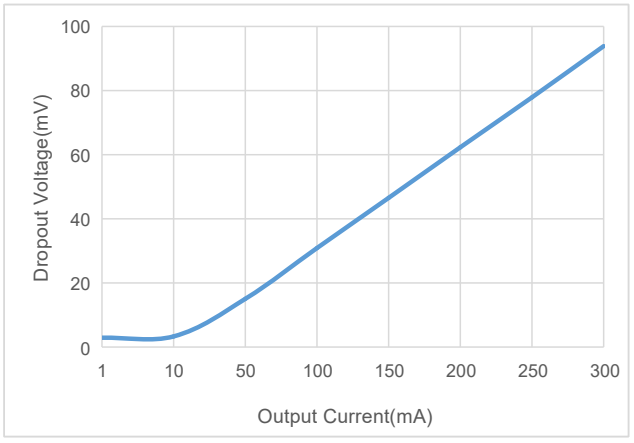
LDO1/2 Output Voltage VS IOUT



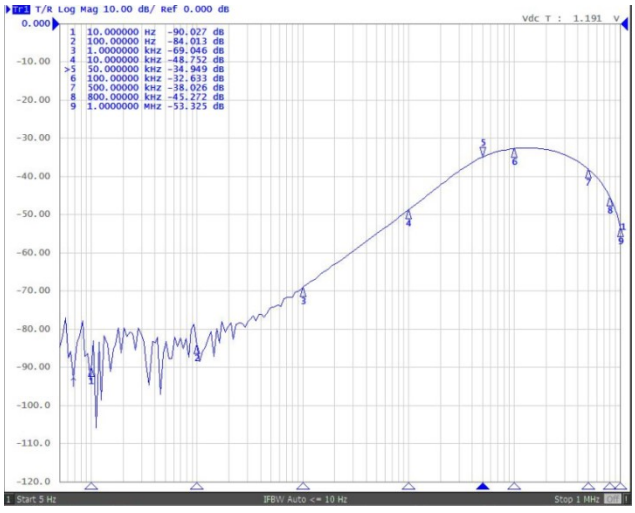
LDO3/4/ Output Voltage VS IOUT



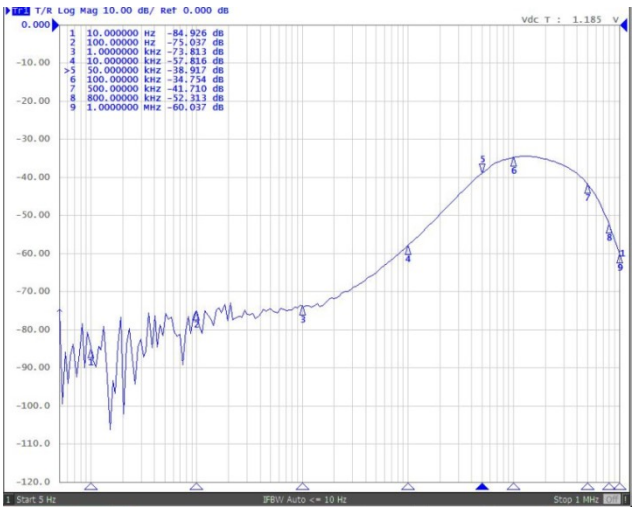
LDO1/2 Dropout Voltage VS Output Current



LDO3/4 Dropout Voltage VS Output Current

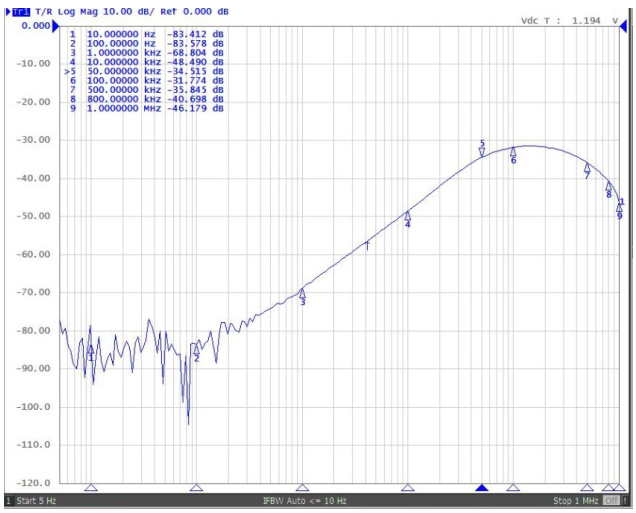


LDO1 PSRR-V_{DVIN}

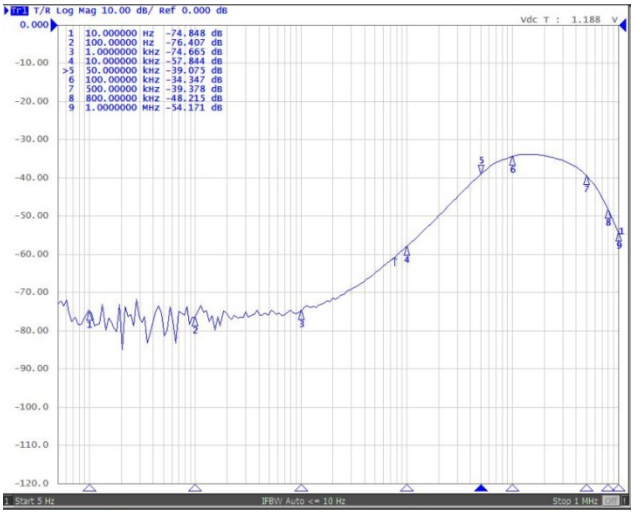


LDO1 PSRR-V_{AVIN}

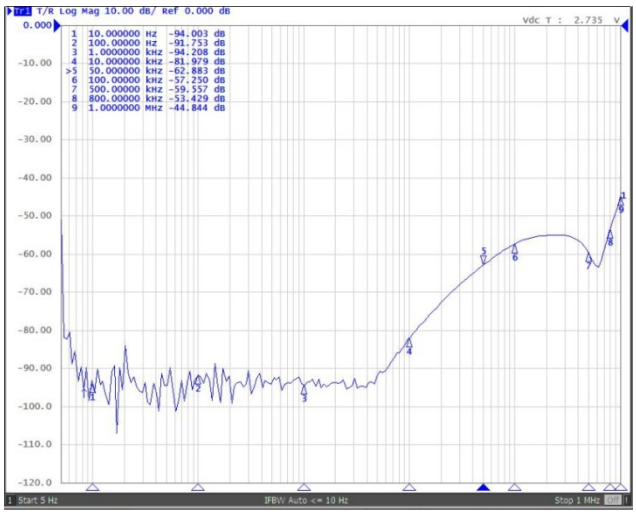
Typical Characteristics (Continued)



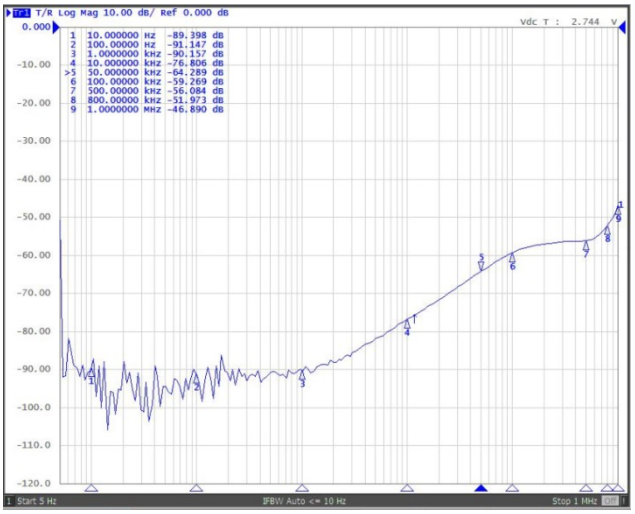
LDO2 PSRR-V_{DVIN}



LDO2 PSRR-V_{AVIN}

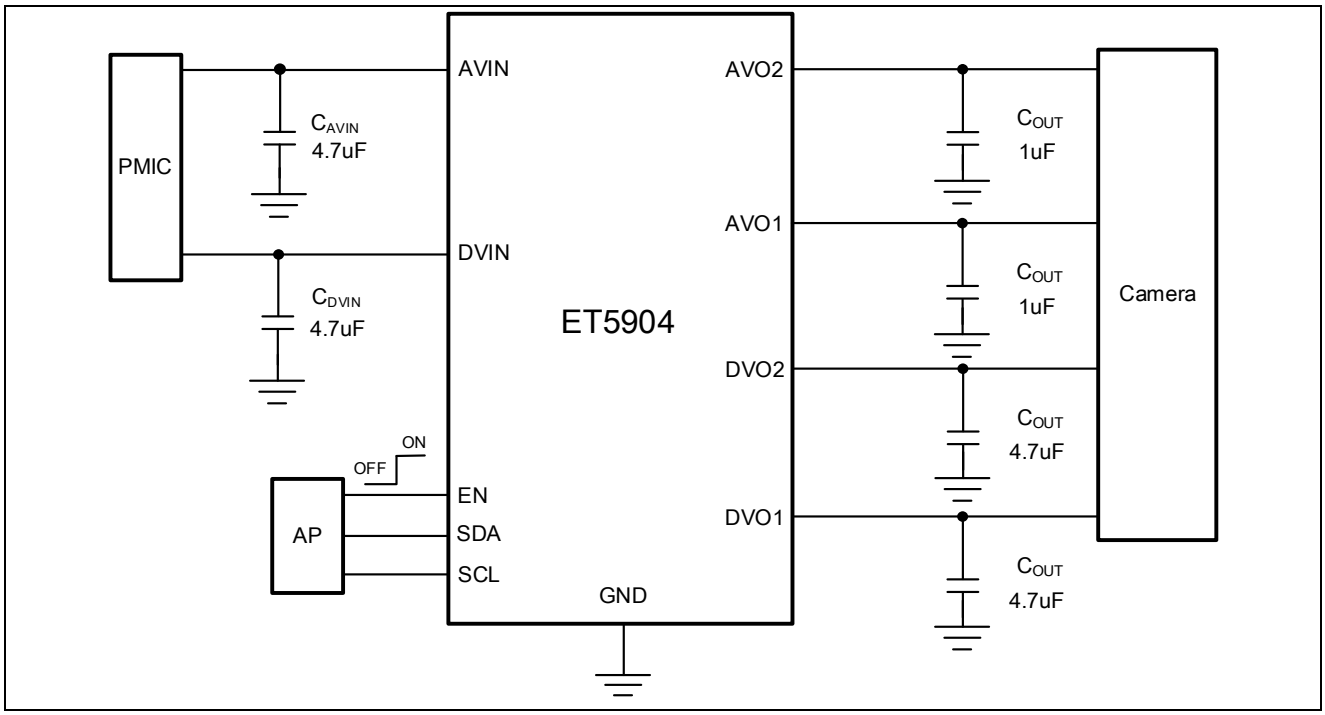


LDO3 PSRR-V_{AVIN}

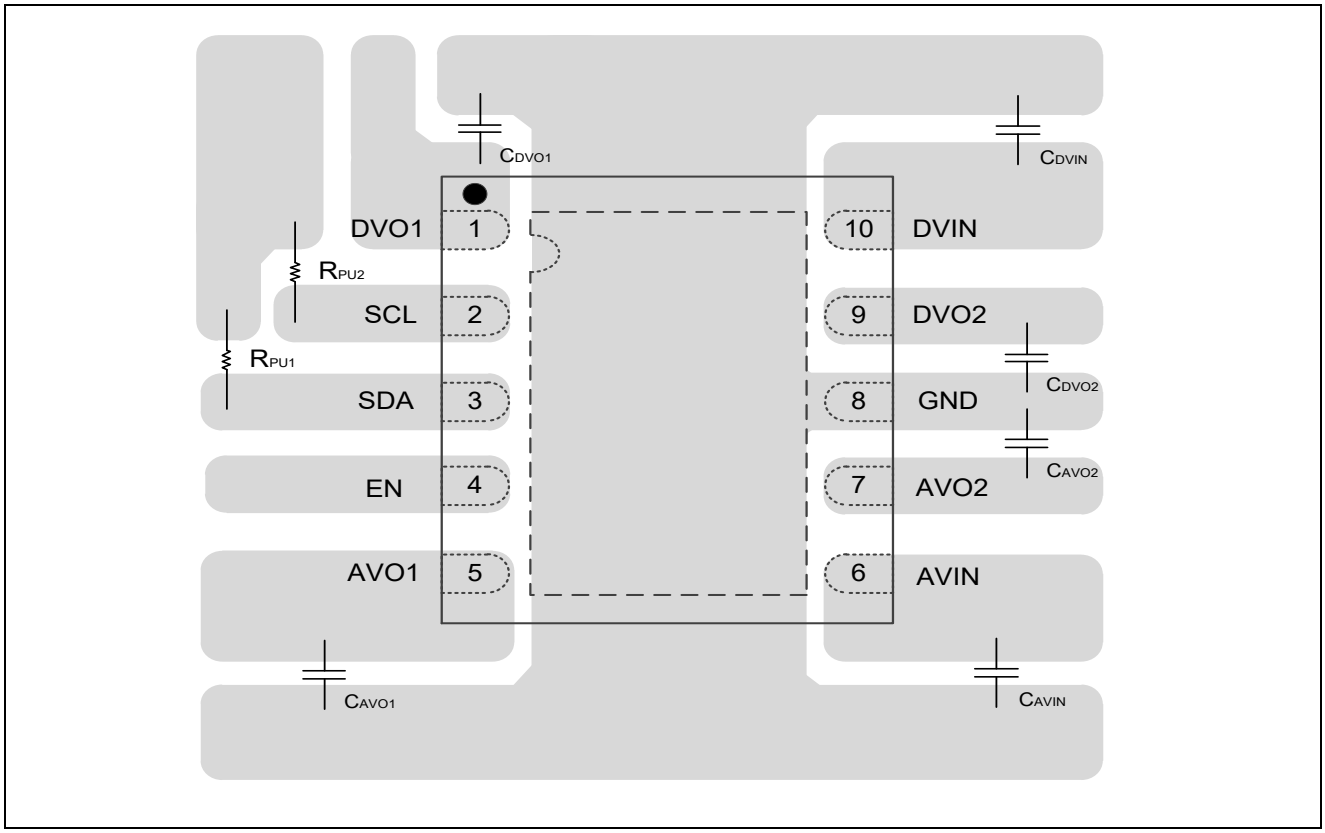


LDO4 PSRR-V_{AVIN}

Application Circuits

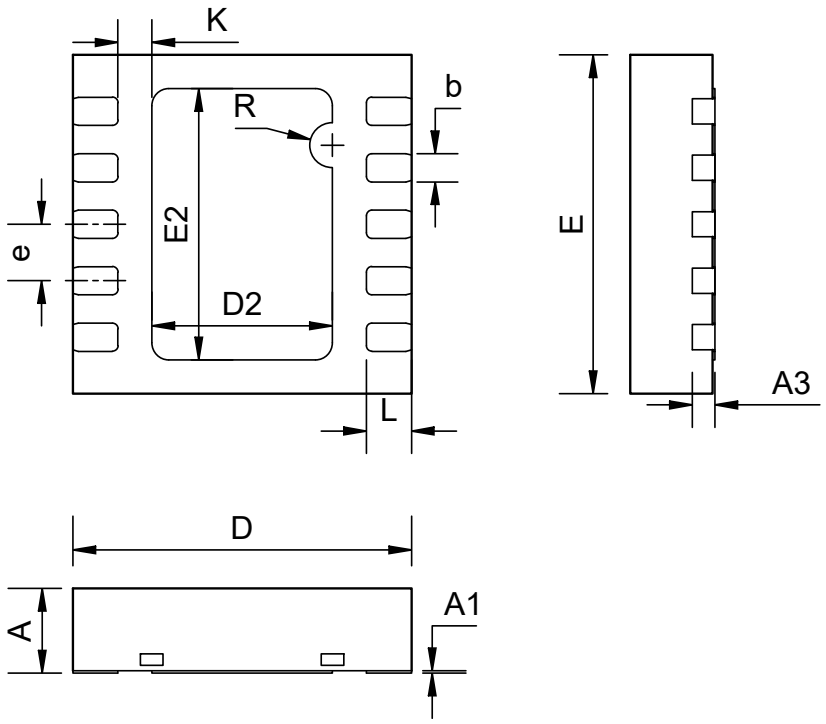


Recommended PCB Layout



Package Dimension

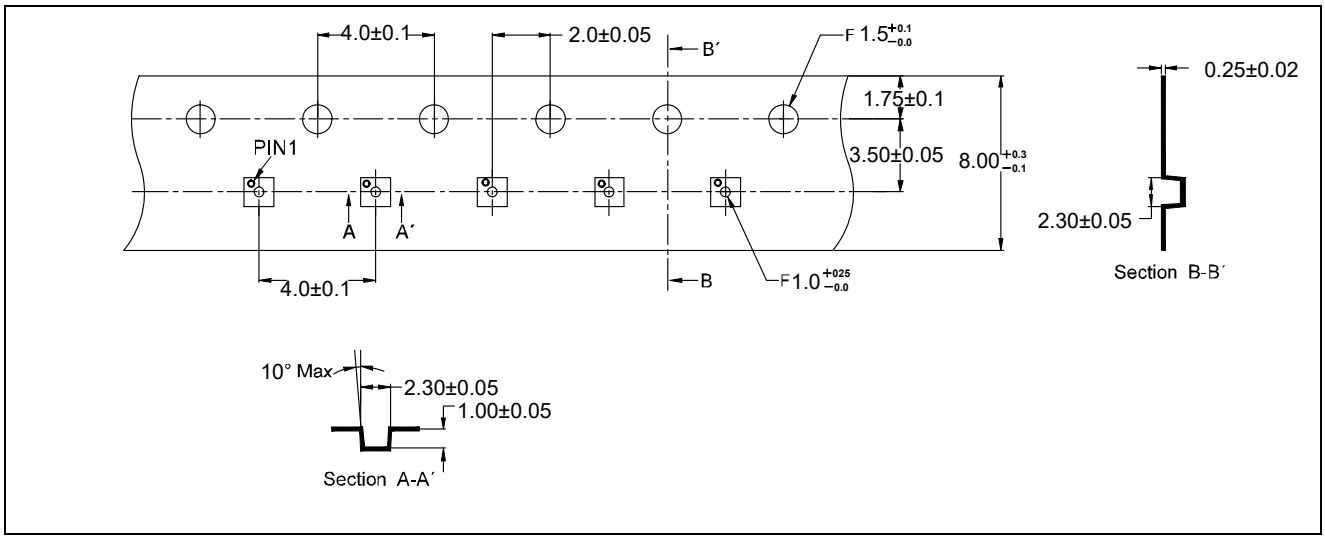
DFN10(2×2)



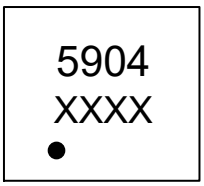
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
K	0.15	0.25	0.35
L	0.25	0.30	0.35
R		0.10REF	

Tape Information



Marking



5904 = Part Number

XXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0	2019-10-22	Preliminary Version	Liu Yi Guo	Liu Yi Guo	Zhu Jun Li
1.0	2020-01-02	Original Version	Liu Yi Guo	Liu Yi Guo	Liu Jia Ying
1.1	2020-03-13	Documents check and formalize	Shib	Shib	Liujy
1.2	2020-03-25	Update V_{I2CL} / T_{ON_DVOx} /I_{SHORT_AVOx} /I_{LMT_AVOx}	Liu Yi Guo	Liu Yi Guo	Liu Jia Ying
1.3	2023-02-15	Update Test date	Yang Zhi	Yang Zhi	Yang Zhi