Dual-Rail Ultra-Low Dropout 1.5A LDO

General Description

The ET5A5ADJZB is CMOS-based low-dropout, low-power linear regulators, offering 1500mA with NMOS pass transistor and a separate bias supply voltage(V_{BIAS}). The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application. ET5A5ADJZB consists of an accurate voltage-reference block, an error amplifier, a thermal-shutdown circuit, and a current limit circuit.

Features

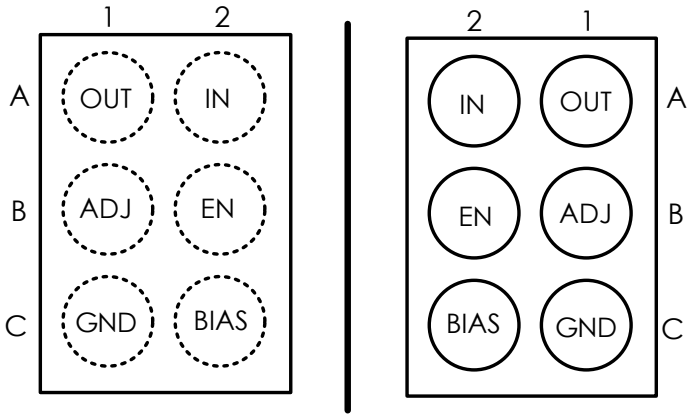
- Wide V_{IN} Voltage Range: $V_{OUT}+V_{DROP}$ to 5.5V&<V_{BIAS}
- Wide V_{BIAS} Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.5V to 3.0V
- Very Low V_{BIAS} Input Current: 60μA
- Ultra Low Dropout: 120mV at 1.5A@V_{OUT}=1V
- Built-in Over-current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit (optional)
- Built-in Under Voltage Lock-out
- Package Information:

Part No.	Package	MSL
ET5A5ADJZB	WLCSP6 (1.2mm×0.8mm×0.35mm,0.4pitch)	Level 1

Applications

- Telecom Industrial and Consumer Equipment
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Specific Start−up Time or Sequencing Requirement Applications

Pin Configuration

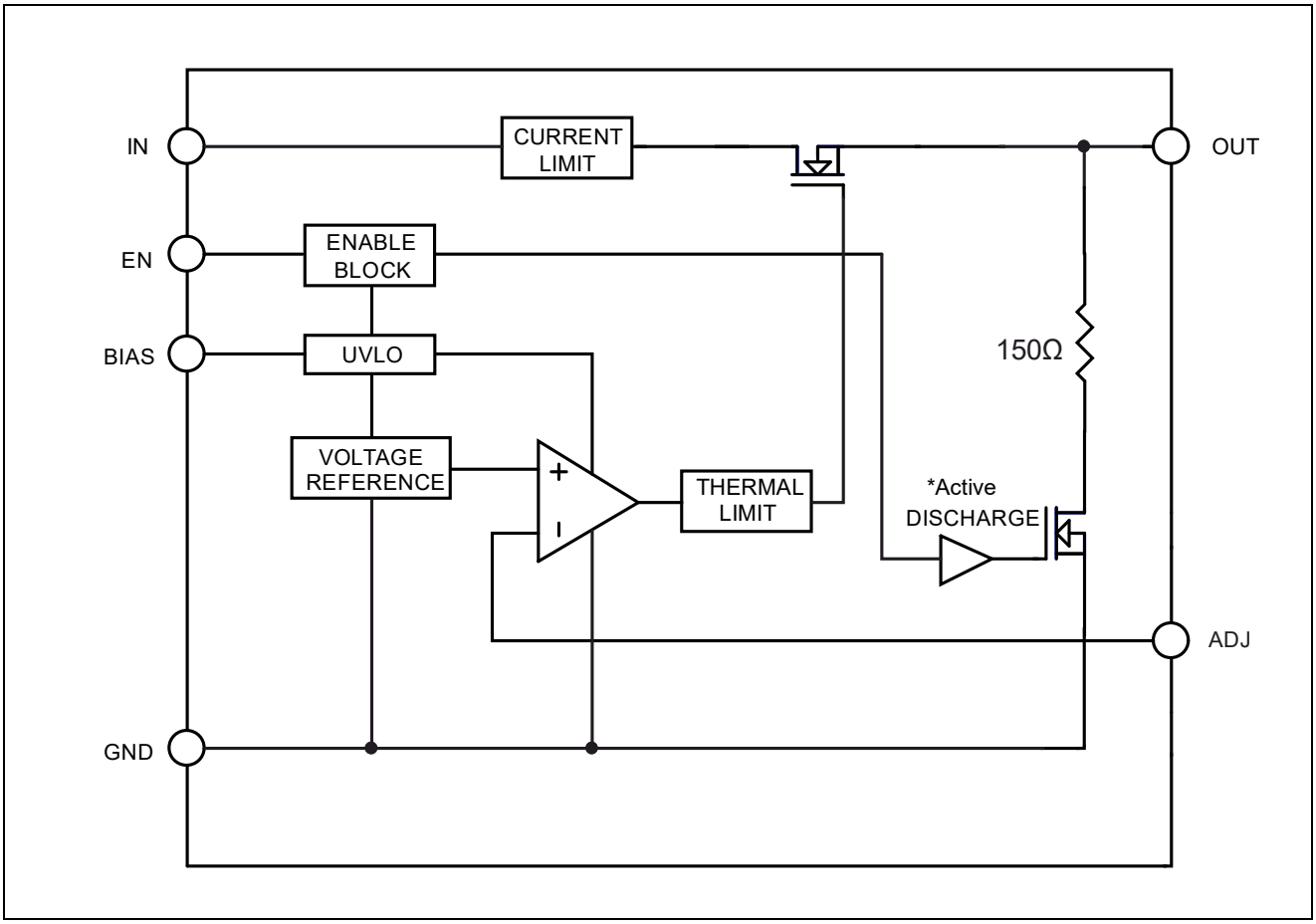


Top View Bottom View

Pin Function

Pin Name	Symbol	Pin Description
A1	OUT	The power output of the device. A 22μF (typ.) ceramic capacitor is recommended at this pin.
A2	IN	Input voltage Pin. Large bulk capacitance should be placed closely to this pin. A 10μF (typ.) ceramic capacitor is recommended at this pin.
B1	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
B2	EN	Enable Input.
C1	GND	Ground pin.
C2	BIAS	Input voltage for controlling circuit.

Block Diagram



Functional Description

The ET5A5ADJZB dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET5A5ADJZB offers smooth start-up.

Input and Output Capacitor

The device is designed to be stable for ceramic output capacitors with 4.7μF effective capacitance, greater ceramic capacitor is selected to get good dynamic performance. The device is also stable with multiple capacitors in parallel. In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} =10μF and C_{BIAS}= 1μF or greater.

Enable Pin Operation

The ET5A5ADJZB is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical

characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with V_{BIAS} to keep the LDO in operating mode.

Current Limit Protection

When output current of V_{OUT} pin is higher than current limit threshold or the V_{OUT} pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

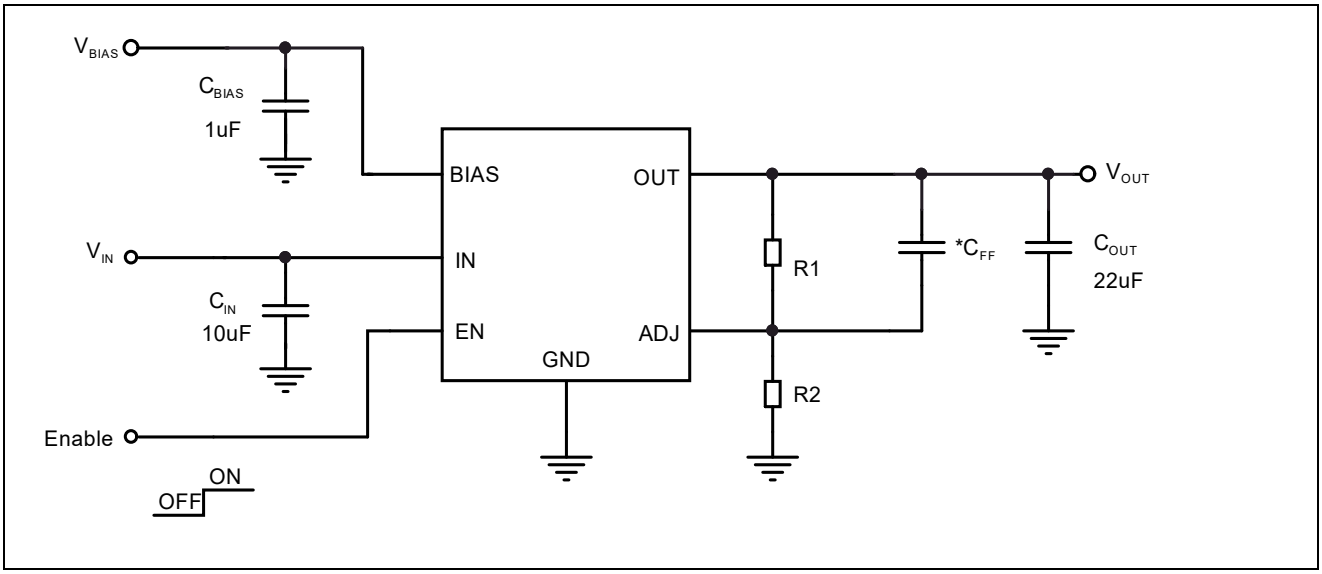
Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool down. When the junction temperature reduces to approximately +140°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from V_{REF} to 3.0 V using two external resistors. Typical application schematics is shown blow.



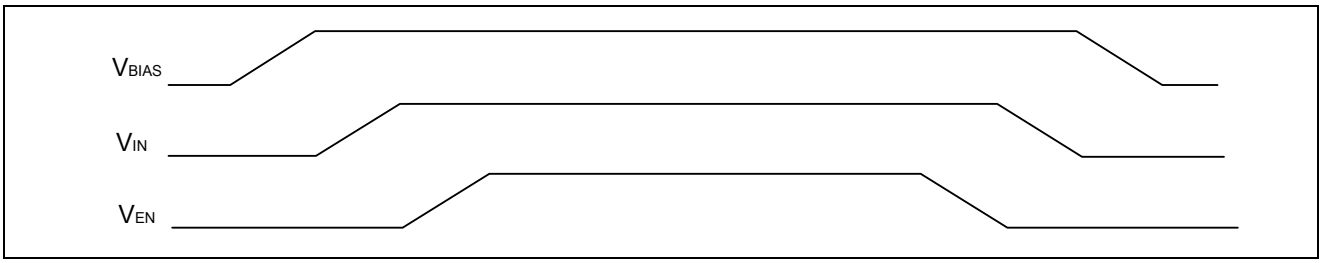
$$V_{OUT} = V_{REF} \times (1+R1/R2)$$

Typical value of V_{REF} (ADJ Pin) is 0.5V.It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100kΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

Power Up/Down Sequence Control

The recommended power on sequence of ET5A5ADJZB is to power on V_{SYS} first, then power on input power V_{IN}, then set V_{EN} to high level, and then enable LDO. The corresponding power off sequence is to turn off LDO. First, set V_{EN} to low level, then power off input power V_{IN}, and finally power off V_{SYS}.



Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage(IN Pin)	-0.3 to 6.0	V
V_{BIAS}	Input Voltage (BIAS Pin)	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V_{FB}	Input Voltage (FB Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage(OUT Pin)	-0.3 to 6.0	V
I_{OUT_MAX}	Maximum Load Current	1500	mA
$PD_{\_MAX}$	Maximum Power Consumption(PCB: 5cm × 5cm, 2layer, 1OZ)	1500	mW
T_{J_MAX}	Maximum Junction Temperature	-40 to 150	ºC
T_{STG}	Storage Temperature Range	-65 to +150	ºC
T_L	Lead Temperature (Soldering, 10 sec)	260	ºC
$R_{\theta JA}$	Thermal Resistance, Junction-to-Air	66.6	ºC/W
ESD	HBM (EIA/JESD22-A114-A)	±2	KV
	CDM (EIA/JESD22-C101-A)	±1.5	KV

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	IN Input Voltage	$V_{OUT}+V_{DROP}$ to 5.5 &$V_{IN}<V_{BIAS}$	V
V_{BIAS}	BIAS Input Voltage	2.7 to 5.5 & $V_{BIAS}>V_{OUT}+1.6V$	V
I_{OUT}	Output Current	0 to 1500	mA
T_A	Operating Ambient Temperature	-40 to 85	ºC
T_J	Operating Junction Temperature	-40 to 125	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	2.2 to 22	µF
C_{BIAS}	Effective Input Ceramic Capacitor Value	0.22 to 4.7	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	4.7 to 33	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted,V_{IN}=V_{OUT}+0.3V,V_{BIAS}= V_{OUT}+1.6V or 3.0V which is greater, I_{OUT}=10mA, C_{IN}=10μF, C_{OUT}=22μF,C_{BIAS}=1μF, T_A=-40~+85°C.Typical values are at T_A =25 ºC)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}(1)	V_{IN}≥V_{OUT}+0.15V,T_A=25ºC	V_{OUT}+ V_{DROP}		5.5&< V_{BIAS}	V
V_{BIAS} Voltage Range	V_{BIAS}	V_{BIAS}>2.7&V_{BIAS}> V_{OUT}+1.6	2.7		5.5	V
Under-voltage lock-out	V_{UVLO}	V_{BIAS} Rising	1.50	1.80	2.10	V
	V_{UVLO_H}	Hysteresis	0.10	0.26	0.45	V
V_{BIAS} Current	I_{Q_ON}	Active mode: V_{EN}=V_{BIAS}	40	60	100	μA
	I_{Q_OFF}	V_{EN}=0V		1.0	3	μA
FB Voltage	V_{FB}	T_A=25 ºC	0.495		0.505	V
		T_A=-40 to 85 ºC	0.490		0.510	V
Output Voltage	V_{OUT}		0.5		3.0	V
Dropout Voltage	V_{DROP}(2)	I_{OUT}=500mA,V_{OUT}=1.0V		35	55	mV
		I_{OUT}=1000mA,V_{OUT}=1.0V		75	110	
		I_{OUT}=1500mA,V_{OUT}=1.0V		120	180	
Current Limit	I_{LIM}	V_{IN}=V_{OUT}+0.2V,T_A=25ºC	1.8	2.5	3.8	A
Short Current Limit	I_{SHORT}	V_{OUT}=0V	400	700	1100	mA
Load Regulation	Reg_{LOAD}	1mA≤I_{OUT}≤1500mA V_{OUT}=1.0V		2	25	mV
V_{IN} Line Regulation	Reg_{LINE}	V_{OUT}+0.3V≤V_{IN}≤5V V_{OUT}=1.0V		0.01	0.1	%/V
V_{BIAS} Line Regulation		2.7V<V_{BIAS}<5.5V, (V_{BIAS}>V_{OUT}+1.6)V_{OUT}=1.0V		0.01	0.1	%/V
Ripple Rejection	PSRR(3)	V_{IN} to V_{OUT} , f=1kHz, V_{IN}=V_{OUT}+0.5V,V_{OUT}=1.0V, Ripple 0.2Vp-p, I_{OUT}=30mA	60	75		dB
		V_{BIAS} to V_{OUT},f=1kHz, V_{IN}=V_{OUT}+0.5V,V_{OUT}=1.0V, Ripple 0.2Vp-p,I_{OUT}=30mA	55	70		
Output Noise	e_N(3)	V_{IN}=V_{OUT}+0.5V, f=10 Hz to 100 kHz, I_{OUT}=1mA	40* V_{OUT}	60* V_{OUT}	120* V_{OUT}	μV_{RMS}
EN Pull-down Current	I_{EN}	V_{EN}=5.5V,V_{BIAS}=5.5V		0.9	3	μA
EN Input Voltage High	V_{ENH}		0.9		5.5	V
EN Input Voltage Low	V_{ENL}		0		0.4	V
Output resistance of auto discharge at off state	R_{DIS}	V_{EN}=0V,V_{OUT}=0.5V	85	150	250	Ω

Electrical Characteristics(Continued)

(Unless otherwise noted,V_{IN}=V_{OUT}+0.3V,V_{BIAS}=3.0V,I_{OUT}=10mA,C_{IN}=10μF,C_{OUT}=22μF,C_{BIAS}=1μF, T_A=-40~+85°C.Typical values are at.T_A =25 ºC)

Load transient	V_{TRLD}[3]	I_{OUT}=1mA to 1500mA in 10us V_{IN}= V_{OUT}+0.2V,T_A=25ºC		65* V_{OUT}	85* V_{OUT}	mV
		I_{OUT}=1500mA to 1mA in 10us V_{IN}= V_{OUT}+0.2V,T_A=25 ºC		65* V_{OUT}	85* V_{OUT}	mV
Turn-On Time	T_{ON}	V_{OUT}=1.0V, From assertion of V_{EN} to V_{OUT}=90%$V_{OUT(NOM)}$	150	230	450	μs
Rise Time	T_R	V_{OUT}=1.0V, From assertion of V_{OUT}=10% to 90%$V_{OUT(NOM)}$	40	120	260	μs
Thermal shutdown threshold	T_{TSD}[3]	T_J rising	145	160	175	ºC
Thermal shutdown hysteresis	T_{HYS}[3]	T_J falling from shutdown	15	20	30	ºC

Notes:

1: The maximum input voltage should take into account the maximum power consumption (PD(max)). The calculation formula is as follows:

$$\mathbf{PD(max)= (V_{IN}(max)- V_{OUT})\times I_{OUT}}$$

The maximum power consumption of the circuit is 1500mW.

$$\mathbf{V_{IN(max)}=1500mW/I_{OUT}+V_{OUT}}$$

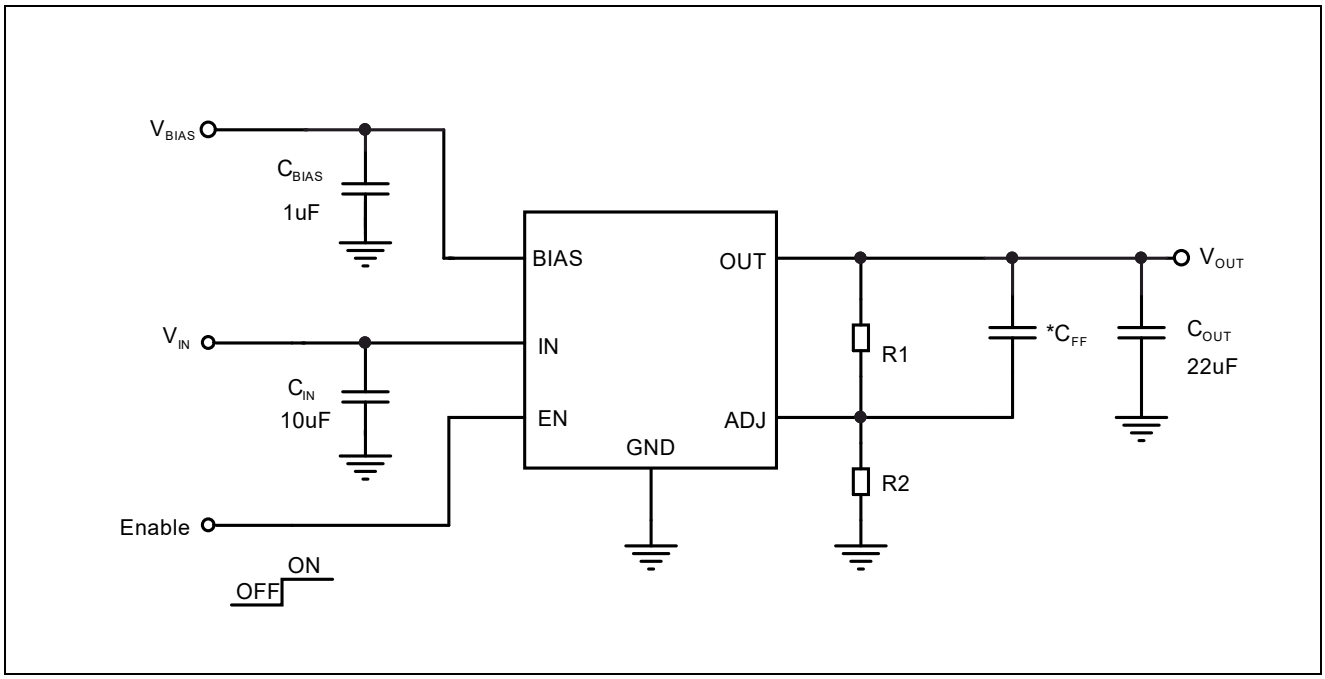
For example:

If V_{OUT}= 1.0V,I_{OUT} =1500mA, The maximum input voltage is V_{IN}(max)=1500mW/1500mA+1.0=2.0V

2: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET}+$V_{DROPMAX}$ with output current.

3: Guaranteed by design and characterization. not a FT item.

Application Circuits

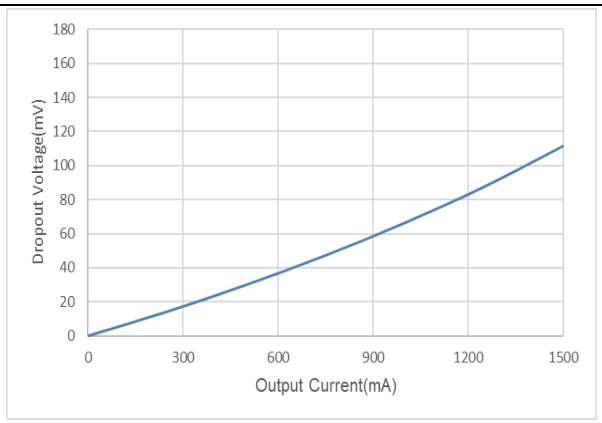


Note*:V_{OUT} = 0.5×(1+R1/R2), (R1+R2) no greater than 100kΩ. The feedforward capacitor C_{FF} is optional for the optimization of transient response , suggested value is 10nF.

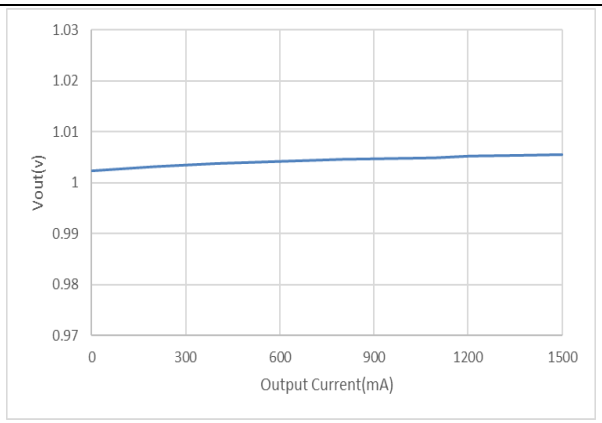
Typical Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

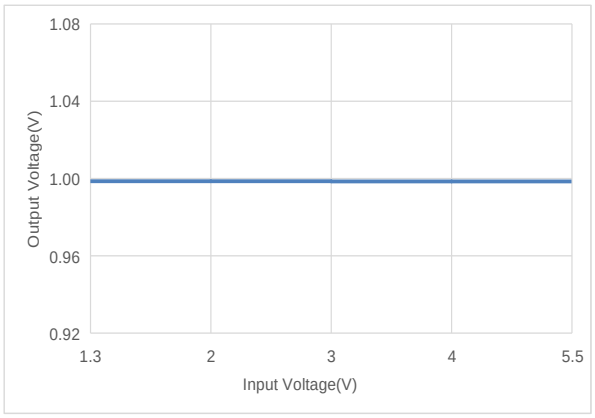
(V_{IN}=1.30V, V_{BIAS}= 3.0V, I_{OUT}=1mA, C_{IN}=10μF,C_{OUT}=22μF, C_{BIAS}=1μF，V_{OUT}=1V)



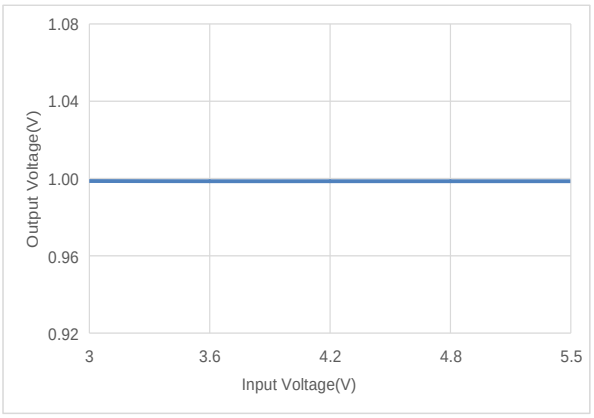
Dropout Voltage vs. Output Current



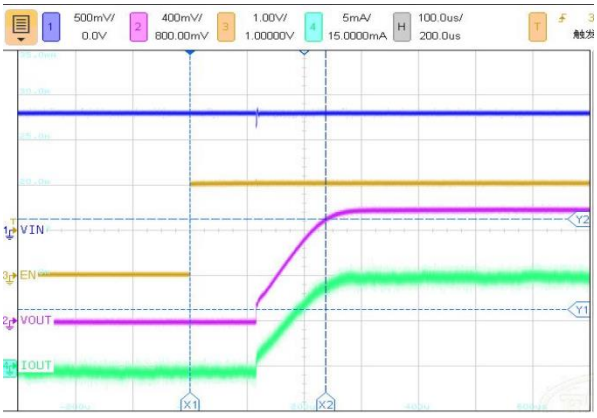
Output Voltage VS Output Current



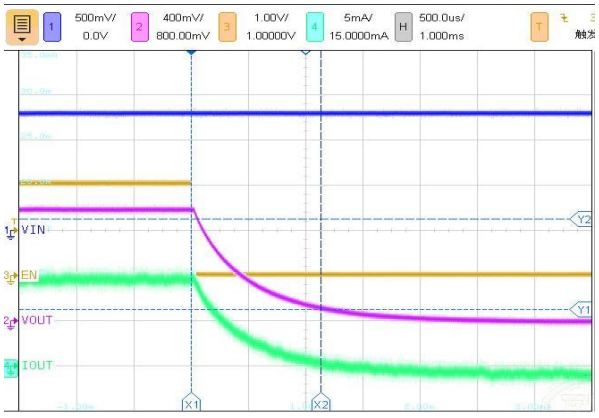
Output Voltage VS IN Input Voltage



Output Voltage VS BIAS Input Voltage



Turn On VS EN Voltage (I_{OUT}=10mA)

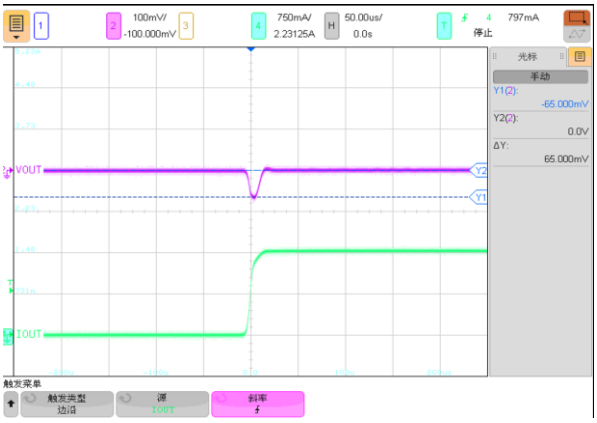


Turn Off VS EN Voltage (I_{OUT}=10mA)

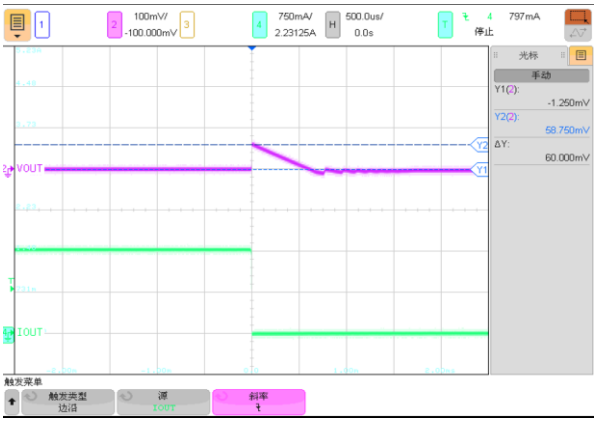
Typical Characteristics (Continued)

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

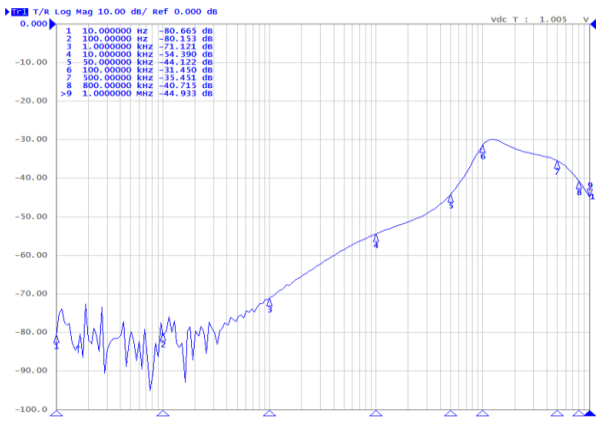
(V_{IN}=1.30V, V_{BIAS}= 3.0V, I_{OUT}=1mA, C_{IN}=10μF,C_{OUT}=22μF, C_{BIAS}=1μF，V_{OUT}=1V)



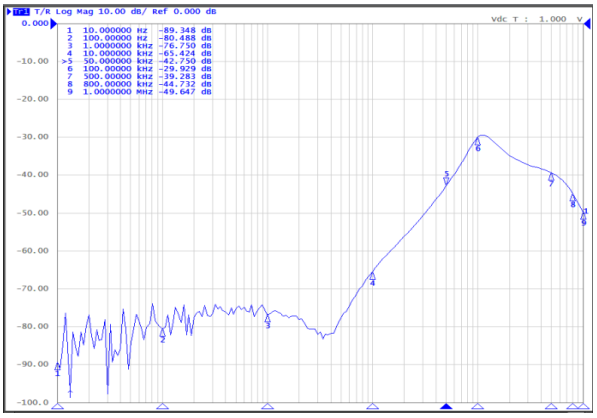
Load Transient Response(I_O=1~1500mA)



Load Transient Response(I_O=1500~1mA)



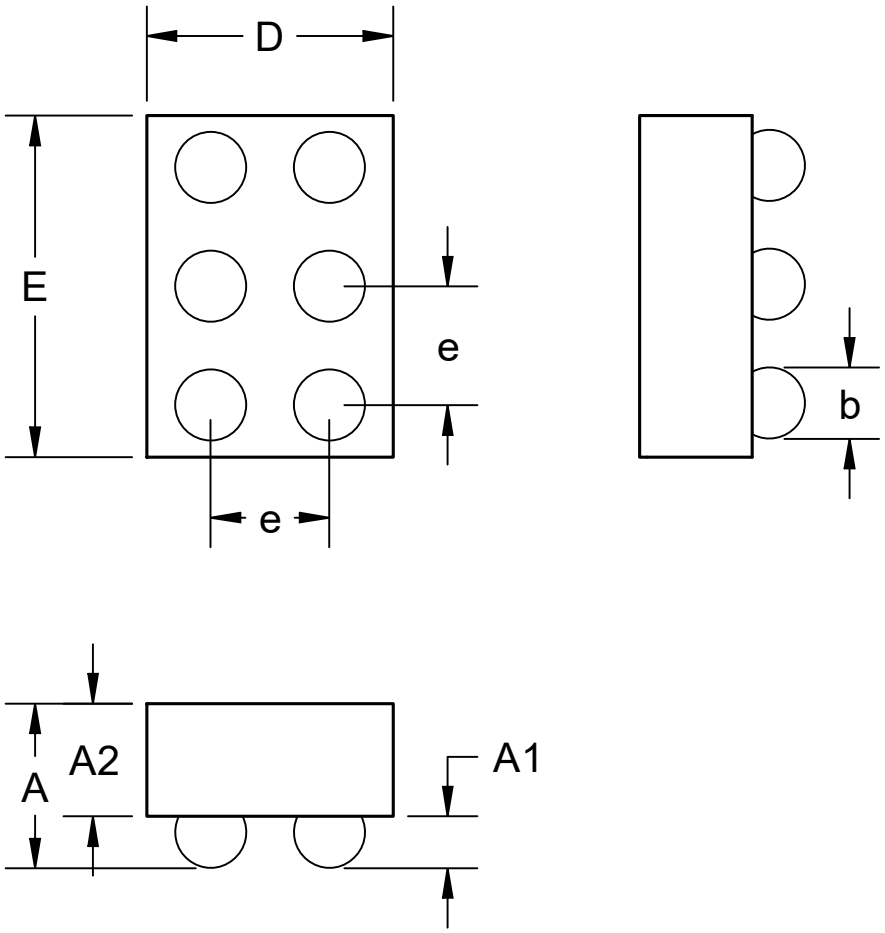
VIN PSRR VS I_{OUT}(I_{OUT}=30mA)



VBIAS PSRR VS I_{OUT}(I_{OUT}=30mA)

Package Dimension

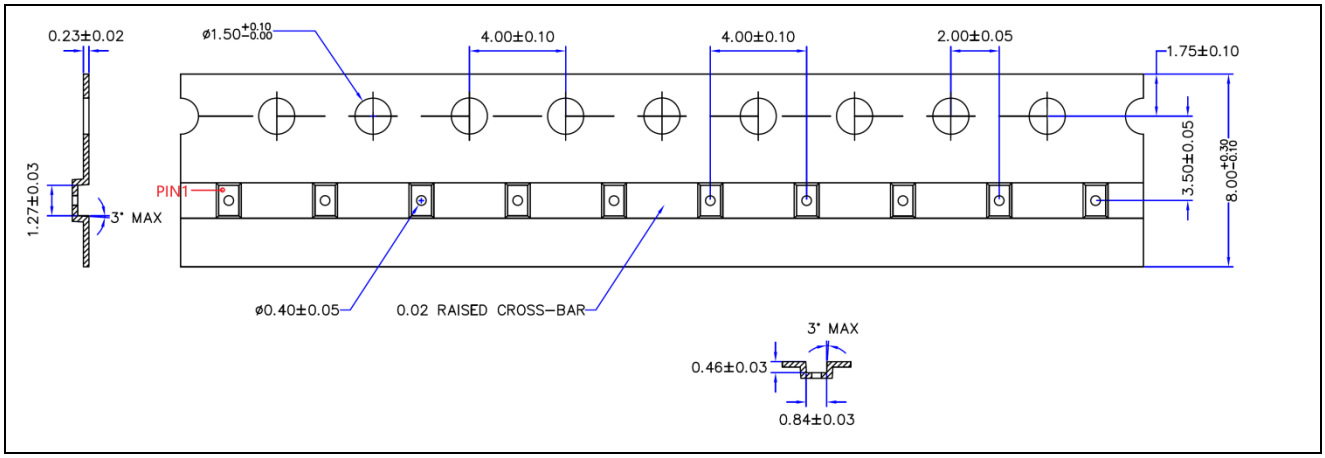
WLCSP6



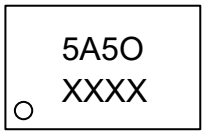
Dimensions Table (Units: mm)

Symbol	Min	Nom	Max
A	0.32	0.36	0.40
A1	0.06	0.08	0.10
A2	0.26	0.28	0.30
b	0.22	0.24	0.26
D	0.754	0.774	0.804
E	1.156	1.176	1.206
e	0.400 BSC		

Tape Information



Marking Information



5A5O - Part Number

XXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-12-26	Preliminary Version	Tugz	Liuxm	Liujy
1.0	2023-04-16	Official Version	Tugz	Liuxm	Liujy
1.1	2023-05-26	Add Vin Range &Dropout	Tugz	Liuxm	Liujy
1.2	2023-09-05	Update V_{BIAS} ,C_{IN},C_{OUT} Rang	Wangp	Liuxm	Liujy
1.3	2024-05.31	Add SPEC Rang	Tugz	Liuxm	Liujy