Dual-Rail Ultra-Low Dropout 1A LDO

General Description

The ET5A3ADJZB is CMOS-based low-dropout, low-power linear regulators, offering 1000mA with NMOS pass transistor and a separate bias supply voltage(V_{BIAS}). The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application. ET5A3ADJZB consists of an accurate voltage-reference block, an error amplifier, a thermal shutdown circuit, and a current limit circuit.

Features

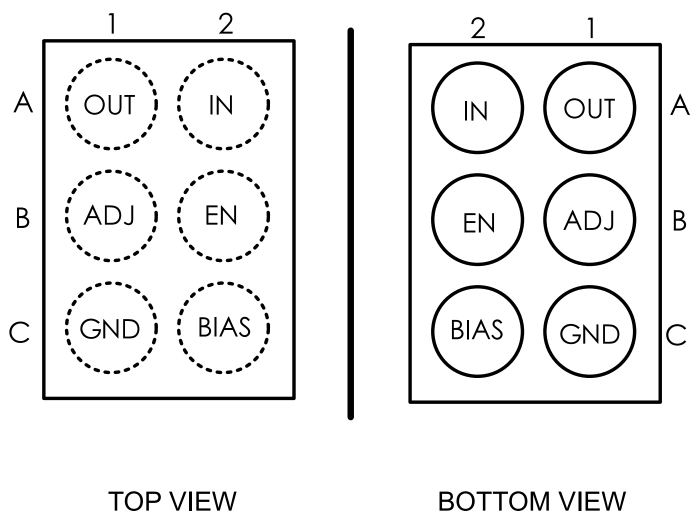
- Wide V_{IN} input voltage range from V_{OUT}+0.15V to 5.5V
- Wide V_{BIAS} voltage range from 3.0V to 5.5V
- Output voltage range from 0.5V to 3.0V adjustable
- Very low V_{BIAS} input current of typical 100μA
- Ultra low dropout is typical 40mV at 1000mA load
- Built-in over-current protection and thermal shutdown circuit
- Built-in auto-discharging circuit (optional)
- Built-in under voltage lock-out
- Part No. and package

Part No.	Package	MSL
ET5A3ADJZB	WLCSP6 (1.15mm×0.75mm,0.4 pitch)	Level 1

Applications

- Constant-voltage power supply for battery-powered device
- Constant-voltage power supply for smartphones, tablets
- Constant-voltage power supply for cameras, DVRs, STB and camcorders

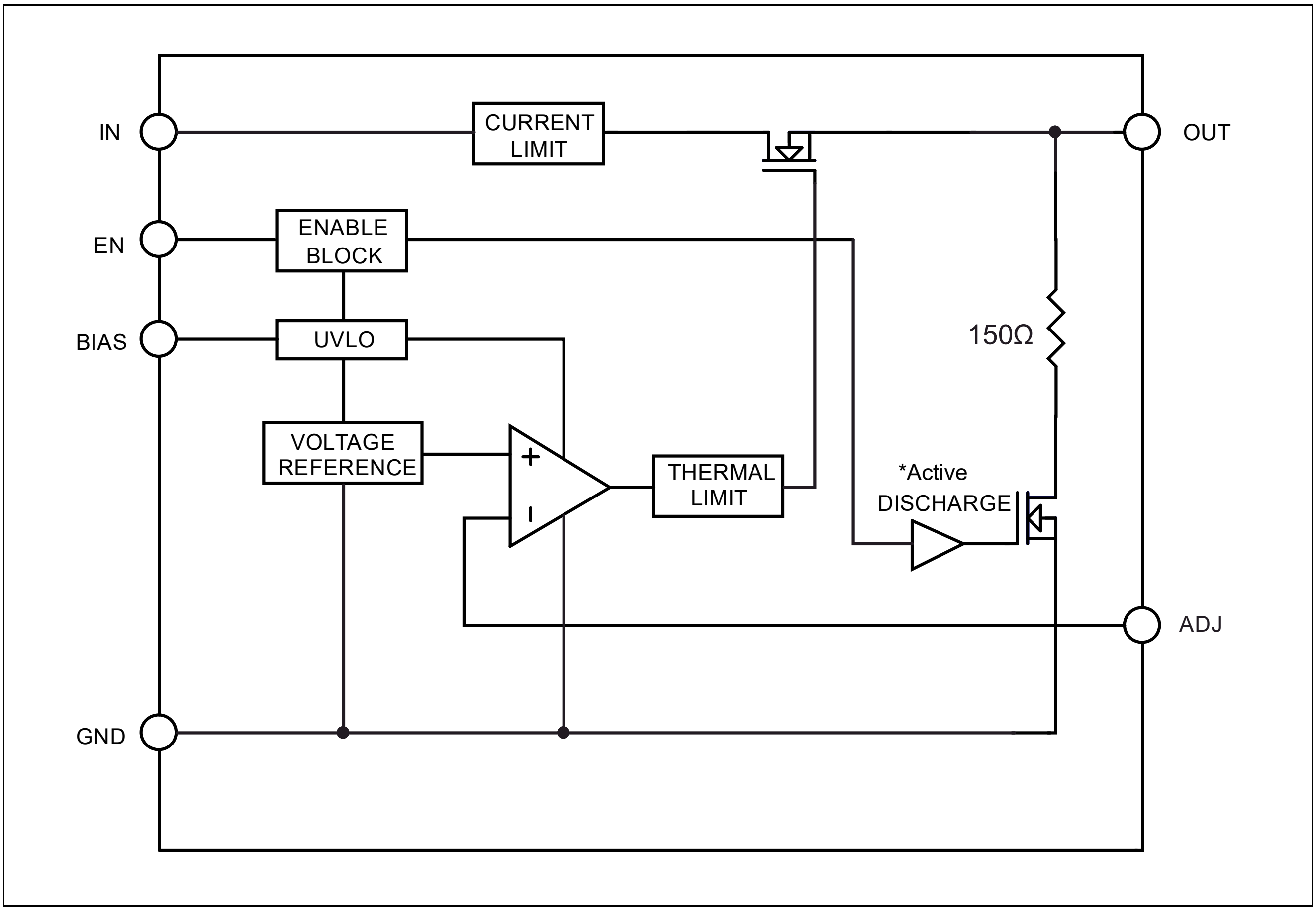
Pin Configuration



Pin Function

Pin Name	Symbol	Pin Description
A1	OUT	The power output of the device. A 22μF (typ.) ceramic capacitor is recommended at this pin.
A2	IN	Input voltage Pin. Large bulk capacitance should be placed closely to this pin. A 10μF (typ.) ceramic capacitor is recommended at this pin.
B1	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
B2	EN	Enable Input.
C1	GND	Ground pin.
C2	BIAS	Input voltage for controlling circuit.

Block Diagram



Functional Description

The ET5A3ADJZB dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET5A3ADJZB offers smooth start-up.

Input and output Capacitor

The device is designed to be stable for ceramic output capacitors with 22μF capacitance. The device is also stable with multiple capacitors in parallel. In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} =10μF and C_{BIAS}= 1μF or greater.

Enable Pin Operation

The ET5A3ADJZB is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with V_{BIAS} to keep the LDO in operating mode.

Current Limit Protection

When output current of V_{OUT} pin is higher than current limit threshold or the V_{OUT} pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

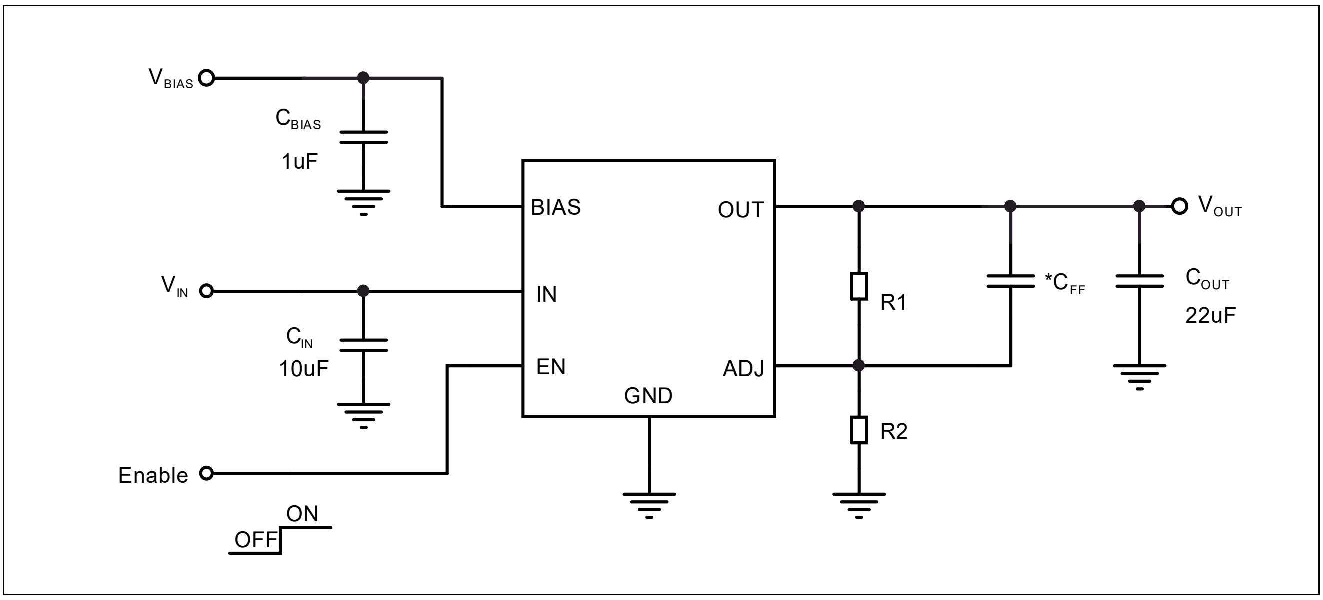
Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool down. When the junction temperature reduces to approximately +140°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from VREF to 3.0 V using two external resistors. Typical application schematics is shown blow.



$$V_{OUT} = V_{REF} \times (1 + R1/R2)$$

Typical value of V_{REF} (ADJ Pin) is 0.5V. It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100kΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

Absolute Maximum Ratings

Item	Rating	Unit
Input Voltage (IN Pin)	-0.3 to 6.0	V
Input Voltage (BIAS Pin)	-0.3 to 6.0	V
Input Voltage (EN Pin)	-0.3 to 6.0	V
Input Voltage (FB Pin)	-0.3 to 6.0	V
Output Voltage (OUT Pin)	-0.3 to 6.0	V
Maximum Load Current	1000	mA
Maximum Power Consumption	1150	mW
Operating Junction Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering, 10 sec)	260	°C

Recommended Operating Conditions

Symbol	Items	Rating	Unit
V_{IN}	IN Input Voltage	V_{OUT}+0.15V to 5.5	V
V_{BIAS}	BIAS Input Voltage	3 to 5.5 & V_{BIAS}>V_{OUT}+1.6V	V
I_{OUT}	Output Current	0 to 1000	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	4.7 to 22	µF
C_{BIAS}	Effective Input Ceramic Capacitor Value	0.22 to 4.7	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	6.8 to 33	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

（Unless otherwise noted , V_{IN}=V_{OUT}+0.3V, V_{BIAS}= 3.0V, I_{OUT}=10mA, C_{IN}=10μF,C_{OUT}=22μF, C_{BIAS}=1μF , T_A = -40°C ~85°C. Typical values are at. T_A=25°C）

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}[1][4]	V_{IN} ≥V_{OUT}+0.15V, T_A=25 ºC	V_{OUT}+ 0.15V		5.5	V
V_{BIAS} Voltage Range	V_{BIAS}	V_{BIAS} >3.0V&V_{BIAS} >V_{OUT}+1.6V	3.0		5.5	V
Under-voltage lock-out	V_{UVLO}	V_{BIAS} Rising	1.25	1.6	1.95	V
	V_{UVLO_H}	Hysteresis	0.05	0.2	0.35	V
V_{BIAS} Current	I_{Q_ON}	Active mode: V_{EN}=V_{BIAS}		100	160	μA
	I_{Q_OFF}	V_{EN}=0V		0.2	1	μA
FB Voltage	V_{FB}[5]	T_A=25 ºC	0.495		0.505	V
Output Voltage	V_{OUT}		0.5		3.0	V
Dropout Voltage	V_{DROP}[2]	I_{OUT}=500mA,V_{OUT}=1.05V	10	20	35	mV
		I_{OUT}=1000mA,V_{OUT}=1.05V	20	40	70	
Current Limit	I_{LIM}[4]	V_{IN}=V_{OUT}+0.2V,T_A=25 ºC	1.05	1.4	2.1	A
Load Regulation	Reg_{LOAD}	1mA≤I_{OUT}≤1000mA V_{OUT}=1.05V		2	10	mV
V_{IN} Line Regulation	Reg_{LINE}	V_{OUT}+0.3V≤V_{IN}≤5V, V_{OUT}=1.05V		0.01	0.1	%/V
V_{BIAS} Line Regulation		3.0V < V_{BIAS} < 5.5V , (V_{BIAS}> V_{OUT}+1.6),V_{OUT}=1.05V		0.01	0.1	%/V
Ripple Rejection	PSRR[3]	V_{IN} to V_{OUT} , f=1kHz, V_{IN}=V_{OUT}+0.5V,V_{OUT}=1.05V, Ripple 0.2Vp-p, I_{OUT}=30mA	60	75		dB
		V_{BIAS} to V_{OUT} , f=1kHz, V_{IN}=V_{OUT}+0.5V, V_{OUT}=1.05V, Ripple 0.2Vp-p, I_{OUT}=30mA	60	75		
Output Noise	e_N[3]	V_{IN}= V_{OUT}+0.5V, f= 10 Hz to 100 kHz, I_{OUT}=1mA		30* V_{OUT}	60* V_{OUT}	μV_{RMS}
EN Pull-down Current	I_{EN}	V_{EN}=5.5V, V_{BIAS}=5.5V		0.3	1	μA
EN Input Voltage High	V_{ENH}		0.9			V
EN Input Voltage Low	V_{ENL}				0.4	V
Output Resistance of Auto Discharge at Off State	R_{DIS}	V_{EN}=0V, V_{OUT} =0.5V	80	150	220	Ω

Electrical Characteristics(Continued)

（Unless otherwise noted , V_{IN}=V_{OUT}+0.3V, V_{BIAS}= 3.0V, I_{OUT}=10mA, C_{IN}=10μF,C_{OUT}=22μF, C_{BIAS}=1μF , T_A = -40°C ~85°C. Typical values are at. T_A=25°C）

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Transient	V_{TRLN}(3)	V_{IN}= V_{OUT+}0.3V to V_{OUT}+1.3 in 10us, I_{OUT}=1mA，T_A=25 ºC		3	12	mV
		V_{IN}= V_{OUT+}1.3V to V_{OUT}+0.3 in 10us, I_{OUT}=1mA，T_A=25 ºC		3	12	mV
Load Transient	V_{TRLD}(3)	I_{OUT}=1mA to 1000mA in 10us V_{IN}= V_{OUT}+0.2V, T_A=25 ºC		80	100	mV
		I_{OUT}=1000mA to 1mA in 10us V_{IN}= V_{OUT}+0.2V, T_A=25 ºC		60	80	mV
Turn-On Time	t_{ON}(3)	V_{OUT}=1.05V, From assertion of V_{EN} to V_{OUT}=90%$V_{OUT(NOM)}$	50	110	200	μs
Rise Time	t_R	V_{OUT}=1.05V, From assertion of V_{OUT}=0 to V_{OUT}=90%$V_{OUT(NOM)}$	30	90	170	μs
Thermal Shutdown Threshold	T_{TSD}(3)	T_J rising	140	160	175	°C
Thermal Shutdown Hysteresis	T_{HYS}(3)	T_J falling from shutdown	10	20	35	°C

Notes:

1: Here V_{IN} means internal circuit can work normal. If V_{IN} <V_{OUT}, Output voltage follow V_{IN}(I_{OUT}=1mA), circuit is safety. The maximum input voltage should take into account the maximum power consumption (PD(max)). The calculation formula is as follows:

$$P_D(max) = (V_{IN}(max) - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the circuit is 1150mW.

$$V_{IN}(max) = 1150mW / I_{OUT} + V_{OUT}$$

For example:

If V_{OUT}= 1.05V,I_{OUT} =1000mA, The maximum input voltage is V_{IN}(max)=1150mW/1000mA+1.05=2.2V

2: V_{DROP} FT test method: test the V_{OUT} voltage at Vset +$V_{DROPMAX}$ with output current.

3: Guaranteed by design and characterization. not a FT item.

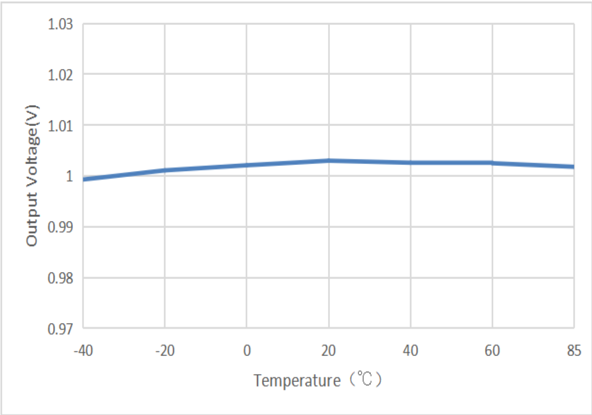
4: I_{LIM} condition if : V_{IN}<V_{OUT}+0.15V,I_{LIM} will bigger than 2.2A.

5: V_{FB} is ADJ feedback voltage, equal to V_{REF}. When OUT and ADJ are short circuited together, V_{OUT} = V_{REF}.

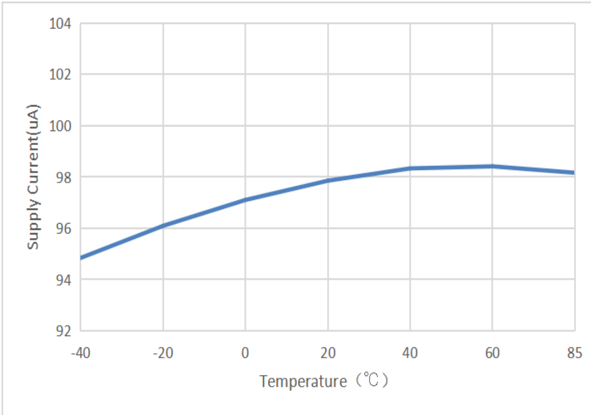
Typical Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

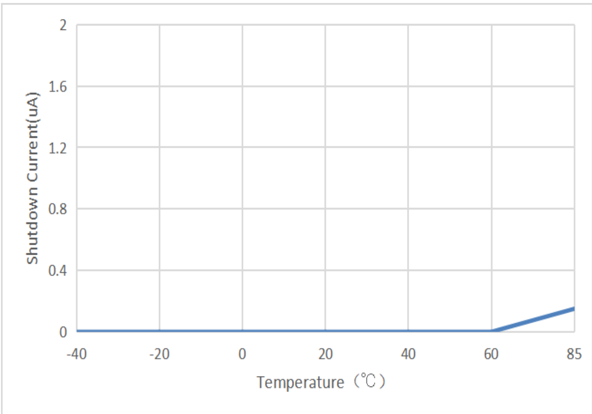
(V_{IN}=1.30V, V_{BIAS}= 3.0V, I_{OUT}=1mA, C_{IN}=10μF,C_{OUT}=10μF, C_{BIAS}=1μF，V_{OUT}=1V)



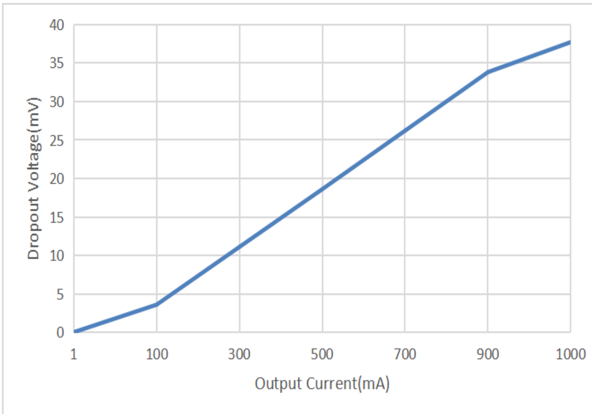
Output Voltage vs. Temperature



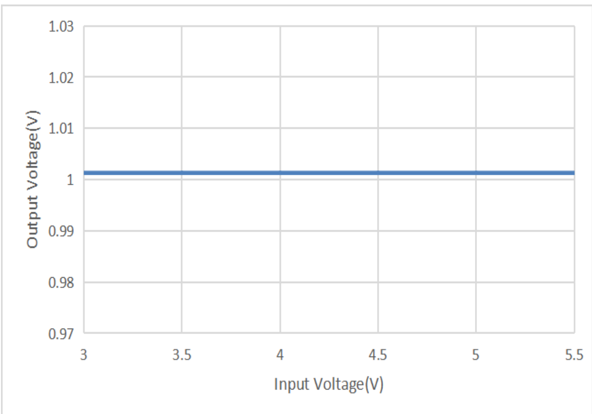
Supply Current vs. Temperature



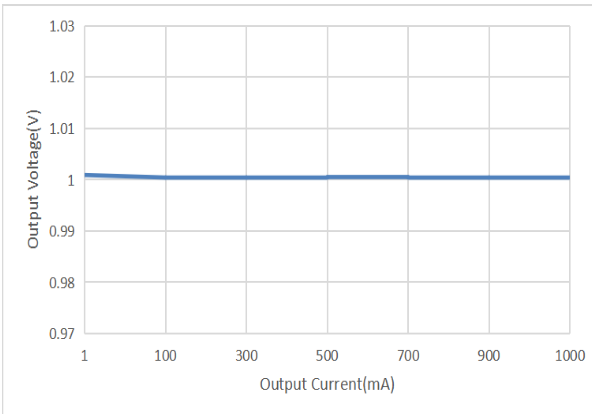
Shutdown Current VS Temperature



Dropout Voltage vs. Output Current



Output Voltage VS Input Voltage

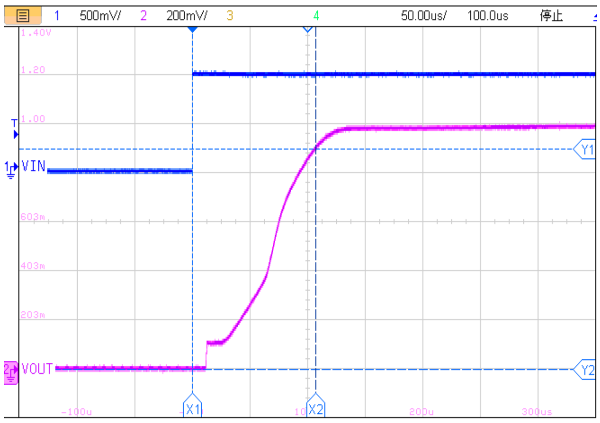


Output Voltage VS Output Current

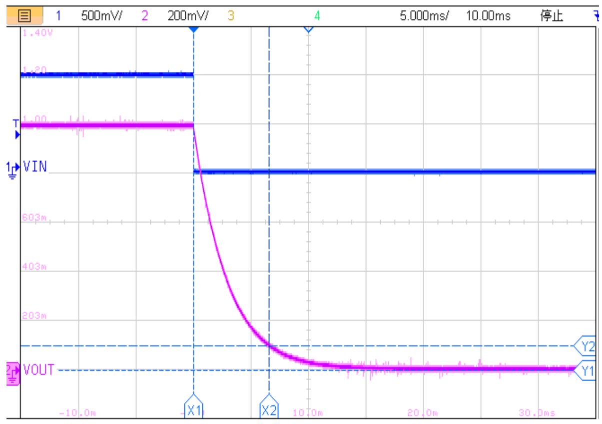
Typical Characteristics (Continued)

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

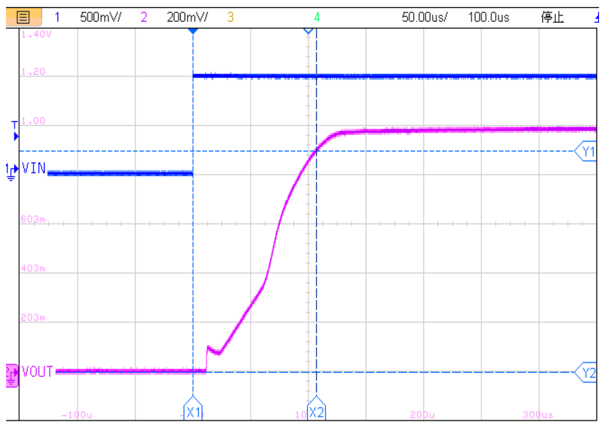
(V_{IN}=1.30V, V_{BIAS}= 3.0V, I_{OUT}=1mA, C_{IN}=10μF,C_{OUT}=10μF, C_{BIAS}=1μF， V_{OUT}=1V)



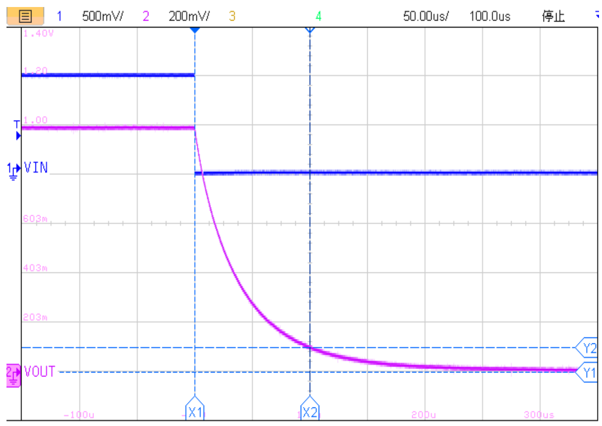
Turn On VS EN Voltage (I_{OUT}=0mA)



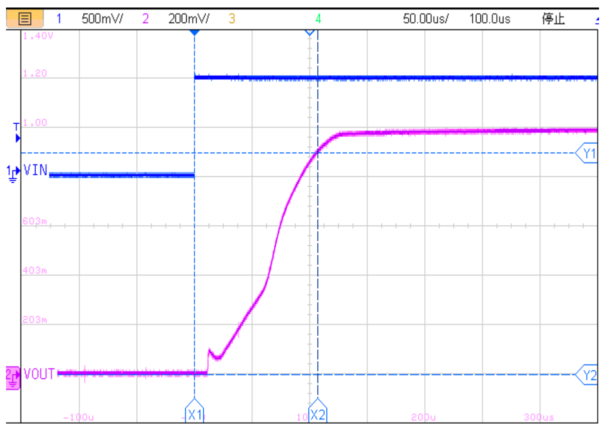
Turn Off VS EN Voltage (I_{OUT}=0mA)



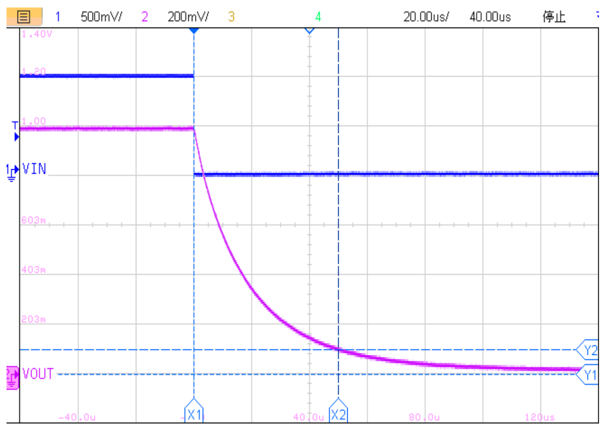
Turn On VS EN Voltage (I_{OUT}=500mA)



Turn Off VS EN Voltage (I_{OUT}=500mA)



Turn On VS EN Voltage (I_{OUT}=1000mA)

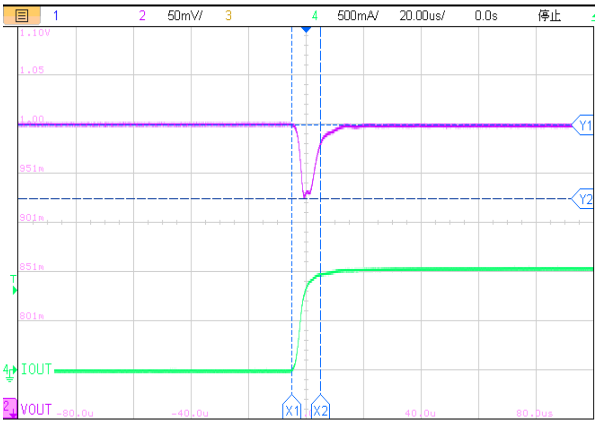


Turn Off VS EN Voltage (I_{OUT}=1000mA)

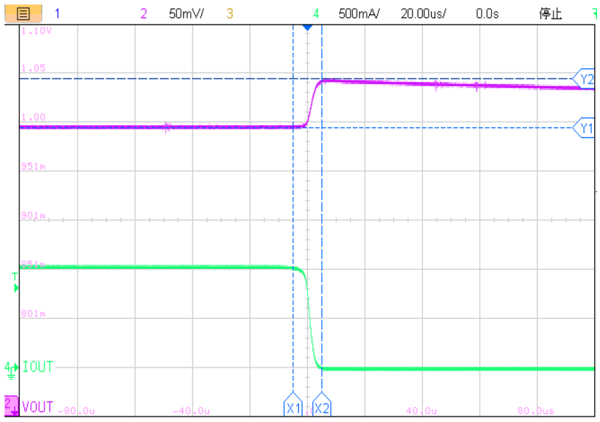
Typical Characteristics (Continued)

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

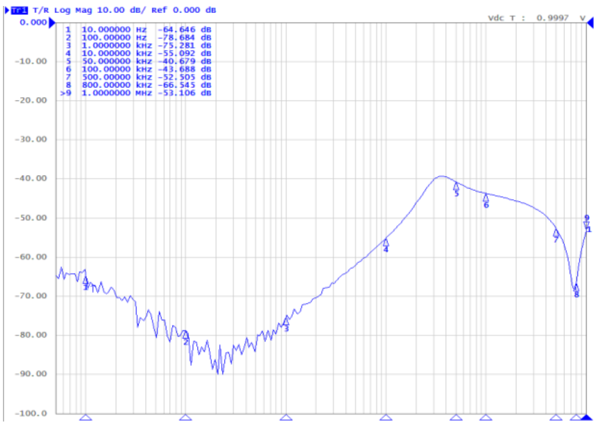
(V_{IN}=1.30V, V_{BIAS}= 3.0V, I_{OUT}=1mA, C_{IN}=10μF,C_{OUT}=10μF, C_{BIAS}=1μF， V_{OUT}=1V)



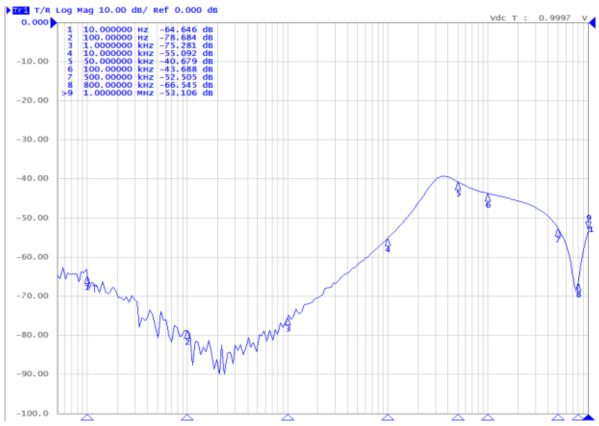
Load Transient Response(I_O=1~1000mA)



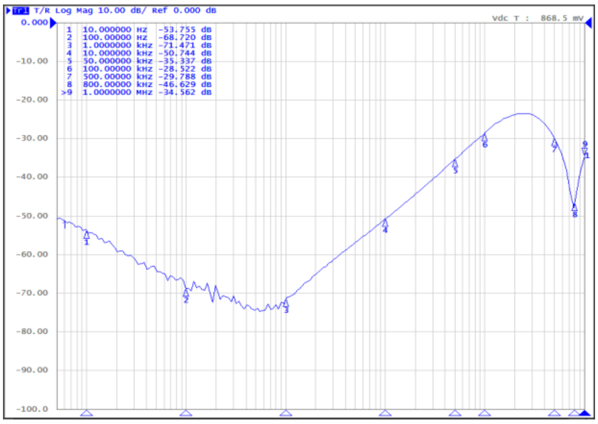
Load Transient Response(I_O=1000~1mA)



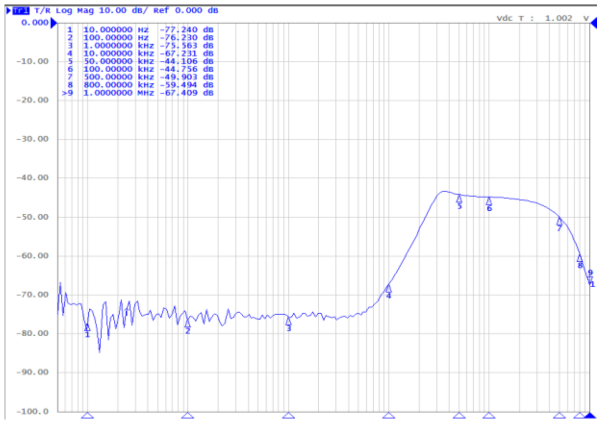
VIN PSRR VS I_{OUT}(I_{OUT}=30mA)



VIN PSRR VS I_{OUT}(I_{OUT}=500mA)



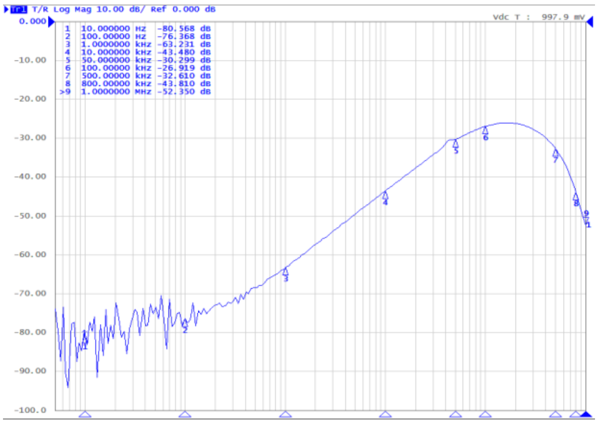
VIN PSRR VS I_{OUT}(I_{OUT}=1000mA)



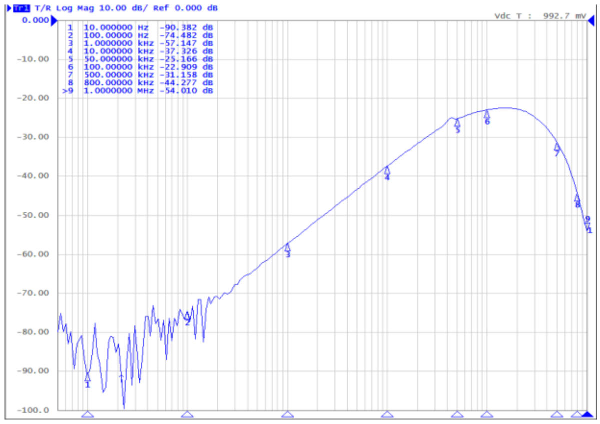
VBIAS PSRR VS I_{OUT}(I_{OUT}=30mA)

Typical Characteristics (Continued)

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.
(V_{IN}=1.30V, V_{BIAS}= 3.0V, I_{OUT}=1mA, C_{IN}=10μF,C_{OUT}=10μF, C_{BIAS}=1μF， V_{OUT}=1V)

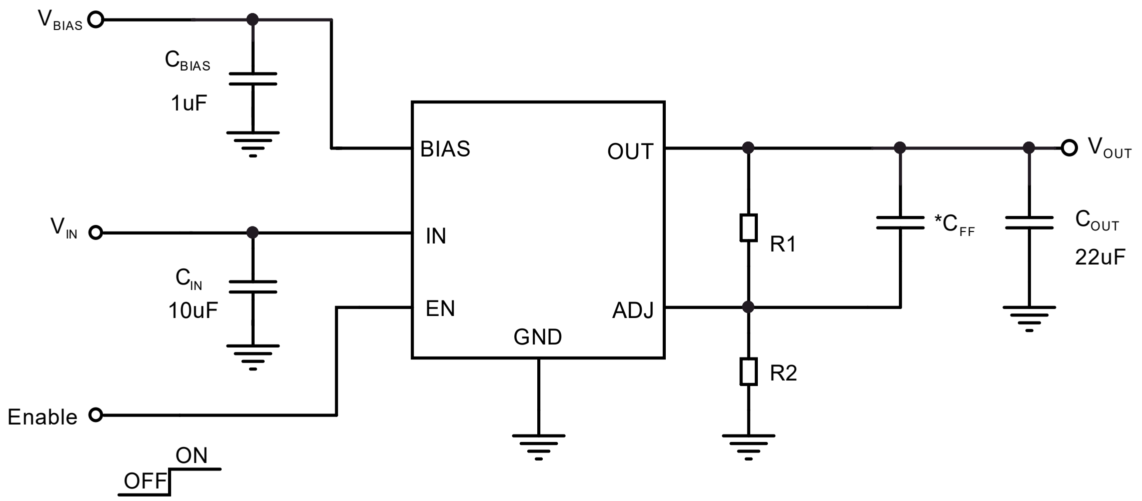


VBIAS PSRR VS I_{OUT}(I_{OUT}=500mA)



VBIAS PSRR VS I_{OUT}(I_{OUT}=1000mA)

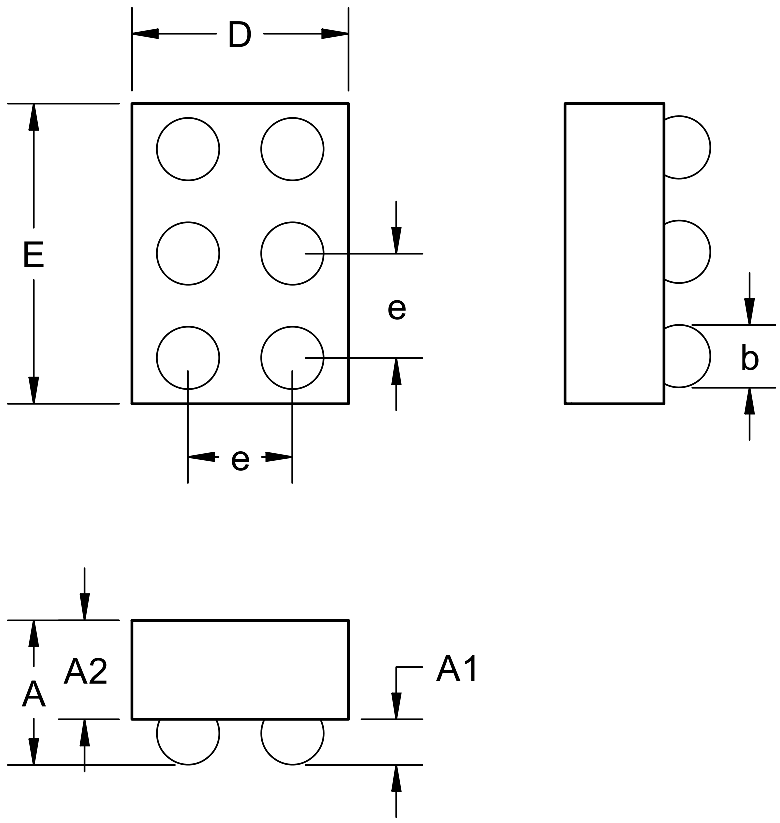
Application Circuits



Note*: V_{OUT} = 0.5×(1+R1/R2), (R1+R2) no greater than 100kΩ,the feedforward capacitor CFF is optional for the optimization of transient response,suggested value is 10nF.This electric circuit only supplies for reference.

Package Dimension

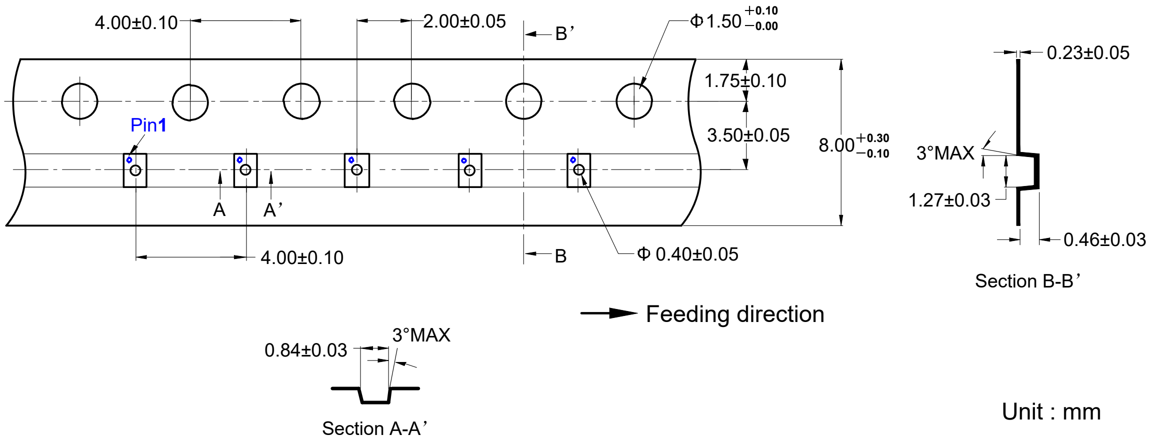
WLCSP6 (1.15mm×0.75mm)



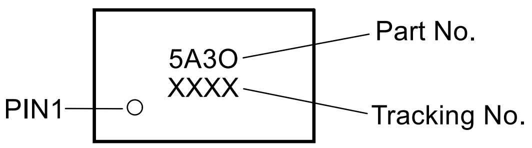
Dimensions Table (Units: mm)

Symbol	Min	Nom	Max
A	0.32	0.37	0.42
A1	0.06	0.08	0.10
A2	0.26	0.29	0.32
b	0.21	0.24	0.27
D	0.72	0.75	0.78
E	1.12	1.15	1.18
e	0.400BSC		
f	0.175BSC		

Tape



Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0	2019-08-19	Preliminary Version	Liuyg	Liuyg	Liujy
1.0	2019-10-30	Initial Version	Liuyg	Liuyg	Liujy
1.1	2019-11-15	Update test condition and value of I_{LIM}	Liuyg	Liuyg	Liujy
1.2	2019-12-18	Update Package Dimension	Liuyg	Liuyg	Liujy
1.3	2019-12-27	Update Application Circuit	Liuyg	Liuyg	Liujy
1.4	2020-05-30	Update EC table	Liuyg	Liuyg	Liujy
1.5	2020-06-11	Add I_{LIM} notice	Liuyg	Liuyg	Liujy
1.6	2020-06-17	Add Tape Information	Liuyg	Liuyg	Liujy
1.7	2020-07-07	Update VIN test conditions and add note 5 for VFB	Liuyg	Liuyg	Zhujl
1.8	2020-08-28	Modified from' V_{OUT} to 5.5V' to 'V_{OUT}+0.15V to 5.5V' in Features	Liuyg	Liuyg	Zhujl
1.9	2020-09-22	Update current limit in EC table	Liuyg	Liuyg	Zhujl
2.0	2020-10-28	Add Marking	Liuyg	Liuyg	Liujy
2.1	2021-1-22	Add T_R in EC table	Liuyg	Liuyg	Liujy
2.2	2021-2-3	Add Typical Characteristic Graph	Shib	Shib	Liujy
2.3	2021-7-13	Correct Typo in Typical Characteristics graph	Shib	Shib	Liujy
2.4	2022-8-23	Update Typeset	Lic,Shib	Shib	Liujy