800mA Dual-rail Very Low Dropout LDO

General Description

The ET551ADJY1B is a CMOS-based low-dropout, low-power linear regulators, offering 800mA with NMOS pass transistor and a separate bias supply voltage (VBIAS) . The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application. The ET551ADJY1B series consist of an accurate voltage-reference block, an error amplifier, a thermal-shutdown circuit, and a current limit circuit.

The ET551ADJY1B is available in the DFN6(1.2mm ×1.2mm) package.

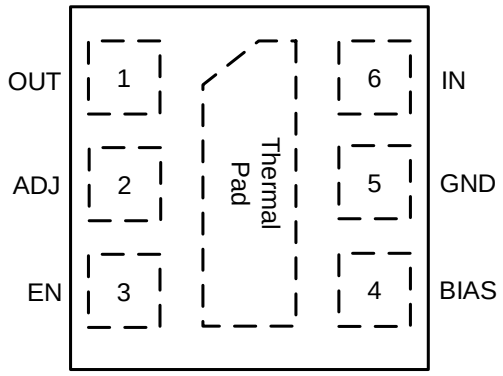
Features

- Wide VIN Input Voltage Range: 0.8V to 5.5V
- Wide VBIAS Voltage Range: 2.7V to 5.5V
- ADJ Output Voltage Range: 0.8V to 3.6V
- Very Low VBIAS Input Current of Typ. 80μA
- Ultra Low Dropout: Typ. 240mV at 800mA, 1.1V Output, 3.3V Bias
- Built-in Over Current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit
- Built-in Under Voltage Lock-out
- Stable with a 2.2μF Ceramic Capacitor
- Package: DFN6 (1.2mm × 1.2mm × 0.4mm)
- MSL: Level 1

Applications

- Constant-voltage Power Supply for Battery-Powered Device
- Constant-voltage Power Supply for Smartphones, Tablets
- Constant-voltage Power Supply for Cameras, DVRs, STB and Camcorders

Pin Configuration

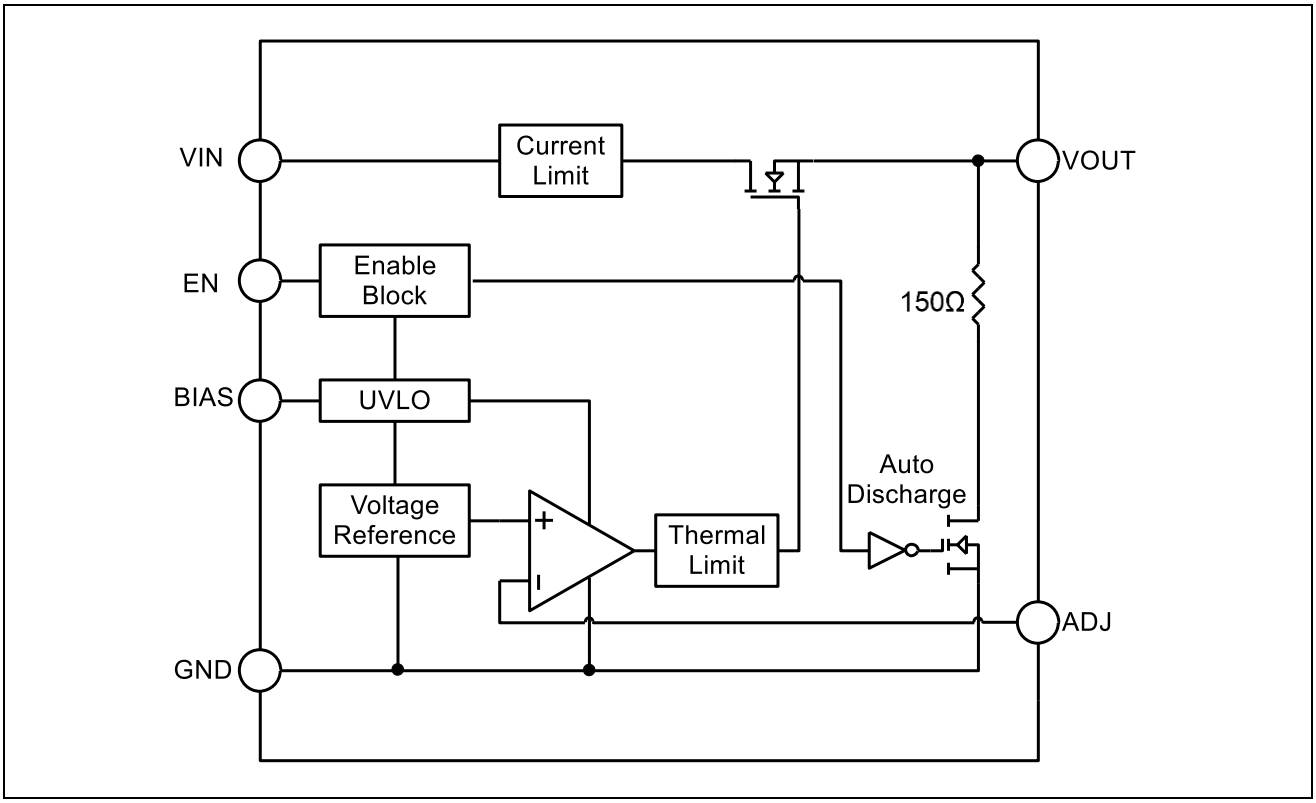


(Top View)

Pin Function

Pin Name	Symbol	Pin Description
1	OUT	The power output of the device.
2	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
3	EN	Enable Input.
4	BIAS	Input voltage for controlling circuit.
5	GND	Ground pin.
6	IN	Input voltage Pin. Large bulk capacitance should be placed closely to this pin. A 1μF ceramic capacitor is recommended at this pin.
	TP	Thermal pad, connect to GND

Block Diagram



Functional Description

The ET551ADJY1B dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET551ADJY1B offers smooth monotonic start-up.

Input and Output Capacitor

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2μF to 4.7μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available (PCB inductance in VIN and/or VBIAS inputs as example), the recommended C_{IN} = 1uF and C_{BIAS}= 0.1uF or greater.

Enable Pin Operation

The ET551ADJY1B is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with VBIAS to keep the LDO in operating mode.

Current Limit Protection

When output current of VOUT pin is higher than current limit threshold or the VOUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool down. When the junction temperature reduces to approximately +145°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time. The Auto-Discharging function is optional.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from V_{REF} to 3.6 V using two external resistors. Typical application schematics is shown blow.

$$\mathbf{V_{OUT} = V_{REF} \times (1+R1/R2)}$$

Typical value of V_{REF} is 0.8V. It is recommended to keep the total serial resistance of resistors (R1+R2) not greater than 100KΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage(VIN Pin)	-0.3 to 6.0	V
V_{BIAS}	Input Voltage (VBIAS Pin)	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V_{FB}	Input Voltage (ADJ Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage	-0.3 to 6.0	V
I_{OUT_MAX}	Maximum Load Current	800	mA
$PD_{\_MAX}$	Maximum Power Consumption	640	mW
T_{STG}	Storage Temperature Range	-65 to +150	ºC
T_J	Operating Junction Temperature	-40 to +150	ºC
V_{ESD}	Human Body Model (JESD22-A114)	±4000	V
	Charged Device Model (JESD22-C101)	±1500	V
I_{LU}	Latch up Current Maximum Rating (JESD78E)	±200	mA

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	IN Input Voltage	V_{OUT}+ V_{DROP} to 5.5	V
V_{BIAS}	BIAS Input Voltage	2.7 to 5.5 & V_{BIAS}>=V_{OUT}+1.4V	V
I_{OUT}	Output Current	0 to 800	mA
T_A	Operating Ambient Temperature	-40 to 85	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	0.47 to 10	µF
C_{BIAS}	Effective Input Ceramic Capacitor Value	0.047 to 4.7	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted , V_{IN}=V_{OUT}+0.3V,V_{BIAS}=V_{OUT}+1.6V,I_{OUT}=1mA, C_{IN}=1μF,C_{OUT}=2.2μF,C_{BIAS}=0.1uF, T_A= -40ºC~85ºC.Typical values are at. T_A=25ºC)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN} (1)	V_{IN}>V_{OUT}	V_{OUT}+ V_{DROP}		5.5	V
V_{BIAS} Voltage Range	V_{BIAS}	V_{BIAS}>V_{OUT}+1.4V	2.7		5.5	V
Under-voltage Lock-out	V_{UVLO}	V_{BIAS} Rising / Hysteresis		1.6/0.2		V
V_{BIAS} Current	I_{Q_ON} (4)	Active mode: V_{EN}=V_{BIAS}		80	110	μA
	I_{Q_OFF}	V_{EN}=0V		0.5	1	μA
V_{OUT} Voltage	V_{OUT}	I_{OUT}=1~800mA, T_A=25ºC OUT connected to ADJ	784		816	mV
		I_{OUT}=1~500mA, T_A=-40ºC~85ºC, OUT connected to ADJ	784		816	mV
		I_{OUT}=1~800mA, T_A=-40ºC~85ºC, OUT connected to ADJ	780		820	mV
Dropout Voltage	V_{DROP} (2)	I_{OUT}=500mA, V_{OUT}=1.2V, V_{BIAS}=2.8V		150	250	mV
		I_{OUT}=800mA, V_{OUT}=1.2V, V_{BIAS}=2.8V		240	400	
		I_{OUT}=500mA, V_{OUT}=1.8V, V_{BIAS}=3.2V		160	260	
Current Limit	I_{LIM}		800	1150	1550	mA
Load Regulation	Reg_{LOAD}	V_{BIAS}=2.7V or V_{OUT}+1.6V, whichever is greater, 1mA≤I_{OUT}≤800mA		2	20	mV
V_{IN} Line Regulation	Reg_{LINE}	V_{OUT}+0.3V≤V_{IN}≤5 V (V_{BIAS} =2.8V, I_{OUT}=1mA)		0.01	0.1	%/V
V_{BIAS} Line Regulation		2.7V or V_{OUT}+1.4V, whichever is greater < V_{BIAS} < 5.5 V (V_{IN}=V_{OUT}+0.3V, I_{OUT}=1mA)		0.01	0.1	%/V
Ripple Rejection	PSRR(3)	V_{BIAS}=2.7V or V_{OUT}+1.6V, whichever is greater , V_{IN} to V_{OUT}, f=1kHz, Ripple 0.2Vp-p, I_{OUT}=30mA		80		dB
		V_{BIAS}=2.7V or V_{OUT}+1.6V, whichever is greater ,V_{BIAS} to V_{OUT} , f=1kHz, Ripple 0.2Vp-p, I_{OUT}=30mA		80		
Output Noise	e_N(3)	V_{IN}= V_{OUT}+0.5V, f= 10 Hz to 100 kHz		50× V_{OUT}		μV_{RMS}

Electrical Characteristics(Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pull-down Current	I_{EN}	V_{EN}=5.5V		0.5	1	μA
EN Input Voltage High	V_{ENH}		0.9			V
EN Input Voltage Low	V_{ENL}				0.4	V
Output Resistance of Auto Discharge at Off state	R_{DIS}	V_{EN}=0V, V_{OUT} =0.5V		150		Ω
Line Transient	V_{TRLN} (3)	V_{IN}= V_{OUT}+0.3V to 5.5V in 10us, I_{OUT}=1mA，T_A=25ºC		5	30	mV
		V_{IN}=5.5V to V_{OUT}+0.3V in 10us, I_{OUT}=1mA，T_A=25ºC		5	30	mV
Load Transient	V_{TRLD} (3)	I_{OUT}=1mA to 500mA in 10us V_{IN}= V_{OUT}+0.5V, V_{BIAS}=2.7V or V_{OUT}+1.6V, whichever is greater, T_A=25ºC		110	180	mV
		I_{OUT}=500mA to 1mA in 10us V_{OUT}+0.5V, V_{BIAS}=2.7V or V_{OUT}+1.6V, whichever is greater, T_A=25ºC		85	120	mV
Turn-On Time	T_{ON}	From assertion of V_{EN} to V_{OUT}=98%$V_{OUT(NOM)}$		120		μs
Thermal Shutdown Temperature	T_{TSD}	Temperature increasing		165		ºC
Thermal Shutdown Released Temperature	T_{TSR}	Temperature decreasing		145		ºC

Notes:

1: The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$).

The calculation formula is as follows:

$$\mathbf{P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}}$$

The maximum power consumption of the circuit is 640mW.

$$\mathbf{V_{IN(MAX)} = 640mW / I_{OUT} + V_{OUT}}$$

For example:

If V_{OUT}= 1.1V, I_{OUT}=800mA, The maximum input voltage is $V_{IN(MAX)}$=640mW / 800mA+1.1=1.9V

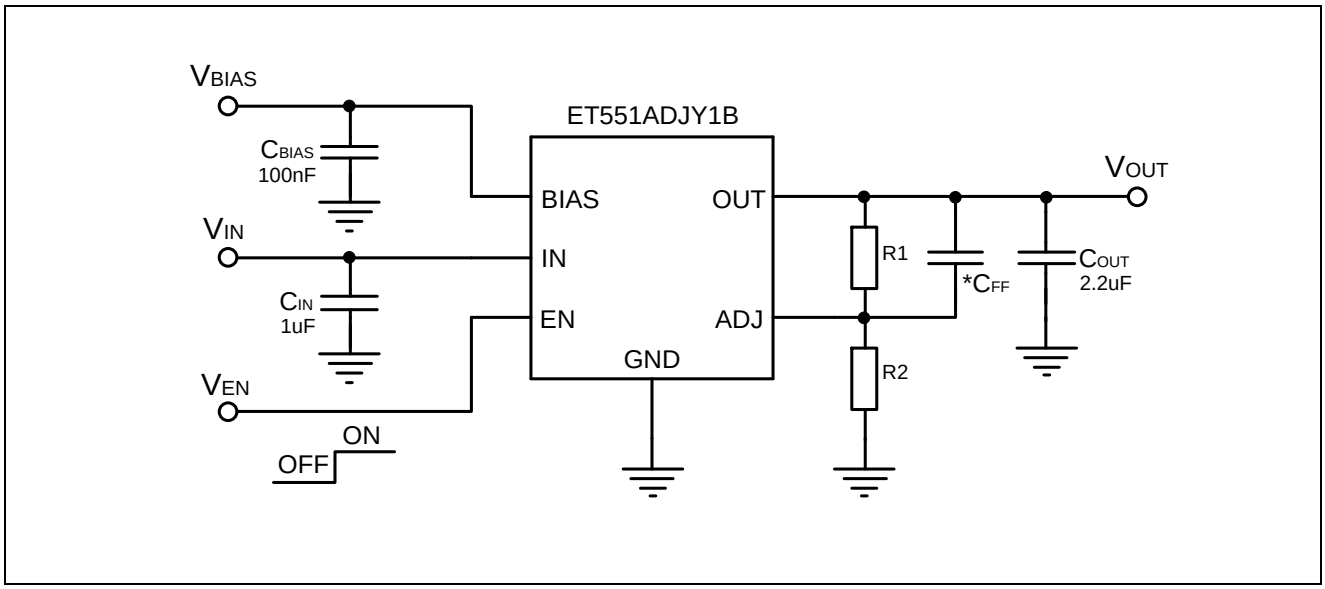
If I_{OUT} >500mA, V_{BIAS} should be bigger than V_{OUT}+1.6V.

2: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} +$V_{DROPMAX}$ with output current.

3: Guaranteed by design and characterization. not a FT item.

4: Since the power on process of BIAS needs a large current, the BIAS input voltage should have a current driving capacity of more than 120mA.

Application Circuits



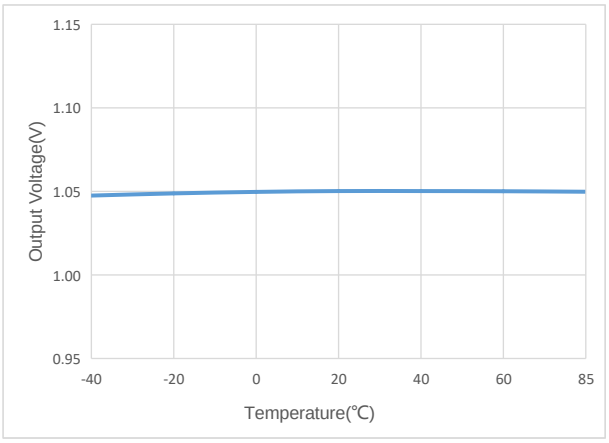
Notes*:

1: Adjust Version: V_{OUT} = 0.8×(1+R1/R2), (R1+R2) no greater than 100kΩ.

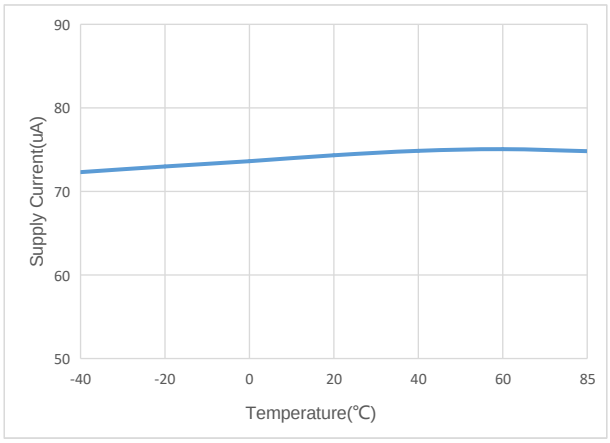
2: The feedforward capacitor C_{FF} is optional for the optimization of transient response.

Typical Characteristics

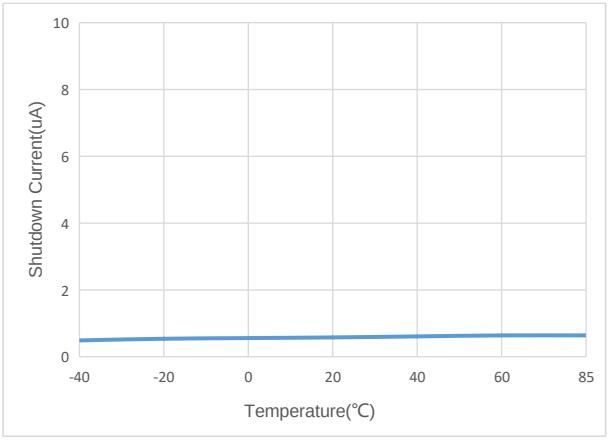
(V_{OUT}=1.05V,V_{IN}=V_{OUT}+0.3V,V_{BIAS}=V_{OUT}+1.6V,C_{IN}=1μF,C_{OUT}=2.2μF,C_{BIAS}=1uF,T_A= -40ºC~+85ºC)



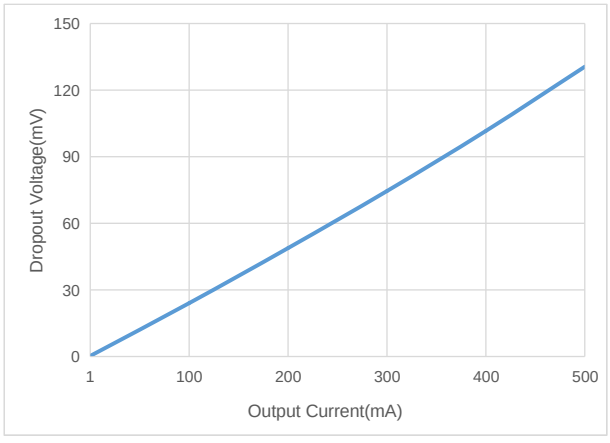
Output Voltage VS Temperature



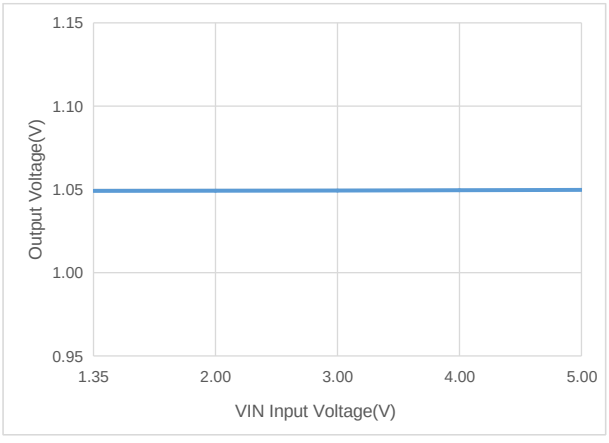
Supply Current VS Temperature



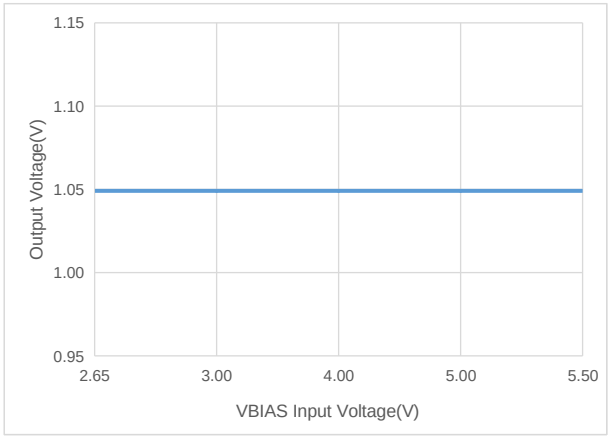
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



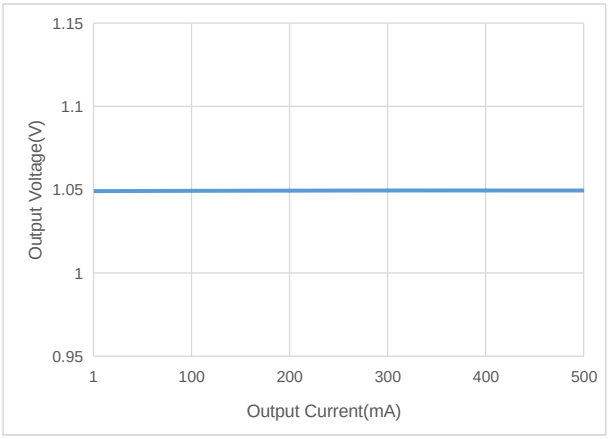
Output Voltage VS VIN Input Voltage



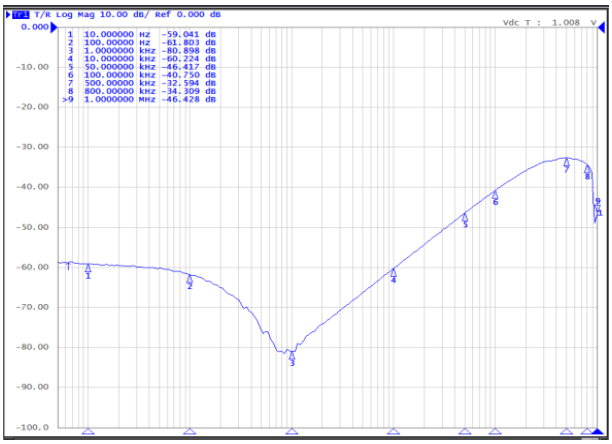
Output Voltage VS VBIAS Input Voltage

Typical Characteristics(Continued)

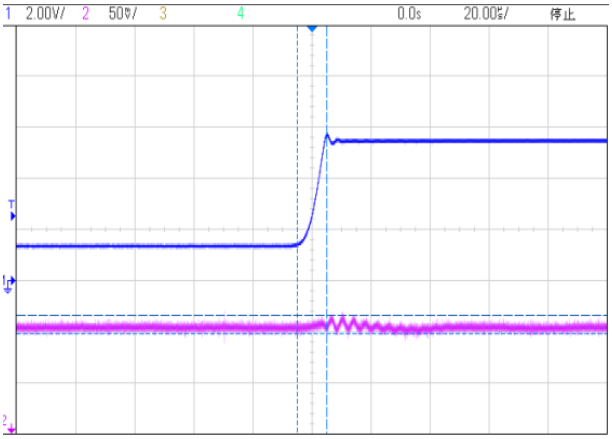
(V_{OUT}=1.05V,V_{IN}=V_{OUT}+0.3V,V_{BIAS}=V_{OUT}+1.6V,C_{IN}=1μF,C_{OUT}=2.2μF,C_{BIAS}=1uF,T_A= -40ºC~+85ºC)



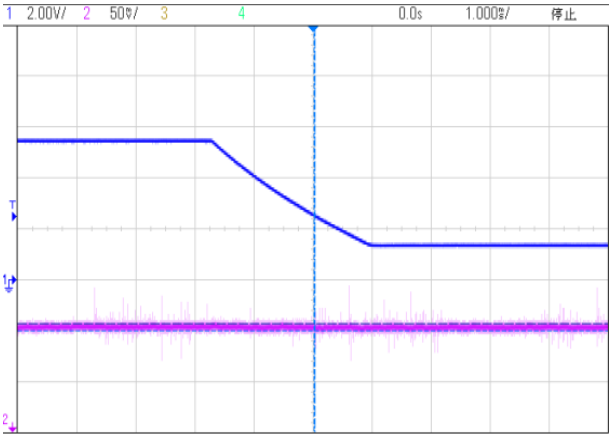
Output Voltage VS Output Current



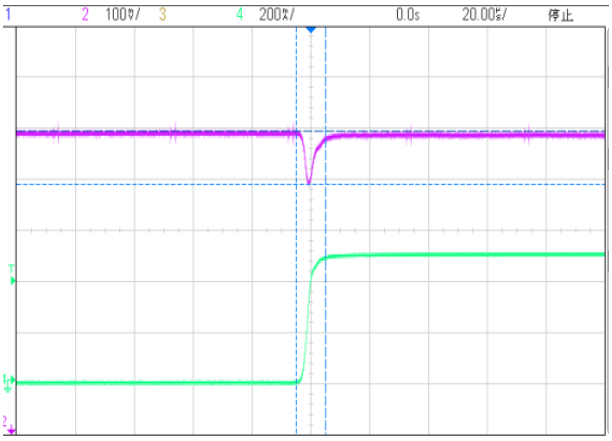
PSRR



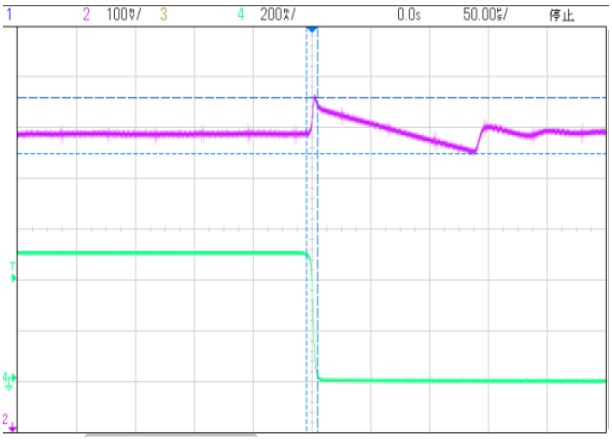
Input Transient(1.35~5.5V t=10us 1mA)



Input Transient(5.5~1.35V)



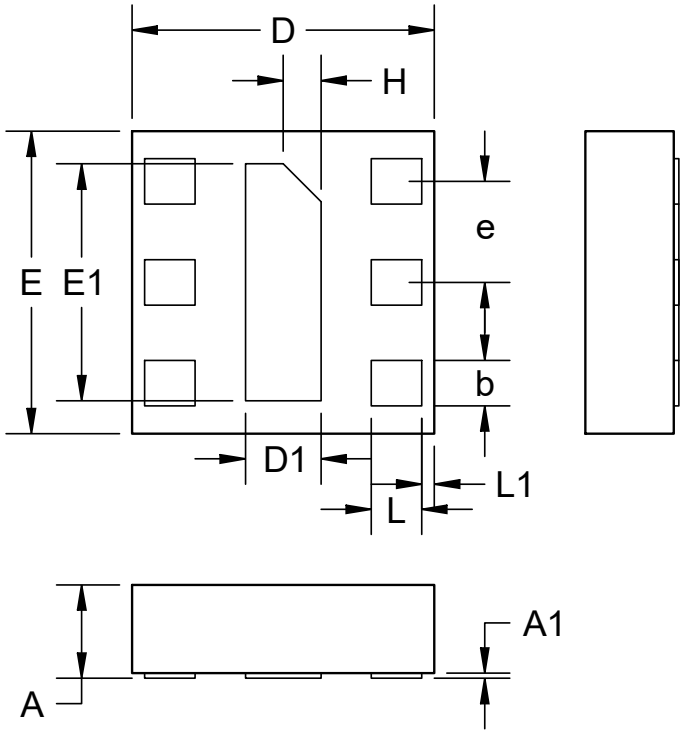
Load Transient(1mA~0.5A t=10us)



Load Transient(0.5A~1mA t=10us)

Package Dimension

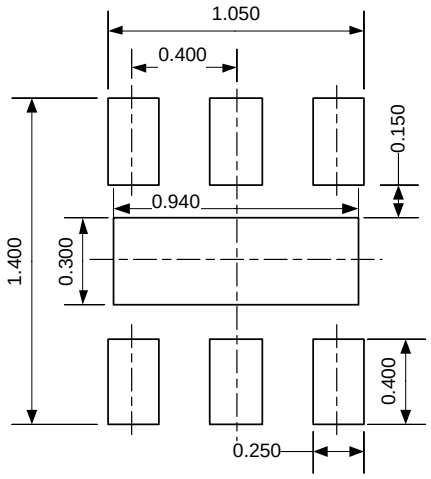
DFN6(1.2×1.2)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

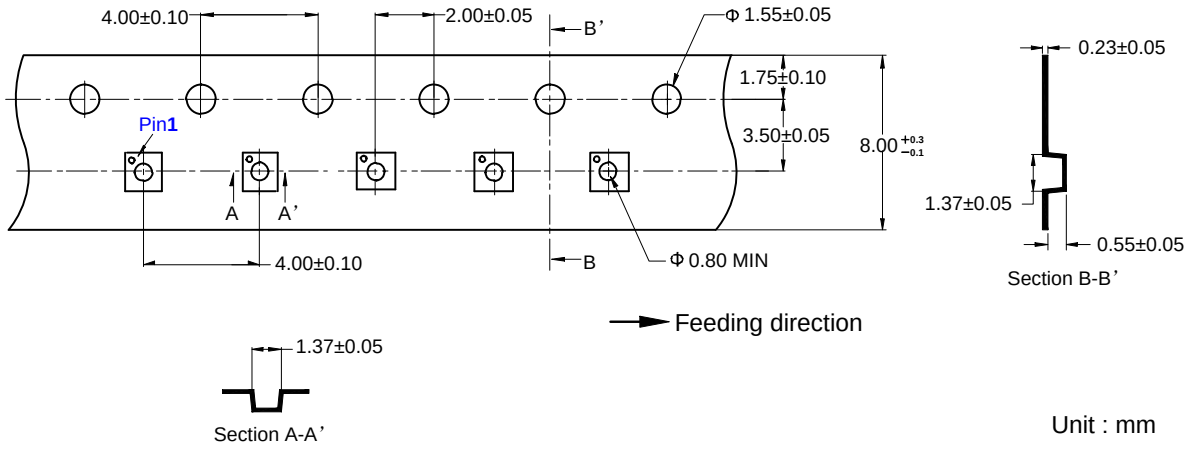
SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.50
A1	0	0.02	0.05
b	0.13	0.18	0.23
D	1.10	1.20	1.30
D1	0.25	0.30	0.35
E	1.10	1.20	1.30
E1	0.89	0.94	0.99
e	0.30	0.40	0.50
L	0.15	0.20	0.25
L1	0	0.05	0.10
H	0.15REF		

Recommend PCB Layout



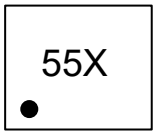
Unit : mm

Reel



Unit : mm

Marking Information



55 - Part Number

X - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-08-07	Initial Version	Liuyg	Liuyg	Liujy
1.1	2019-10-15	Clear V_{OUT} test condition, add recommended operating conditions	Liuyg	Liuyg	Liujy
1.2	2019-12-11	Add Tape Information	Liuyg	Liuyg	Liujy
1.3	2020-08-18	Add recommend PCB layout	Shib	Shib	Liujy
1.4	2020-08-26	Add Marking	Caixw	Caixw	Zhujl
1.5	2020-08-31	Add Characteristics	Shibo	Shibo	Zhujl
1.6	2020-11-13	Add MSL level and ESD Result	Liuyg	Liuyg	Liujy
1.7	2021-01-06	Add Thermal Resistance, Junction-to-Air in AMR and adjust the format	Wuxj	Wuxj	Liujy
1.8	2021-04-06	Update minimum VBIAS voltage	Liuyg	Liuyg	Liujy
1.9	2021-04-22	Update V_{DROP} in EC table	Liuyg	Liuyg	Liujy
2.0	2021-04-28	Update height of dimension	Zhujl	Zhujl	Zhujl
2.1	2021-07-09	Add note 4 for I_{Q_ON}	Liuyg	Liuyg	Liujy
2.2	2023-07-18	Update format, thickness	Shibo	Liuyg	Liujy
2.3	2023-12-28	Update package thickness	Tugz	Liuyg	Liujy
2.4	2024-05-11	Add I_{OUT}=1~500mA V_{OUT} Range	Tugz	Liuyg	Liujy