Phase-Noise Two-Channel Clock Fan-Out Buffer

General Description

The ET3RL02 is a two-channel clock fan-out buffer, which is ideal for use in portable end-equipment, such as mobile phones. ET3RL02 has two clock request inputs (CLK_REQ1 and CLK_REQ2), each of which enable a single clock output.

ET3RL02 has an integrated Low-Drop-Out(LDO) voltage regulator which accepts input voltages from 2.3V to 5.5V and output 1.8V, 50mA.

Features

- Low Additive Noise
- Limited Output Slew Rate for EMI Reduction (1ns to 5ns Rise/Fall Time for 10pF to 50pF Loads)
- Adaptive Output Stage Controls Reflection
- Regulated 1.8V Externally Available I/O Supply
- Ultra-Small WLCSP8 (0.8mm × 1.6mm, 0.4mm Pitch) Package
- ESD Performance Exceeds JESD22:

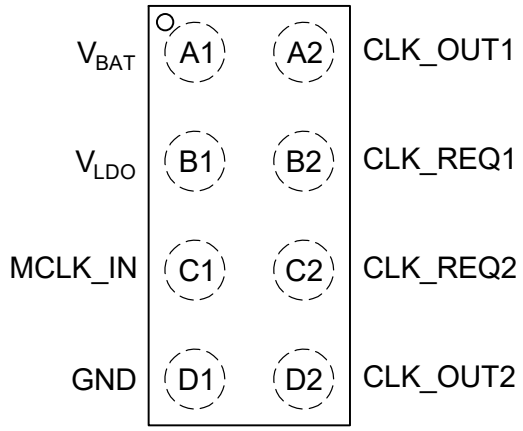
  -- 2000V Human-Body Model (JESD22-A114-A) Pass

  -- 1000V Charged-Device Model (JESD22-C101-A) Pass

Applications

- Mobile Phones
- Global Positioning Systems (GPS)
- Wireless LAN
- FM Radio

Pin Configuration

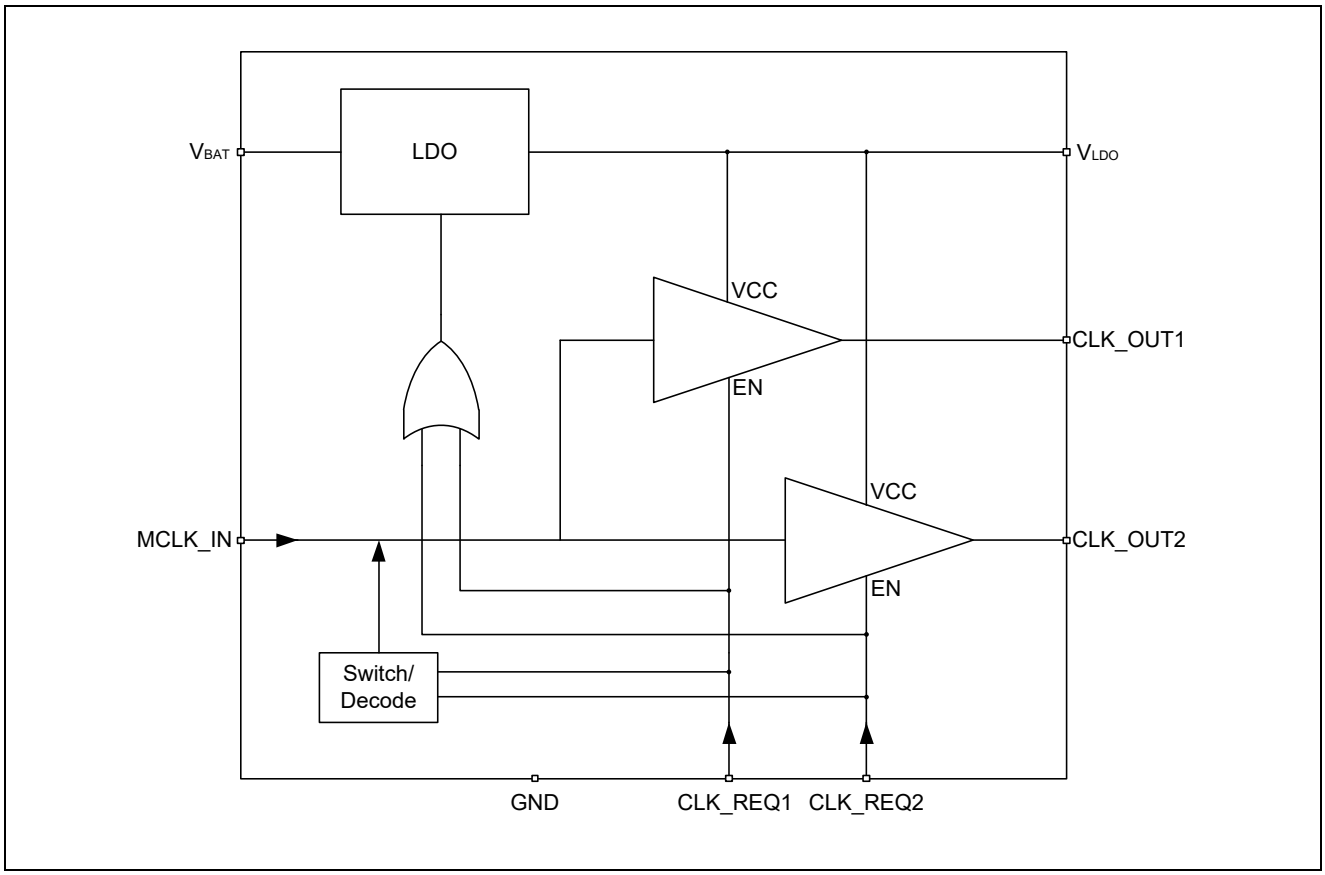


TOP VIEW

Pin Function

Pin No.	Pin Name	Pin Function
A1	V_{BAT}	Input to internal LDO
A2	CLK_OUT1	Clock output 1
B1	V_{LDO}	1.8V I/O supply for ET3RL02 and external TCXO
B2	CLK_REQ1	Clock request 1 (from peripheral) for Clock output 1
C1	MCLK_IN	Master clock input
C2	CLK_REQ2	Clock request 2 (from peripheral) for Clock output 2
D1	GND	Ground
D2	CLK_OUT2	Clock output 2

Block Diagram



Device Functional Modes

INPUTS			OUTPUTS	
CLK_REQ1 (1)	CLK_REQ2 (1)	MCLK_IN	CLK_OUT1	CLK_OUT2
L	L	X	L	L
L	H	CLK	L	CLK
H	L	CLK	CLK	L
H	H	CLK	CLK	CLK

Note(1): If a CLK_OUT will always be enabled, it is acceptable to tie its CLK_REQ pin to an external 1.8V source (not V_{LDO}).

Application Information

Input Clock Squarer

Figure 1 shows the input stage of the ET3RL02. The input signal at MCLK_IN can be a square wave or sine wave. C_{MCLK} is an internal AC coupling capacitor that allows a direct connection from a temperature compensated crystal oscillator (TCXO) to the ET3RL02 without an external capacitor.

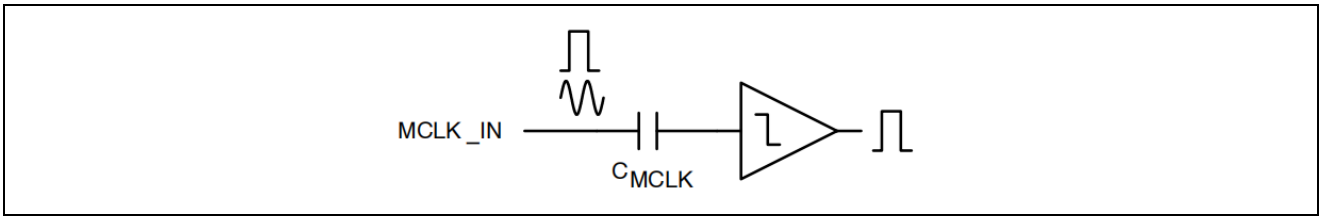


Figure 1. Input Stage with Internal AC Coupling Capacitor

The addition of any external components on the clock signal may increase the phase noise and jitter. The error source related to the internal decoupling capacitor is included in the specification of the ET3RL02. The recommended clock frequency band of the ET3RL02 is 10MHz to 52MHz for specified functionality.

All performance indicators are specified at 26MHz. The lowest acceptable sinusoidal signal amplitude is 0.8 V_{PP} for specified performance.Amplitudes as low as 0.3V_{PP} are acceptable but with reduced phase-noise and jitter performance.

Output Stage

Each output drives 1.8V LVCMOS levels. Adaptive output buffers limit the rise/fall time of the output to within 1ns to 5ns with load capacitance between 10pF and 50pF. Fast slew rates introduce EMI into the system. Each output buffer limits EMI by keeping the rise/fall time above 1ns. Slow rise/fall times may cause additive phase noise and duty cycle errors of the load device. So the output buffer will reduce these errors by keeping the rise/fall time within 5ns.

In addition, the output stage dynamically alters impedance according to the instantaneous voltage level of the output. This dynamic change reduces reflections keeping the output signal monotonic during transitions. Each output is active low when not requested to avoid false clocking of the load device.

LDO

The integrated 1.8V low noise LDO provide the I/O supply for the output buffers. The external output of LDO available to power a clock source such as a TCXO. A clean supply is provided to the clock buffers and the clock source for optimum phase noise performance. The input range of the LDO allows the device to power directly from a single cell Li battery. The LDO is enabled by either of the CLK_REQ_N signals. When the device is disabled, it enters a low-power shutdown mode with battery consumption less than 1μA. The LDO requires an output decoupling capacitor in the range of 1μF to 10μF with an equivalent series resistance (ESR) of at least 0.1Ω for compensation and high-frequency PSR. This capacitor must stay within the specified range for capacitance and ESR over the entire operating temperature range.

A ceramic capacitor can be used if a small external resistance is added in series with it to increase the effective ESR. An input bypass capacitor of 1μF or larger is recommended

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

Symbol	Parameter		Min	Max	Unit
V_{MAX}	Voltage range [(2)]	V_{BAT}	-0.3	7.0	V
		CLK_REQ1/2	-0.3	5.0	V
		MCLK_IN,V_{LDO},CLK_OUT1/2	-0.3	2.19	V
I_{IK}	Input clamp current at VBAT, VI<0	CLK_REQ1/2, and MCLK_IN		-50	mA
I_{MAX1}	Continuous output current	CLK_OUT1/2		±20	mA
I_{MAX2}	Continuous current through GND	V_{BAT}, V_{LDO}		±50	mA
T_J	Operating virtual junction temperature		-40	150	°C
T_{STG}	Storage temperature range		-65	150	°C

***Note2*:** All voltage values are with respect to network ground pin.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{BAT}	Input voltage to internal LDO		2.3	5.5	V
V_I	Input voltage	MCLK_IN, CLK_REQ1/2	0	1.89	V
V_O	Output voltage	CLK_OUT1/2	0	1.8	V
V_{IH}	High-level input voltage	CLK_REQ1/2	1.3	1.89	V
V_{IL}	Low-level input voltage	CLK_REQ1/2	0	0.5	V
I_{OH}	High-level output current, DC current		-8		mA
I_{OL}	Low-level output current, DC current			8	mA
C_{LDO}	Effective V_{LDO} output ceramic capacitor value		0.47	10	uF
ESR	V_{LDO} output capacitor equivalent series resistance (ESR)		5	100	mΩ
T_A	Operating ambient temperature range		-40	85	°C

All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
LDO							
V_{OUT}	LDO output voltage	I_{OUT} = 50mA		1.71	1.8	1.89	V
C_{LDO}	External load capacitance			1		10	μF
$I_{OUT(SC)}$	Short circuit output current	R_L = 0Ω			100		mA
$I_{OUT(PK)}$	Peak output current	V_{BAT} = 2.3V, V_{LDO} = V_{OUT} – 5%				180	mA
PSRR	Power supply rejection	V_{BAT} = 2.3V, I_{OUT} = 2mA	f_{IN}= 217Hz & 1kHz	60			dB
			f_{IN}=3.25MHz	40			
eN	Output noise	10Hz to 100kHz T_A=25°C	I_{LDO}=1mA		17		uV_{RMS}
			I_{LDO}=50mA		25		uV_{RMS}
T_{SU}	LDO startup time	V_{BAT} = 2.3 V , C_{LDO} = 1 μF, CLK_REQN to V_{IH} = 1.71V			0.2		ms
		V_{BAT} = 5.5V, C_{LDO} = 10μF, CLK_REQN to V_{IH} = 1.71V				1	
POWER CONSUMPTION							
I_{SB}	Standby current	Device in standby (all $V_{CLK\_REQ\_N}$ = 0 V)			0.2	1	μA
I_{CCS}	Static current consumption	Device active but not switching			0.4	1	mA
I_{OB}	Output buffer average current	f_{IN} = 26MHz, C_{LOAD} = 50pF			4.2		mA
C_{PD}	Output power dissipation capacitance	f_{IN}= 26MHz				44	pF
MCLK_IN INPUT							
I_{I1}	CLK_REQ1/2 leakage current	V_I = V_{IH} or GND				1	μA
I_{I2}	MCLK_IN	CLK_REQ1&2=GND, V_{LDO}=1.8V				1	uA
R_I	MCLK_IN impedance	f_{IN} = 26MHz			6		kΩ
F_{IN}	MCLK_IN frequency range			10	26	52	MHz

Electrical Characteristics(Continued)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
MCLK_IN LVCMOS SOURCE							
	Additive phase noise	f_{IN} = 26MHz, tr/tf ≤ 1ns	10Hz		-117		dBc/ Hz
			100Hz		-129		
			1kHz offset		-140		
			10kHz offset		-149		
			100kHz offset		-153		
			1MHz offset		-148		
	Additive jitter	f_{IN} = 26MHz, V_{PP} = 0.8V, BW = 10K～5MHz			0.37		ps (rms)
t_{DL}	MCLK_IN to CLK_OUTn propagation delay				10		ns
DCL	Output duty cycle	f_{IN} = 26MHz, DC_{IN} = 50%		45	50	55	%
MCLK_IN SINUSOIDAL SOURCE							
V_{MA}	Input amplitude						V
	Additive phase noise (3)	f_{IN} = 26MHz, V_{MA} = 1.8V_{PP}	10Hz		-118		dBc/ Hz
			100Hz		-130		
			1kHz offset		-141		
			10kHz offset		-149		
			100kHz offset		-152		
			1MHz offset		-148		
		f_{IN} = 26MHz, V_{MA} = 0.8V_{PP}	10Hz		-116		
			100Hz		-128		
			1kHz offset		-139		
			10kHz offset		-146		
			100kHz offset		-150		
			1MHz offset		-146		
	Additive jitter (3)	f_{IN} = 26MHz, V_{MA} = 1.8V_{PP}, BW = 10K～5MHz			0.41		ps (RMS)
t_{DS}	MCLK_IN to CLK_OUT1/2 propagation delay				12		ns
DCs	Output duty cycle	f_{IN} = 26MHz, V_{MA} > 1.8V_{PP}		45	50	55	%

Electrical Characteristics(Continued)

Over operating free-air temperature range (unless otherwise noted)

CLK_OUT_N OUTPUTS						
tr	20% to 80% rise time	C_L = 10pF to 50pF	1		5	ns
tf	20% to 80% fall time	C_L = 10pF to 50pF	1		5	ns
tsk	Channel-to-channel skew (3)	C_L = 10pF to 50pF (C_{L1} = C_{L2})	-0.5		0.5	ns
V_{OH}	High-level output voltage	I_{OH} = -100μA, reference to V_{LDO}	-0.1			V
		I_{OH} = -8mA	1.2			
V_O	Low-level output voltage	I_{OL} = 20μA			0.2	V
		I_{OL} = 8mA			0.55	

Note3 :Guaranteed by design and characterization. not a FT item.

Typical Application

The ET3RL02 is ideal for use in mobile applications as shown in Figure 2. In this example, a single low noise TCXO system clock source is buffered to drive a mobile GPS receiver and WLAN transceiver. Each peripheral independently requests an active clock by asserting a single clock request line (CLK_REQ1 or CLK_REQ2). when both clock request lines are inactive, the ET3RL02 enters a low current shutdown mode. In this mode the LDO output, CLK_OUT1, and CLK_OUT2 are pulled to GND and the TCXO will be unpowered.

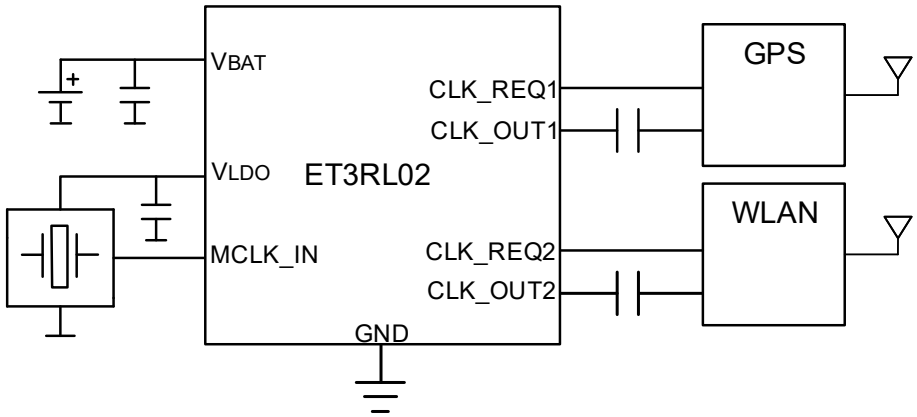
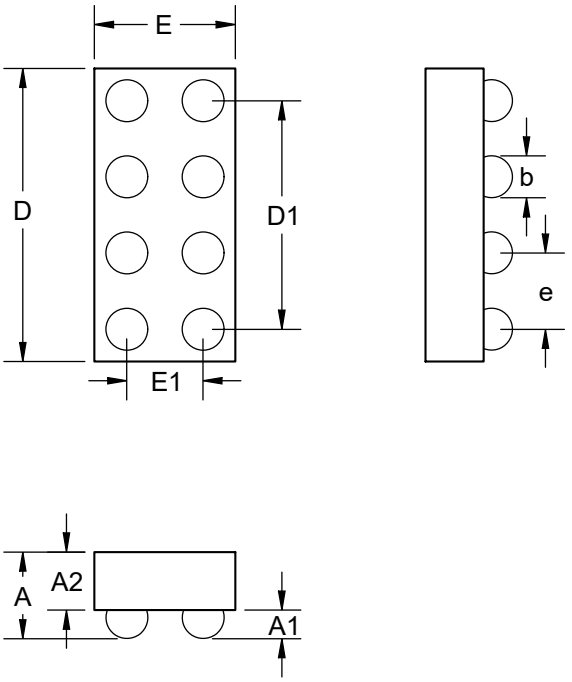


Figure 2. Mobile Application.

Package Dimension

WLCSP8



COMMON DIMENSIONS

(UNITS OF MEASURE = MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.405	0.455	0.505
A1	0.125	0.150	0.175
A2	0.280	0.305	0.330
b	0.195	0.220	0.245
D	1.510	1.540	1.570
D1	1.200BSC		
E	0.710	0.740	0.770
E1	0.400BSC		
e	0.400BSC		

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2020-10-15	Preliminary Version	Shilj	Shilj	Zhujl
1.0	2021-7-6	Initial Version	Shilj	Shilj	Zhujl
1.1	2021-8-19	Add remark in EC table	Shilj	Shilj	Liujy
1.2	2021-9-26	Add Output Noise and C_P value	Shilj	Shilj	Liujy
1.3	2021-10-8	Add C_{LDO} and ESR	Shilj	Shilj	Liujy
1.4	2022-11-15	Update Typeset	Tianqh	Shilj	Zhujl